On-Chip Inductance Modeling and Analysis

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Abstract

With operating frequencies approaching the gigahertz range, inductance is becoming an increasingly important consideration in the design and analysis of on-chip interconnect. We present an accurate technique for modeling and analyzing the effects of parasitic inductance on power grid noise, signal delay and crosstalk. We propose a detailed circuit model composed of interconnect resistance, inductance and distributed capacitance, device decoupling capacitances, quiescent activity in the grid, pad locations, and pad/package inductance which accurately determines current distribution and, hence, on-chip inductive effects, and proves superior to the traditional simplified loop inductance approach. The model uses partial inductances, computed using an analytical formula for a pair of parallel rectangular conductors spaced in any relative position. We present experimental results, obtained from simulations of industrial circuits, that show the importance of various model components while analyzing on-chip inductance. We also propose a simple sparsification technique to handle large, dense partial inductance matrices.

1 Introduction

Inductance effects in on-chip interconnect structures have become increasingly significant[1] due to longer metal interconnects, reductions in wire resistance (as a result of copper interconnects and wider upper-layer metal lines) and higher frequency operation. These effects are particularly significant for global interconnect lines such as those in clock distribution networks, signal buses, and power grids for high-performance microprocessors. On-chip inductance impacts these in terms of delay variations, degradation of signal integrity due to overshoots/oscillations, aggravation of signal crosstalk, and increased power grid noise.

The main difficulty in the extraction and simulation of on-chip inductance is the fact that inductance is a function of a closed current loop. Therefore, it is required that both the current through a signal net and the return currents through the power grid be considered simultaneously instead of being analyzed in isolation. The current distribution in the entire circuit, including the grid, must be known in order to obtain a correct estimate of loop inductance.

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However, actual chip topologies consist of complex power grid and signal line structures, and current distribution depends on many elements, including device and interconnect decoupling capacitance, power grid resistance and inductance, pad locations, and operating frequency. Thus, the determination of current paths and, hence, the inductance is quite difficult, since it requires the accurate modeling and simulation of the complete signal net and power grid topology.

Traditional approaches to inductance analysis are based on simple loop inductance models[2], [3], [4]. The loop inductance and resistance are extracted by defining ports at the driving gate, and then solving the current distribution for an RL model of the circuit using tools such as FastHenry[5]. The extracted inductance and resistance are then combined with lumped capacitance to construct a netlist. While extracting the inductance, current distribution is determined solely by the resistance and inductance of the conductors. This leads to significant inaccuracies, since the interconnect and device decoupling capacitances strongly affect current return paths. Also, defining a port at the driving gate ignores other current paths, such as the short-circuit gate current and the power grid current generated by the switching of other gates in the vicinity of the signal net. However, the simplicity of the loop inductance model means it is faster to simulate, and can be used as a pre-layout estimation methodology.

Alternative approaches use the Partial Equivalent Elements Circuit (PEEC)[6] method based on partial inductances, which can be defined for wire segments. The PEEC method can be used to construct a circuit model that does not require the predetermination of current loops. PEEC models have been used to obtain more accurate current distribution[7]. However, such techniques have been applied to highly simplified structures like coplanar waveguides. In addition, they ignore important components that determine current paths, and hence lack accurate estimation capability.

In this paper, we propose an accurate and comprehensive PEEC-based model of on-chip inductance that includes the elements listed below.

1. Interconnect resistance, capacitance and partial inductance
2. Device decoupling capacitances between power grids
3. Power/ground pad locations and inductance models
4. Quiescent activity in the power/ground grids
5. Signal net driver and receiver gates

These elements have a strong impact on current distribution in a power grid and, lead to a significantly more accurate analysis of signal nets. The proposed approach was used on industrial circuits to study the effect of on-chip inductance on delay, crosstalk, and power grid noise. When comparing the PEEC model with the sim-

plified loop inductance model, we found that the latter dramatically overestimates the impact of signal inductance. It is important for the circuit designer to know the accurate impact of inductance to avoid over-designing of signal nets or shields. We also studied the impact of the number of pads and their locations, pad inductance decoupling capacitance, other switching activity in the grid, and shielding on signal net behavior.

The proposed PEEC model leads to a dense RLC circuit matrix requiring large SPICE simulation times. Hence, we further propose a sparsification technique to improve run-time by partitioning the circuit topology into sections, with no inductive coupling between two sections. The partitioning method leads to a trade-off between the run-time and simulation accuracy.

The remainder of this paper is organized as follows: In Section 2, we describe the traditional loop inductance approach and related issues. In Section 3, we present our partial inductance based model for analyzing the effects of on-chip inductance, and compare it with the loop inductance model. In Section 4, we show how our methodology can be used to model devices and interconnect and analyze the effect of each separately. Section 5 discusses our approach used to speed-up the simulation of the PEEC model using sparsification. In Section 6 we draw our conclusions.

2 Loop inductance approach

Figure 1(a) shows a typical signal net and its neighboring ground grid. The loop inductance model defines a port at the driver side of the signal line and shorts the receiver side (which actually sees a capacitive load) to the local ground, since inductance extraction is performed independent of capacitance. Typically, an extraction tool such as FastHenry[5] is used to obtain the impedance over a frequency range, as shown in Figure 1(b). A netlist is then constructed with the resistance and loop inductance of the signal and ground grid, at one frequency, as shown in Figure 1(c).

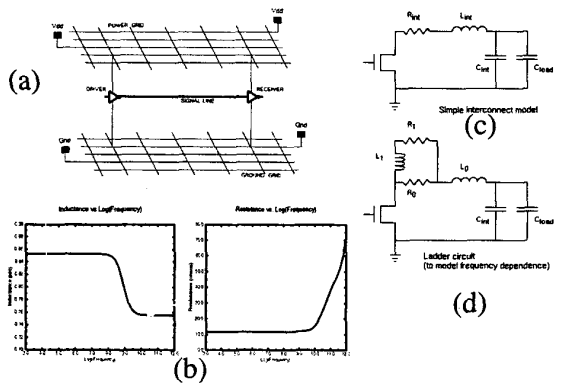


FIGURE 1. Typical grid topology, R & L vs. frequency

Note that all the interconnect and load capacitance is modeled as a lumped capacitance at the receiver end of the signal interconnect.

A recent approach[2] suggests the construction of a ladder circuit, Figure 1(d), to model the frequency dependence of resistance and inductance. The loop impedance is extracted at two frequencies, and the parameters R_0, L_0, R_1 and L_1 used in the ladder circuit in Figure 1 are computed. The lumped RLC circuit representation can also be distributed using many RLC-π segments. After the interconnect model is constructed, driver and receiver gates are connected and the complete circuit is simulated in SPICE.

The loop inductance approach makes certain assumptions about the current return paths in the grid. Whenever we define a port between two points to obtain loop inductance, it implies that all current injected from the positive port terminal will return to the negative port terminal via the grid. However, Figure 2 shows the different types of current loops that arise in the power grid when a gate drives a signal line and a load.

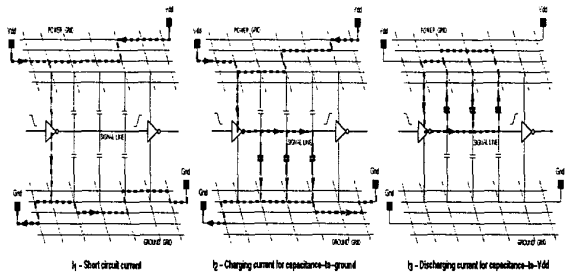


FIGURE 2. Currents in Driver-Receiver-Grid topology

1. I_1 - Short circuit current flowing from power grid to ground grid while the gate is switching.
2. I_2 - Charging current, flowing from Vdd to ground, for the interconnect capacitance and gate capacitance between signal line and ground grid.
3. I_3 - Discharging current for the interconnect capacitance and gate capacitance between signal line and power grid.

The currents I_1 and I_2 form loops throughout the package and grid decoupling capacitances, while I_3 forms a current loop from the driver output, through the grid and back, as modeled in the traditional loop inductance approach.However, I_1 and I_2 significantly impact the effective inductance seen by the signal net. Thus, simply connecting a port at the driving gate of the signal line and computing the loop inductance can result in large estimation errors. Even I_3 forms different (and smaller) loops due to the distributed nature of the interconnect capacitance as shown in Figure 2, whereas the loop model lumps this capacitance at the receiver side.

3 Proposed circuit model

Figure 3 shows the proposed partial inductance based circuit model for the study of on-chip inductance effects. A typical circuit topology consists of two supply grids (power, ground) and signal lines laid out over multiple metal layers. The gates draw power from the lowest metal layer, while external power and ground are supplied via pads to the uppermost metal layer.

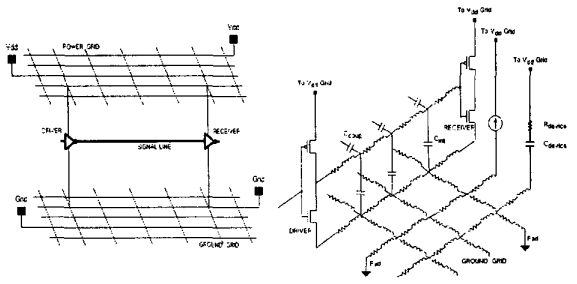


FIGURE 3. Typical power grid topology and corresponding partial-inductance circuit

The circuit model shown above consists of

- Resistance, partial self-inductance and capacitance (RLC-π) model for each metal segment.
- Mutual inductances between all pairs of parallel segments.
- Coupling cap between all pairs of adjacent metal lines.
- Via resistances between adjacent metal layers.
- Resistance and decoupling capacitance (to model non-switching gates)
- Time-varying current sources (to model switching gates)
- Pad resistances and inductances.

A detailed explanation of these model components is given later in this section. In addition to these, our model can easily be extended to include substrate models, N-well capacitance and explicit decoupling capacitance.

3.1 Interconnect RLC extraction

Each grid segment is modeled as a RLC-π circuit. The resistance is frequency-independent and is computed as a function of length, width and sheet resistance. The segment capacitance to ground and the coupling capacitances between each pair of parallel and adjacent metal lines are computed using the Chern models in our experiments. Higher accuracy models or extracted values can also be incorporated in our model. We use analytical formulae to compute partial self and mutual inductances. These hold for parallel conductors with rectangular cross-sections, placed in any relative position as shown in Figure 4.

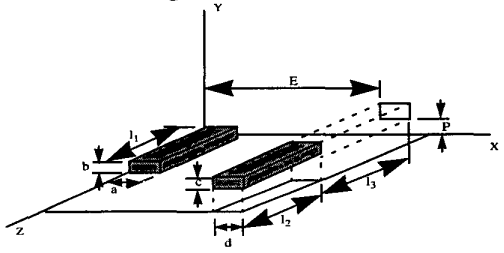


FIGURE 4. Two parallel rectangular conductors, placed in any relative position

We first compute the Geometrical Mean Distance (R) between the two conductors. This is a function of the conductor widths, thicknesses and their spacing in the X and Y dimensions. The GMD formulation was derived by developing the integral formulation given in [8]. Next, the partial self and mutual inductances are obtained using formulae that are functions of the GMD, the conductor lengths and their relative spacing in the Z dimension [9].

An alternative formulation, which includes all 3 dimensions in the same expression, can also be used to compute the inductance values[10]. These analytic formulae are exact, under the assumption of uniform current distribution. However, they ignore the skin effect and proximity effect within the conductor. For a rise-time of 100ps, the maximum frequency of interest is 3.2GHz and the skin depth is 1.53um. Thus, wider metal lines must be split into several narrow lines. These approximations were found to have errors of less than 1% in the self and mutual inductance values.

3.2 Device decoupling capacitance

During normal chip operation, approximately 10-20% of the gates switch while the remaining 80-90% remain static. These non-switching gates result in a significant decoupling capacitance effect, which reduces IR-drop and changes current distribution by allowing current to jump from one grid to the other.

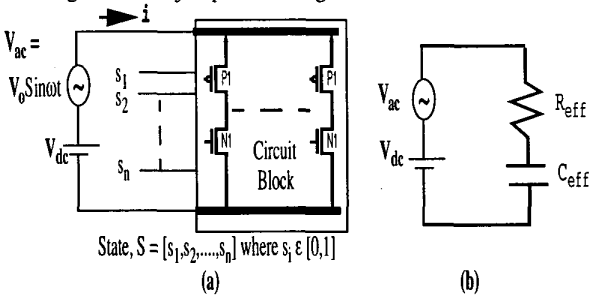


FIGURE 5. Determination of device decoupling cap

We estimate the decoupling capacitance directly using SPICE simulation of several representative circuit blocks. Figure 5(a) depicts the simulation setup. Figure 5(b) shows the equivalent RC circuit of the circuit. The input terminals of the circuit are set arbitrarily at logic 0 or 1 and the power terminals are set at a d.c. bias equal to the operating voltage. A small sinusoidal voltage is then superimposed on the supply rails to cause fluctuation in the supply voltage. Now the decoupling action of the circuit is studied by monitoring the input current. Since no devices are switched, the input current is solely in response to the fluctuation in the grid voltage, thus representing the current in the underlying RC decoupling circuit(Figure 1(b)). The C_{eff} and R_{eff} values determined for a block represent the combined decoupling action of the device capacitances and the extracted parasitic capacitances of the interconnects. We repeat the above measurements for a set of random states and take the average values for resistance and capacitance. The values of one block can be easily translated to other circuit blocks based on the circuit sizes (total transistor widths) of the blocks.

3.3 Current sources

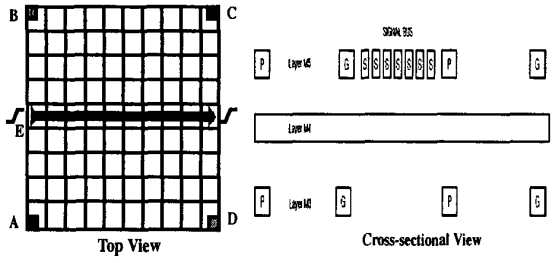
In addition to the gate driving the signal line, other gates switch simultaneously, drawing current from the Vdd grid and injecting it into the ground grid, causing voltage fluctuations and affecting current distribution. Different gates draw current at different times and in varying amounts, causing a continuously changing current profile in the grid. When the signal of interest switches, the other grid activity will be one of the factors that determines the actual current return paths and, hence, the signal inductance. Explicit modeling of all devices would lead to intractably large models. We therefore use a statistical model, consisting of time-varying current sources connected at random locations on the lowest metal layer, with a triangular wave-shape serving as a good approximation. The current value changes with time during the transient simulation, to account for different parts of the chip switching at different times.

3.4 Pad/package inductance model

External signals are routed to a chip via package leads and pads. The parasitic inductances associated with the package geometries must be modeled, since they affect on-chip behavior significantly. In our circuit model, it is assumed that the planes in the package are ideal, since the voltage difference across these planes is typically of order of few mV. Thus, the package is modeled as a rectangular bar, including the pad and a vertical via which connects the pad to a package layer.

3.5 Comparison with loop inductance model

To compare the proposed PEEC model with the traditional loop inductance model, we construct and simulate both models for the same circuit topology. The topologies of interest to us are those having long and wide signal lines, since inductive effects dominate for such interconnect lines. Hence, we consider signal lines routed on the uppermost layer, which typically carry global signals such as clocks and buses in the presence of a multi-layer power grid.



* Delay (for the signal interconnect) is measured from 50% Vdd at the driver output to 50% Vdd at the receiver input. Slope is measured from 10% Vdd to 90% Vdd at the receiver input. Undershoot is measured at the receiver input.

FIGURE 6. Experimental grid topology

Figure 6 shows a 3-layer power and ground grid along with a bus of signal lines on the uppermost layer. This topology is based on a recent high-performance microprocessor design. The power and ground grid occupy all three metal layers, while the signal bus lies on the uppermost layer M5. Each signal line is connected to driver and receiver inverters. Power and ground pads are connected as shown. The grid thus constructed has approximately 1000 nodes.

For the loop inductance model, the complete topology is fed to FastHenry and the loop inductance and resistance extracted by defining ports for each signal line. These are then combined with capacitances and gates to obtain a complete netlist which is simulated in SPICE. We also construct a detailed PEEC model and the corresponding netlist for this topology.

Figure 7 shows the simulation results for the two approaches. The loop inductance approach significantly overestimates delay* and ringing, which is undesirable since it might prompt the designer to overcompensate in the power grid or shielding structures, thereby yielding an inefficient interconnect topology. The PEEC approach more closely reflects the current distribution and circuit elements in the actual circuit and therefore provides more accurate simulation results.

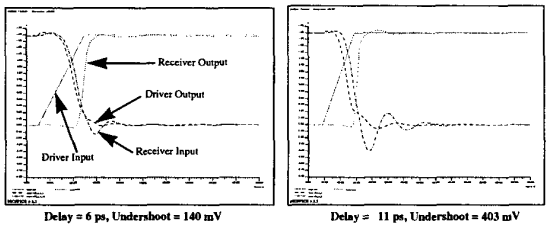


FIGURE7. Partial(left) vs. Loop inductance model(right)
Circuit area: 350 μm * 350 μm

Figure 8 shows a similar comparison for a larger circuit (700μm * 350μm). The larger topology demonstrates a worse over-estimation of inductive effects in the loop approach. The PEEC model allows us to study the effects of pad placement, pad inductance, explicit decoupling capacitances, and the switching activity of other gates in the grid. The PEEC model, with this additional information, provides an accurate and powerful methodology to study on-chip inductance.

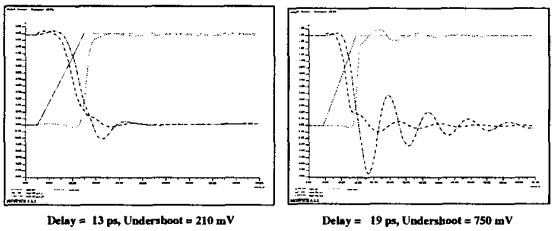


FIGURE8. Partial(left) vs. Loop inductance model(right)
Circuit area: 700 μm * 350 μm

4 Effect of model components on circuit behavior

Below we study the effects of various model components on signal behavior. These experiments have been performed on the topology described in Figure 6.

Table 1: Effect of model components on signal behavior

Row	Experiment setup	Delay (ps)	Slope (ps)	Undershoot (mV)
1	Basic topology (Figure 6)	6.1	42	140
2	Remove device decoupling cap	4.5	45	157
3	Add extra decoupling cap	6.2	40	140
4	Include pad inductances	6.0	39	240
5	1 Vdd pad at A, 1 Gnd pad at B	6.3	42	152
6	No current sources	6.5	43	165
7	3-line bus: W/O shielding	4.0	44	50
8	3-line bus: With shielding	3.3	48	8

Device decoupling capacitance / Explicit decoupling capacitance

The removal of device decoupling capacitance from the model introduces high-frequency oscillations into the transient voltages, while adding explicit decoupling capacitance at the driver and receiver reduces the inductive ringing. (Table 1: Rows 2,3)

Pad/package inductance

The inclusion of pad/package inductance in the model introduces lower-frequency oscillations into the transient waveforms. However, the node voltages on the signal lines, if measured w.r.t. the local power/ground nodes, are relatively unchanged (Table 1: Row 4). Note that only the relative voltages are important for the driver and receiver gates and signal integrity, but the absolute voltages need to be considered when analyzing global power grid noise.

Pad number / location

We simulate the experimental topology with only one power and one ground pad. Reducing the number of pads worsens the IR drop. Changing the pad locations influences current return paths and, hence, the effective inductance. With the pads located at the signal driver, undershoot is reduced and IR-drop improved near the signal line. (Table 1: Row 5,6)

Current sources

If we ignore current sources which model the switching of other gates, we notice that there is no IR-drop in the supply grids. On comparison with results from the full model, it is observed that the current sources have a damping effect on the circuit. (Table 1: Row 7)

Shielding

To study shielding effects, we model a 3-signal bus with all signals driven identically and shielded by power and ground lines between the signal lines. It is observed that such coplanar wave-guides act as nearby current return paths and reduce inductive effects. (Table 1: Rows 8,9)

5 Acceleration/Sparsification

Since our PEEC model includes all possible self and mutual inductances, the resulting circuit matrix is very dense. As an example, the topology used in the experiments (Area: 350μm * 350μm) leads to 250,000 mutual inductances, and the SPICE simulation needs 12 hours and 150MB of RAM on a Sun UltraSPARC 60. This has been the main bottleneck in the use of PEEC models, but we have developed a simple sparsification technique which reduces the circuit size and speeds up simulation.

5.1 Prior Work

The simplest approach to sparsifying the inductance matrix is to discard all mutual coupling terms falling below a certain threshold. However, this can result in indefinite matrices, which imply unstable systems. As an alternative to simple truncation, one approach associates each segment with a distributed current return path out to a shell of some radius[11]. Segments with spacing more than this radius are assumed to have no inductive coupling. However, this approach leads to complications in determining the global value of the shell radius. An extension of this work[12] uses a moment-based algorithm to compute the shell radius.

A recent approach[13] introduces return-limited inductances for sparsification and the use of "halos" to limit the number of mutual inductances. However, a chief assumption requires that the mutual inductances between signal and power grid be dropped. Our experiments with this technique indicate that it can lead to huge inaccuracies, since the power grid provides an important return path for signal currents.

Reduced-order models [14],[15] for the linear portion of the model can be combined with the gate models and simulated in SPICE. However, model order reduction algorithms such as PRIMA[16] require matrix inversion, which is expensive for the fully-dense matrix of our model. Also, they cannot handle time-varying current sources or non-linear devices, which we use to model the switching activity in the grid. However, reduced order models are very efficient in terms of simulation time and match the original large model quite accurately. They are well suited to handle large topologies or longer simulation times and also provide a control over the accuracy via the order of the reduced system.

5.2 Block diagonal sparsification

We propose a simple partitioning technique, based on circuit topology, which guarantees that the resulting sparsified matrix is positive semi-definite. We split our experimental topology into multiple sections using the following methodology:

- Within each section, we stamp the partial self inductances along with all possible partial mutual inductances.
- Between a pair of sections, there exists no mutual coupling.
- The signal bus of interest lies in the middle of the corresponding section. This ensures that the model captures the most significant inductive coupling between signal lines and power grid.
- The number of sections can be adjusted to meet sparsity or simulation time requirements.
- As we move away from the signal net, we can model sections as RC instead of RLC.

The resulting circuit matrix is then block diagonal and positive semi-definite, since each block corresponds to the fully-coupled inductance matrix of a real system. We used our partitioning technique on a range of circuits, and the results are summarized in Table 2. The fully-dense models for larger topologies lead to extremely huge inductance matrices and could not be simulated in SPICE. However, our partitioning algorithm allowed us to sparsify the matrix and reduce the circuits to reasonably-sized models.

Table 2: Results for partitioning

Circuit area	# M (before)	# M (after)	Run-time (before)	Run-time (after)
350μm * 350μm	250k	55k	12 hr.	1 hr.
700μm * 350μm	1,000k	110k	80 hr.	2 hr.
1050μm * 350μm	2,400k	165k	*	4 hr.

* Circuit was too large to be simulated.

Note that this partitioning method allows us to model and analyze moderately sized circuits. However, it is only an initial approach, and needs to be developed into a more sophisticated sparsification technique, since the proposed methodology must be able to handle much larger topologies.

6 Conclusions

We have presented a new methodology for modeling and analyzing the effects of on-chip inductance on signal and power grid integrity. The proposed circuit model consists of interconnect resistance, partial inductance and distributed capacitance, device decoupling capacitance, quiescent activity in the grid, pad locations, and pad/package inductance. Simulation results show that the proposed model more accurately determines the current distribution and hence inductive effects, while the traditional simplified loop inductance model significantly overestimates the inductive effects. Further, we have used the PEEC model to study the effects of various model components on signal behavior. We have also proposed a simple partitioning algorithm to reduce run-time and handle larger topologies.

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