Leakage Current Modeling in PD SOI Circuits

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Abstract

In this paper we demonstrate the transient behavior of off-state device leakage due to signal switching history in PD SOI devices. We address the leakage modeling for PD SOI circuits taking input switching history into account and demonstrate that the off-state power dissipation is a function of the device input duty cycle due to body voltage variations with switching history in SOI devices. We also demonstrate that the device off-state power dissipation can be 2.4 times higher than the power dissipation calculated with traditional steady state off-state device current.

1. Introduction

Device and voltage scaling in high performance technologies has resulted in an increase in off-state device currents, [1]. The reduction in threshold voltage, V_t, to maintain device drive current has lead to an increase in leakage current which has become a major contributor to the total power [2]. Various design techniques, e.g. variable device threshold, low leakage standby input vectors, are employed to reduce off-state leakage current because increased system power dissipation can result in performance degradation and failures [3].

In PD-SOI technology, the leakage current components are: subthreshold current, gate leakage current and junction currents [4]. In this paper we only consider the subthreshold current, I_{sub}, and its dynamic behavior with respect to signal switching. Note that the gate leakage current has no impact on body voltage in device "OFF" state [5] and therefore, has no impact on I_{sub} modeling described in this paper. PD-SOI devices have electrically isolated body terminal capacitively coupled to device gate, drain and source terminals as illustrated with the inverter in Fig. 1, which results in threshold voltage variations for the device based on the input and output voltage changes. Plot A in Fig. 1 illustrates the body voltage change as the input pulse duty cycle changes. This threshold voltage variation translates into off state leakage current variation due to subthreshold current dependence on threshold voltage.

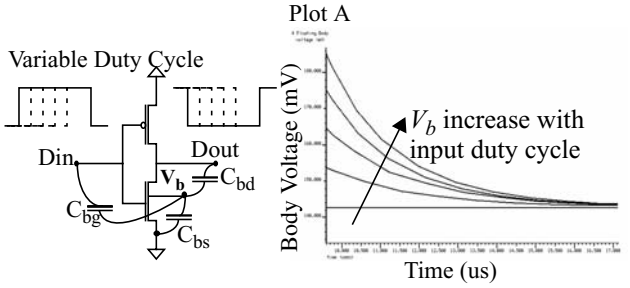

Figure 1. Inverter switching and body voltage variation

The threshold current, I_{sub} is very well defined as a function of technology parameters, gate to source voltage, V_{gs} and threshold voltage, V_t [5]. For PD-SOI, the added complexity of floating body node, i.e. threshold voltage variation based on input switching history has not been modeled. Previous work in PD-SOI has considered switching history impact on delay vs. power trade-off [6] but did not consider the switching history effects on I_{sub} and off-state power. We propose a model for subthreshold current in a PD-SOI device that incorporates the input switching behavior in I_{sub} modeling and derive the power dependence on signal duty cycle. We demonstrate that the power estimation purely based on steady state subthreshold current could be 2.4 times less than the actual power dissipation due to the dependence of threshold current on input switching.

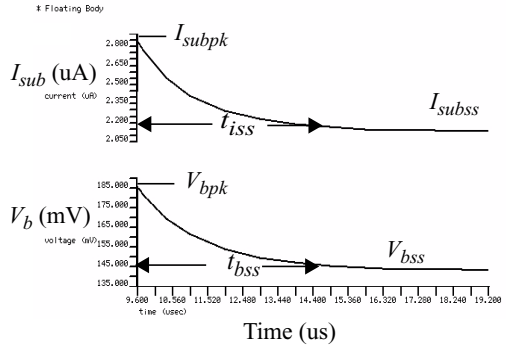

Figure 2. Switching history effect on body voltage and I_{sub}

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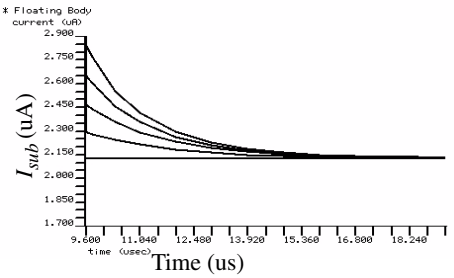

Figure 3. Inverter switching and I_{sub} variation

2. Input Switching History and Subthreshold Leakage

Consider the inverter illustrated in Fig. 1, The floating body terminal of the nfet is capacitive coupled to its drain, source and gate terminals. Any variations in nfet source, drain and gate voltages also changes the body terminal voltage which in turn affects its device threshold voltage and the leakage through it. For a given input pulse the body voltage and the corresponding threshold current through the nfet are plotted in Fig. 2. As shown in the plot, the body voltage converges from a peak value V_{bpk} to its steady state value, V_{bss} over several system cycles called its body settling time, t_{bss}. Similarly, I_{sub} varies exponentially from a peak value, I_{subpk} to eventually settle to the steady state value, I_{subss}, in settling time t_{iss}. Notice that it takes the body voltage longer to settle to its steady state value.

Varying the input pulse width before it switches low, results in a variation in peak body voltage, V_{bpk} for the nfet in the inverter. As shown in Plot A in Fig. 1, each V_b curve corresponds to an input pulse width, the longer the device is in the on-state before turning off, the larger its V_{bpk} when it turns off. Similarly, I_{subpk} variations with input pulse width are shown in Fig. 3.

The subthreshold current peak variation with input pulse width however, is not unlimited. I_{subpk} is an exponential function of the input pulse width as shown in Fig. 4. The x-axis denotes pulse width and the y-axis denotes the corresponding I_{subpk}. Once the input pulse width is equal to t_{bss},

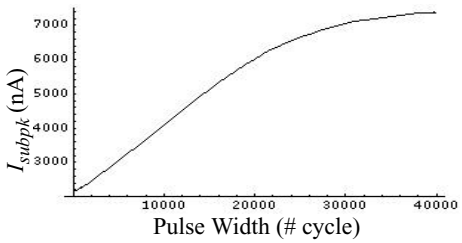

Figure 4. $I_{subpeak}$ variation with input pulse width

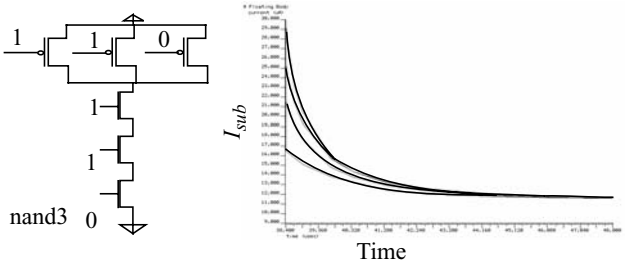

Figure 5. Nand3 nfet stack

the body settling time, I_{subpk} reaches its maximum value and for pulse widths exceeding t_{bss} it is independent of the input pulse width.

It can be shown that the I_{sub} variations with input pulse width is also demonstrated by stacked devices. For a nand3 with 3 stacked nfets, I_{sub} for the stack in worst leakage configuration of only one nfet off, shows input pulse width dependency similar to the inverter case, illustrated in Fig. 5.

3. PD-SOI Leakage Current Model

Leakage current through a PD-SOI circuit, unlike bulk technology is a function of its current and previous input logic states. The off state subthreshold leakage I_{sub} through the device when it turns off has an initial I_{subpk} value which is a function of input pulse width and an exponential decay rate in time which also has pulse width dependence. I_{sub} can therefore, be written in the following form:

$$I_{sub} = I_{ss} + (I_{subpk} - I_{ss}) \cdot f(w) \cdot e^{-g(w,t)} \quad (1)$$

where I_{ss} is the steady state threshold current, w is the duration of signal high state before turning off i.e. pulse width, $f(w)$ is an exponential function of w alone affecting I_{subpk} and $g(w,t)$ is a linear function of time, t and an exponential function of pulse width, w affecting the settling time.

The function $f(w)$ is of the form:

$$f(w) = 1 - e^{-(a \cdot w)} \quad (2)$$

where a is the constant found by curve fitting to the simulated I_{sub} through the device with varied input pulse width, w.

The rate of decay, $g(w,t)$ that is a function of input pulse width, w and time, t is of the form:

$$f(w,t) = b_1 \cdot t + b_2 \cdot t \cdot e^{-w} \quad (3)$$

where b_1 and b_2 are constants determined by curve fitting to simulated I_{sub} data for variable w over its settling time.

I_{sub} is therefore given by:

$$I_{sub} = I_{ss} + (I_{subpk} - I_{ss}) \cdot (1 - e^{-(a \cdot w)}) \cdot e^{-\left(b_1 \cdot t + b_2 \cdot t \cdot e^{-w}\right)} \quad (4)$$

The validity of the model described in (4) can be tested by applying the boundary values for pulse width and time. For,

$$\begin{aligned} w = 0, t = 0 &\Rightarrow I_{sub} = I_{ss} \\ w = 0, t = \infty &\Rightarrow I_{sub} = I_{ss} \\ w = \infty, t = 0 &\Rightarrow I_{sub} = I_{subpk} \\ w = \infty, t = \infty &\Rightarrow I_{sub} = I_{ss} \end{aligned} \quad (5)$$

i.e., the leakage is same as steady state leakage if the device is in off state with no switching history ($w = 0, t = \infty$) and the leakage is at its peak value if the device switches off after being on for a long time ($w = \infty, t = 0$).

For a high performance PD-SOI technology with 45nm gate lengths [7], the calculated and modeled currents are shown in Fig. 6. The plot shows I_{sub} for four different input duty cycles. Simulated vs. model current values within 10% error.

4. Off-State Power Dissipation

The off-state power dissipation for a circuit is a function of its subthreshold leakage current I_{sub}. As already illustrated in Section 3, I_{sub} has a dependence on input duty cycle and the off-state duration and is expressed by (4). The

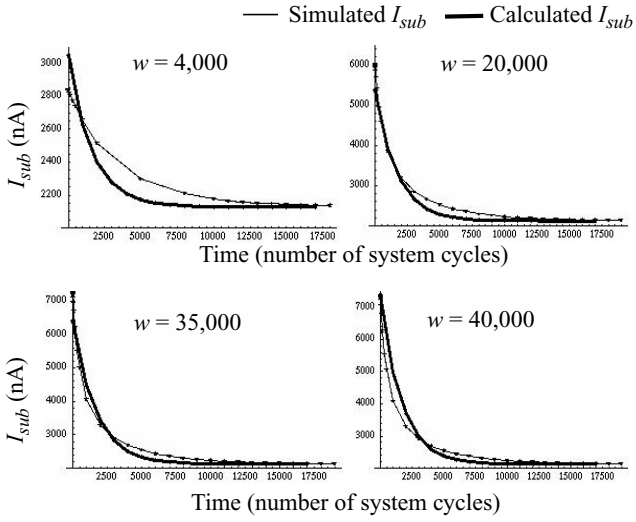

Figure 6. Modeled and simulated I_{sub}

off state average power, P_{off} can be derived from the I_{sub} formula as:

$$P_{off} = \frac{V}{(t_1 - t_0)} \cdot \int_{t_0}^{t_1} (I_{sub} \cdot dt) \quad (6)$$

were V is the operating voltage, t_0 and t_1 the time period for which the device is off. Substituting for I_{sub} from (4) yields:

$$P_{off} = \frac{V}{(t_1 - t_0)} \cdot \int_{t_0}^{t_1} \left(I_{ss} + (I_{subpk} - I_{ss}) \cdot (1 - e^{-(a \cdot w)}) \cdot e^{-\left(b_1 \cdot t + b_2 \cdot t \cdot e^{-w}\right)} \right) dt \quad (7)$$

Therefore, average P_{off} as illustrated with (7), is a function of both input duty cycle and the time for which the device is in off-state. The longer the device is in on-state before switching off, the larger the off-state power dissipation. The longer the device is in off-state the closer P_{off} is to the steady state off-state power, P_{ss}.

If the power dissipated at steady state P_{ss} is expressed as:

$$P_{ss} = V \cdot I_{ss} \quad (8)$$

Increase in off-state power dissipation, ΔP_{off} can be expressed as:

$$\Delta P_{off} = \frac{P_{off} - P_{ss}}{P_{ss}} = \frac{1}{(t_1 - t_0)} \cdot \int_{t_0}^{t_1} \left(\left(\frac{I_{subpk}}{I_{ss}} - 1 \right) (1 - e^{-(a \cdot w)}) \cdot e^{-\left(b_1 \cdot t + b_2 \cdot t \cdot e^{-w}\right)} \right) dt \quad (9)$$

For a high performance PD-SOI technology with 45nm gate lengths, ΔP_{off} is plotted as a function of input duty

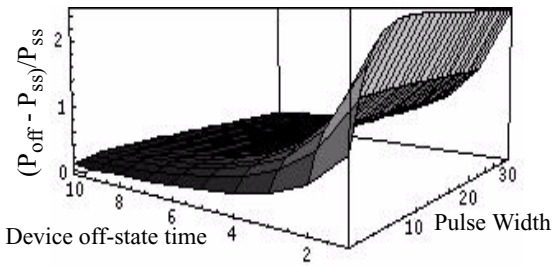

Figure 7. ΔP_{off} variation

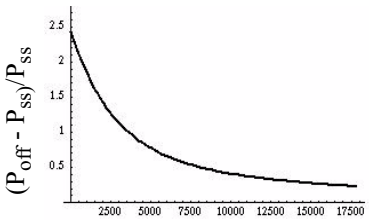

Figure 8. Power increase with off-state time

cycle and off-state duration in Fig. 7. In the plot z-axis is ΔP_{off}, x-axis is the off-state time and y-axis is the input duty cycle. ΔP_{off} increases with pulse width and reduces with increase in off-state duration. It can be 2.4 times the steady state power dissipation for large pulse widths and small off-state durations. This is also demonstrated by the plot in Fig. 8. ΔP_{off} is plotted as a function of device off-state time for a fixed input duty cycle equal to t_{bss}, i.e. maximum signal duty cycle that can affect the $I_{subpeak}$. The plot demonstrates that for a device which has been in on-state for a long time followed by small off-state duration, switching off results in the ΔP_{off} of 2.4 times P_{ss}. Note that as the device continues to be in the off-state, its body voltage and hence, the leakage current and off-state power dissipation gradually converges to steady state values.

5. Input Pulse Train

The switching history of the input to the device could have a stream of pulses as shown in Fig. 9, with pulse widths tp_1, tp_2, tp_3, tp_n. separated by time intervals ts_1, ts_2, ts_n before time t_0 when the device switches off. The leakage current I_{sub} after t_0 is a function of all previous input pulse widths, tp_1, tp_2, tp_3, tp_n, and pulse separations, ts_1, ts_2, ts_3, ts_n. The following algorithm is used to achieve an equivalent single pulse input for computing I_{sub} after time t_0:

1. Pulse train history prior to t_{bss} is ignored.
2. If ts_n is greater than t_{iss}, then the pulse train is truncated at ts_n.
3. If the ts_n is less than t_{iss}, the input is represented by a single pulse with pulse width equal to the sum of weighted pulse widths, tp_1, tp_2, tp_3, etc. given by:

$$w_{eq} = tp_1 + tp_2 \cdot e^{\frac{-t_{iss}}{t_{iss} - ts_1}} + tp_3 \cdot e^{\frac{-t_{iss}}{t_{iss} - ts_2}} + \ldots \quad (10)$$

were t_{iss} is the I_{sub} settling time.

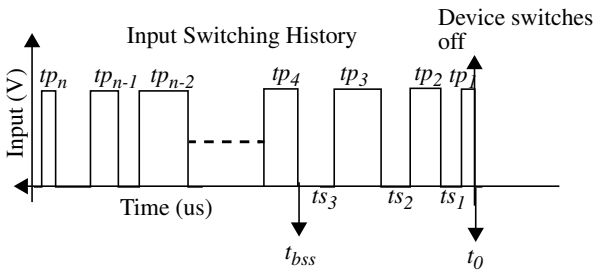

Figure 9. Input pulse stream and I_{sub}

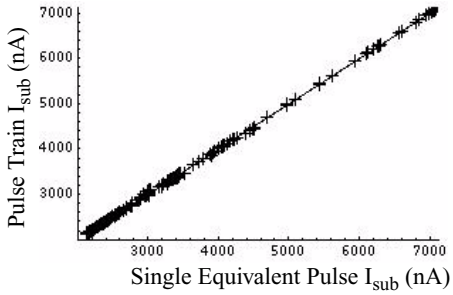

Figure 10. Single pulse approximation

The scatter plot data comparing the data for this approximation is shown in Fig. 10. Each point in the plot represents I_{sub} magnitude at the given time obtained from spice simulation with an input pulse train and the corresponding I_{sub} magnitude obtained with equivalent single pulse input. All measurement points lie very close to the 45 degree line in the plot demonstrating very small variation in the two values.

Once the input pulse train is reduced to a single pulse input, the I_{sub} model developed in the previous section with single pulse width value, can be applied here as well. Similarly, the off-state power expressions can also be used. For a pulse train shown in Fig. 11, the device is assumed to be initially on for a long time, it switches off at t=0, the device is in off state for 100 system cycles, then switches on for 30k system cycles and so on. Note that the on-times are shown as compressed to observe the time varying nature of off-state power in the off-state durations, which are otherwise much smaller than the on-times. For this input pulse, the

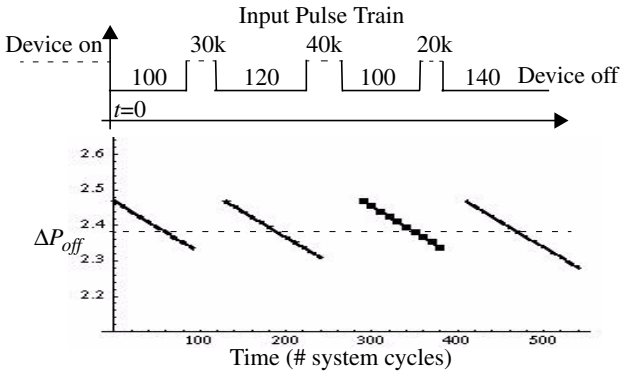

Figure 11. Pulse train power dissipation

ΔP_{off} computed is on an average 2.4 times the steady state power dissipation, in other words the device is 2.4 times more leaky than what steady state values predict.

6. Conclusion

In this paper we demonstrate the dynamic nature of sub-threshold current, I_{sub} for PD-SOI devices. We demonstrated the variation in body voltage, V_b and I_{sub} as a function of input pulse width and device off-state duration. We formulated the I_{sub} variation with input duty cycle and off-state duration and compared it to simulated data illustrating good agreement between the model and device behavior in spice. We extended the formulation to off-state power dissipation and illustrated that the increase in off-state power dissipation is 2.4 times the steady state value. We also account for input pulse train and demonstrate that a device is more leaky due to body voltage variations.

7. References

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