Accurate Gate Delay Model for Arbitrary Waveform Shapes

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Abstract

In this paper we present a new gate delay model for accurate modeling of difficult waveform shapes, such as those resulting from coupling capacitance, inductive ringing, and resistive shielding. Our modeling approach uses a process of *time shifting* and *time stretching* of a set of so-called *base waveforms*. The base waveforms are selected from a large set of generated waveform shapes that occur in interconnect structures such that the delay error across all considered waveforms is minimized. Depending on the desired accuracy, one or more base waveforms can be used. The method is also used to model the output waveforms of gates, allowing for closure in terms of the used base waveforms across a circuit library. We show that the determination of the optimal set of base waveforms under such input to output closure is exponential in complexity. We therefore propose an approach that maps the problem to the unate covering problem, for which efficient heuristics are available. The new delay model can be applied in a timing analysis program with minor changes. We present results that demonstrate the accuracy of the new delay model for a large set of input waveform shapes.

1. Introduction

As clock frequencies continue to increase with process scaling, accurate timing analysis for digital circuits remains a critical concern. A key component in the accuracy of timing analysis is the accuracy of the gate delay model, which models the highly non-linear behavior of CMOS gates. In traditional gate delay modeling a gate is simulated in SPICE with a ramp input waveforms for different input slopes and different capacitive output loadings [1][2]. For each input slope and output loading condition, the delay and output slope obtained from the SPICE simulation is then recorded in a two dimensional delay table. During timing analysis the waveform at the input of a gate is first represented with an equivalent ramp waveform that matches the 20 - 80% Vdd crossing times of the signal. Then, based on the input slope of the ramp and the output load of the gate, the delay of the gate and the slope of the output waveform are obtained from the two-dimensional delay table through linear interpolation.

The advantage of this simple delay modeling approach is that it is very efficient and is easy to implement. The fitting of the ramp to the actual signal input waveform requires only the measurement of two voltage crossing time points and hence the two-dimensional table is relatively small in size. To further reduce the size of the delay model, the 2 dimensional table can be represented as a second order polynomial expression (often referred to as a k-factor equation [3]) that is fit to the table data. In this case, only the parameters of the expression need to be stored for a gate. Extensions have also been developed to model resistive interconnect loading through the computation of an effective loading capacitance, referred to as the so-called Ceff computation [4]. Extensive work in the area of interconnect delay modeling has also been performed to propagate the ramp output waveform at the output of one gate to the input of the next gate through the interconnect [5].

While the simple ramp based input and output waveform approximation has been successfully used for many years, new interconnect effects in nanometer design have significantly increased the error of this gate delay model. An example waveform that is poorly matched by a standard saturated ramp is shown in Figure 1. The noisy waveform is the result of capacitive coupling to a neighboring net. Both waveforms have the same 20-80% transition time and hence are modeled with identical ramp input waveform for delay computation. However, the two waveforms actually result in quite different delays and the delay model incurs a significant error. In addition to this interconnect effect, resistive shielding, inductive ringing, inductive coupling noise and power supply noise all generate input waveforms for which the ramp input delay model incurs considerable error. Hence, it is clear that a new delay model that accurately models the delay of a gate as well as its output waveform under a wide variety of realistic input waveforms shapes is needed.

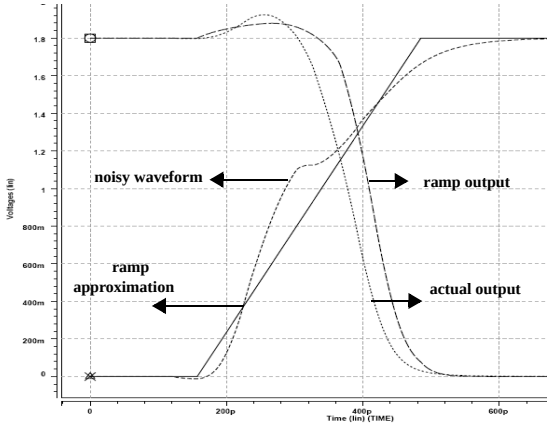

Figure 1. Signal waveforms due to capacitive shielding and coupling noise and their impact on gate delay model accuracy.

A number of methods to improve the traditional delay gate delay model have been proposed. The most obvious approach is to use a transistor level gate model to compute accurate signal waveforms. However, this approach is very slow for large designs. In [6], a new approach is presented where the input ramp is fit to the actual input waveform using a weighted least square fitting approach. This approach has the advantage that it requires only minor changes to the existing method as only the fitting of the input ramp is modified. However, while this approach improves the delay model accuracy, it is limited to signal waveforms that do not deviate substantially from a standard ramp-like waveform in order to maintain good accuracy. Furthermore, no method for modeling the output waveform shape is proposed.

A different approach, presented in [7], uses the shape of a Weibull cumulative distribution function (CDF) to approximate arbitrary gate input waveform shapes. The Weibull CDF is a function of two parameters and can accurately approximate the shape of resistively shielded waveforms. However, in the proposed model the gate delay is characterized for two input waveform parameters as well as the output loading and therefore requires a three-dimensional delay table. This significantly increases the storage requirement and complexity. Also, the Weibull CDF does not fit well for non-monotone waveform shapes induced by capacitive coupling noise or inductive ringing. Finally, in [8], an approach where waveform shapes are analyzed using principle component analysis was proposed. While this approach raises a number of interesting possibilities, the application in [8] is mainly focused on the modeling of the output waveform and the application to gate delay modeling was not discussed.

In this paper, we present a new approach for waveform propaga-

tion through CMOS gates which accurately models a large range of input waveform shapes, such as those resulting from coupling capacitance, inductive ringing, and resistive shielding. We observe that the traditional process of fitting a ramp is in fact one of stretching and shifting a given ramp waveform in the time domain. We model this process as a linear transformation of the ramp waveform using *time shifting* and *time stretching* and then extend this approach to non-ramp input waveforms. We first generate a large number of realistic *candidate* waveforms, W_{Ci}, that can occur at the input of a gate using different interconnect structures. We then select from all candidate waveforms a small subset, W_{Bi}, of *input base* waveforms that are used to approximate the complete set of candidate waveforms using the time shifting and time stretching transformations. Depending on the desired accuracy only a single input base waveform may be necessary or multiple input base waveforms can be used.

Similar to the input waveform, the output waveform of a gate is also approximated using a set of so-called *output base waveforms*, W_{Bo}, selected from a set of output candidate waveforms W_{Co}. For a gate, a two *waveform table* is maintained for each input base-waveform. For all stretch factor *s* of the input base-waveform and for all output loadings the 2-D table stores the identity of the output base waveform and its corresponding time shift and time stretch factors. Note that the time stretch factor *s* is analogous to the traditional slew or slope of signals, except that it is applied to a non-ramp signal. The storage requirement of the waveform table is similar to that of a traditional delay table. The detailed shape of each base waveform is stored only once in the library and its storage cost is therefore amortized. Note that for different input stretch factors and loading conditions, the output can be approximated using different output base waveforms.

During timing analysis, waveforms are propagated as follows: Given an actual waveform at the input of a gate, the time shift t_a and stretch factor *s* that best approximate the actual waveform (using least square error) is computed for all input base waveforms in W_{Bi}. The base waveform with the least error is then selected and, using its 2-D waveform table, the output base waveform is identified along with its required time shift and time stretch factors. The output waveform is then constructed and convolved with the interconnect transfer function, resulting in a waveform at the input of the next gate.

The main additional computation required in the proposed approach is the determination of the time shift, t_a, and stretch factor, *s*, for each base waveform and the selection of the best base-waveform. While this overhead is minor it can be further reduced by selecting the set of the base waveforms to ensure it is closed under propagating waveforms through all gates for all possible loads. In this case, the set of input and output base waveforms is the same and the propagation of any waveform $w_i \in W_B$ through a gate transforms waveform w_i into waveform $w_j \in W_B$ from the same set of base waveforms. As a result, for short output interconnect that does not significantly change the shape of the waveform, the output waveform does not need to be explicitly determined - the identity and time stretch factor of the output base waveform can be directly used to index the correct waveform table of the fanout gates. In this case, the proposed approach will have a runtime efficiency equal to that of the traditional ramp based model and will be independent of the number of base waveforms. For less common long interconnects, that changes the shape of the waveforms, the run time complexity increases linearly with the number of used base waveforms. In all cases the storage requirement is linear with the number of base waveforms.

We show that selecting the minimum set of input and output base waveforms for a given error tolerance has exponential complexity with the number of the candidate waveforms. Hence, we propose an approximate selection approach where the set of input base waveforms is selected first and the set of output base waveforms is restricted to this set. Since the output base waveforms are typically much easier to match, this approach was found to yield high quality results. We then show that input base waveform problem can be cast as a unate covering problem, for which a number of efficient heuristics are available.

We show that even with a single base waveform, the delay accuracy is improved by 52% compared with a ramp delay model. At most 5 waveforms were need to obtain a maximum error in gate delay error of 34ps for cells from an 0.18um industrial library. Finally, the approach adapts well to new and unforeseen waveform shapes. Such new waveform shapes do not require a entirely new modeling approach, but are seamlessly accommodated in the proposed approach by simply adding additional base waveform shapes to the model.

The remainder of the paper is organized as follows. In section 2 we formulate the problem of selecting an optimal set of base waveforms. In Section 3, the signal modeling methodology for static timing analysis is presented in detail. In Section 4, we present our results and in Section 5, we conclude the paper.

2. Problem Formulation

In the traditional gate delay model approach, a ramp input waveform is fit to an actual waveform using two degrees of freedom. The ramp waveform is first shifted in time to match the 50% Vdd crossing time of the actual waveform and the slope of the ramp is then changed to match the delay from the 20% to 80% Vdd crossing time (or 10% to 90% Vdd). As mentioned, we refer to the two fitting parameters as time shifting, denoted by parameter t_a and time stretching parameter, denoted by parameter *s*. It is clear that this same process can be easily extended to arbitrary base waveforms.

We specify a waveform as a vector of *n* time points $T = \{t_1, t_2, t_3, ..., t_n\}$, where time point t_i corresponds to the time that the waveform crosses $\frac{i \cdot Vdd}{n}$. The time points therefore correspond to the crossing times at constant voltage intervals as shown in Figure 2. Note that in this waveform model, voltage is taken as the independent variable and time is expressed as a piece-wise linear function of the voltage. While this is counter to traditional waveform representations in timing analysis where voltage is expressed as a piece wise linear function of time, we found that the proposed representation simplifies the formulation of time shifting and time stretching.

The process of fitting a base waveform *T* to a real waveform is now formulated as the follows:

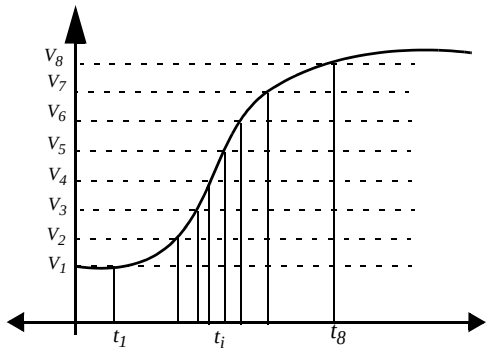

Figure 2. Time as a piece wise linear function of voltage.

Given a base waveform with time point vector T and a fitting objective, find t_a and s such that the waveform $R = t_a + s \cdot T$ minimizes the fitting objective.

In a traditional gate delay model that uses a ramp input, it is clear that the time point vector is simply $t_i = s \cdot i$ and the fitting objective is to match the 50% Vdd crossing time and the 20% to 80% Vdd transition delay of the actual waveform and of R. It should be noted that the work in [6] effectively replaces this simple fitting criteria with a more sophisticated one using a weighted least square error function and shows that this significantly improves the delay model accuracy. In industrial practice, it has been observed that using more realistic waveforms instead of simple ramp improves the accuracy of the waveforms. However, to our knowledge, the selection of such realistic waveforms and their scaling has been performed in an ad hoc manner.

In this paper, we extend the waveform fitting problem, formulated above, to multiple, arbitrary base waveforms in a systematic manner. Allowing for multiple base waveforms raises the question of which base waveforms will most effectively model the large set of actual waveforms that need to be represented for the input and output of a gate. In our approach, we draw this set of base waveforms from the set of actual waveforms themselves, base on the observation that actual waveforms after propagation through a gate resemble each other closely when accounting for time shifting and timing stretching. Given a large set of so-called *candidate* waveforms W_C, which represent the space of possible real waveforms, our task is therefore to select an optimal set of base waveforms W_B, such that the worst-case error of modeling any candidate waveform by one of the base waveforms is minimum. We approach this task using the following formulation:

Formulation 1:

1. Generate a large, comprehensive set of candidate waveforms W_c that represent all possible waveform shapes encounters in a design.
2. For each waveform $w_i \in W_c$, and for each gate G and each load capacitance C, compute propagated waveform $w_{i,out}(G,C)$ and the error of approximating input waveform w_i by $w_j \in W_c$ and its output waveform $w_{j,out}(G,C)$ by $w_k \in W_c$, where w_j and w_k can be arbitrarily shifted and stretched to minimize the approximation error. The error between $w_{out}(G,C)$ and w_k is computed as the maximum deviation in voltage crossing time across all voltages from 20% and 80% of Vdd.
3. Find a minimal set of waveforms W_B such that any input waveform $w_i \in W_c$ and its propagated waveform $w_{i,Prop}(G,C)$ through any gate G and for any load C can be approximated by waveforms $w_j, w_k \in W_B$ with error less than the given value ε.

This formulation can be transformed into discrete by generating a 3 dimensional covering matrix C, such that $C_{i,j,k} = 0$ iff the error of approximating waveform w_i and the result of its propagation $w_{i,Prop}$ with waveforms w_j and w_k, respectively, is more than ε, and $C_{i,j,k} = 1$ otherwise. We then need to find the minimal set of indices N_c corresponding to the selected base waveforms W_B such as for each $1 \le i \le n$ there exists a pair of indices $j, k \in N_c$ such as $C_{i,j,k} = 1$.

It is possible to solve this problem by full enumeration of all the possible solutions of W_B. However, this approach has exponential complexity with respect to the size of the W_B. Alternatively, a possible algorithm based on a greedy approach when we iteratively expand the set of already selected indices with the index resulting in highest coverage could be used. However, these approaches all need to process a very large 3D matrix, the generation of which itself could be infeasible. We therefore propose a different approximate approach to solve this problem by decomposing it into two simpler problems. This approach is based on the observation that output waveforms of gates are much easier to model since the typically represent smooth transitions then input waveforms that can be strongly affected by noise.

1. The first problem is to select a set of waveforms W_{Bi} approximating input waveforms so that the propagated waveform of the original waveform w and its approximation $w_a \in W_{Bi}$ results in error less than the required value e. (The error e is again computed as the maximum deviation in voltage crossing time across all voltages from 20% and 80% of Vdd for the actual and approximate waveforms).
2. The second problem is to approximate the waveforms W_{out} resulted from propagation of the selected waveforms W_{Bi} with some of the selected waveforms W_{Bi}.

Now show that the first problem can be formulated as the unite covering problem. We approach this task using the following formulation:

Formulation 2:

1. Generate a large, comprehensive set of candidate waveforms W_C that represent all possible waveform shapes encounters in a design.
2. Compute a so-called *error matrix E*, where each entry $E_{i,j}$ is the error of approximating the propagated waveform $w_{j,Prop}$ by the propagated approximate waveform $R = t_a + s \cdot w_i$, shifted by time t_a and stretched by factor s where t_a and s are obtained using a fitting criteria.
3. Given a maximum allowed delay error ε, generate the covering matrix C, such that $C_{i,j} = 0$ iff $E_{i,j} > \varepsilon$, and $C_{i,j} = 1$ iff $E_{i,j} \le \varepsilon$.
4. Find the minimum size set of rows, $B = \{b_1, b_2, ..., b_i, ...\}$ (corresponding to the selected base waveforms W_B) such that for each column j (corresponding to the candidate waveforms) at least one entry $C_{i,j} = 1$.

It is clear that step 4 corresponds to the unate covering problem and can be solved using a number of efficient heuristics. In our approach, the fitting criteria in step 2 uses a modified least square error objective which was found to be effective. However, any suitable fitting objective function can be used.

It is important to note that the error matrix E is based on the deviation of the propagated base waveform to the propagated actual waveform in step 2. After propagation through a gate, two very different waveform can become very similar due to the low-pass filtering properties of a gate. Therefore, this approach not only increases the accuracy of the computed error, but also reduces the number of needed base waveforms. The error between the actual propagated waveform and the propagated fitted base waveform is computed by taking the maximum error of their voltage crossing times for voltages between 20 to 80% Vdd. This objective therefore not only guarantees a good approximation of the signal delay (the 50% Vdd crossing time), but also of the waveform shape as a whole.

The error matrix is a function of the gate response to a candidate waveform and its fitted base waveform. Hence, the identified set of base waveforms for a particular error threshold ε will depend on the gate type, the gate size and the output loading. Hence, for each gate

and output loading, a different set of base waveforms can be selected. While this provides the highest accuracy with the least number of base waveforms, it complicates the timing analysis to some extend. Therefore, we also investigate the number of required base waveforms to meet the required error threshold if a single set of base waveforms is used for all loading conditions. Using Formulation 2, this can be accomplished by computing the maximum approximation error across all loading conditions due to selection of each waveform as a base waveform in step 2. Similarly, a single set of base waveforms can be determined for all gates and all loading conditions in a library. In this case, a single set of base waveforms is obtained for the entire library.

The second problem of approximating the output waveforms can be efficiently solved (in quadratic time) by simply computing the error due to approximating each propagated waveform by each waveform from $W_{B,in}$ shifted by time t_a and stretched by factor s. We then select the best approximation. Taking into account that the number of the selected base waveforms is not very large, this computation can be done very efficiently. Therefore we will not consider here the details of solving this problem. It is clear that if we selected a good representative set of base waveforms W_B, the output waveforms can be approximated with W_B with good accuracy.

3. Signal Model for Arbitrary Waveform Shapes

In this section, we discuss the steps in Section 2 in more detail as well as how to perform timing analysis using multiple base waveforms.

3.1 Generating candidate waveforms

As mentioned earlier, in the proposed approach, we select a few base waveforms from a large pool of generated candidate waveforms such that the error of the delay model is bounded. These candidate waveforms must give a comprehensive representation of all possible waveforms that can be accounted for during actual operation. Note that including more waveforms in the candidate set only improves the accuracy of the delay model since it provides a larger set from which to draw the base waveforms. Hence, it is better to include more waveforms in the candidate set than fewer. While increasing the number of the candidate waveforms increases the run time for the error and cover matrix generation and the unate covering problem, these steps are only performed once during the generation of the delay model and their run time is amortized over numerous runs of the timing analysis itself.

In this paper, the candidate waveform set was generated by varying the parameters of a typical interconnect structure as shown in Figure 3 and recording the waveforms at node *A.* The interconnect model values of coupling capacitances, ground capacitance, shielding resistance, relative transition time overlap between the aggressor and victim net, input slopes and driver strength at the aggressor nodes

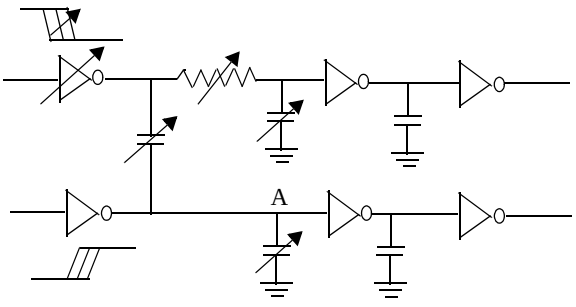

Figure 3. Interconnect structure to generate candidate waveforms

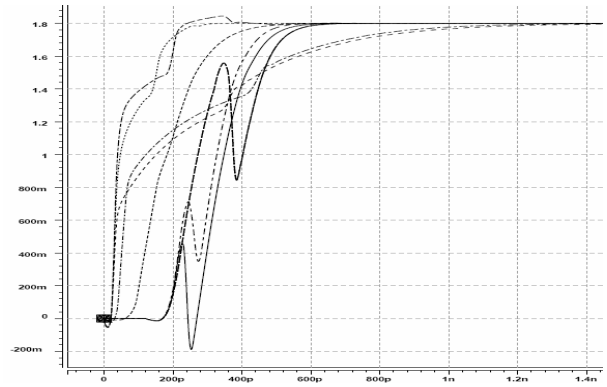

Figure 4. Sample waveforms generated using the circuit in Figure 3

were all swept over their possible range of values, thus generating a large pool of diverse waveforms. Some of the waveforms generated using this setup are shown in Figure 4. Using a wide range of circuit parameters, it is possible to get a comprehensive set of candidate waveforms that provide a good representation of the set of possible actual waveforms encountered during timing analysis. Similarly, we have included inductive noise effects and their impact on the waveform shape in the set of candidate waveforms.

3.2 Creating the error and covering matrices

Based on the set of candidate waveforms, the error and cover matrices are generated. An entry in error matrix $E[i,j]$ is computed as the maximum of the deviations of the propagated j-th output waveform from a shifted and scaled version of the i-th waveform after propagation. It is clear that the entries on the diagonal of E, $E[i,i]$ $i<n$, are always zero. For the sake of illustration, a small error matrix with three candidate waveforms is shown below in Figure 5. Entry $E[1,2]$ is the maximum of squared deviations at the output of the modeled gate when a shifted and scaled version of waveform 2 are applied to the input of the gate instead of waveform 1 for voltage crossing times between 20% and 80% of Vdd.

For a pool of n generated waveforms $n(n\text{-}1)$ SPICE simulations combined with $n(n\text{-}1)$ shifting and scaling co-efficients are computed. However the cost of creating the error matrix is incurred only once while designing a new standard cell library or migrating to a new technology, and thus can be amortized over a large number of digital designs using this new standard cell library or new technology.

Based on a given maximum error ε and the error matrix E, a covering matrix C is be computed as given by the expression in step 3 in Formulation 2. The cover matrix corresponding to the sample error matrix in Figure 5 is shown in Figure 6, when an error threshold $\varepsilon =$ 4ps is used.

The task of selecting a set of base waveforms from a pool of candidate waveforms given a desired maximum allowed error ε is equivalent to the a unite covering problem [9]. The rows of this covering matrix can thought to be the constraints which are to be satisfied by the column of this covering matrix. In other words every waveform in

	1	2	3
1	0ps	5ps	4ps
2	8ps	0ps	7ps
3	4ps	6ps	0ps

Figure 5. Sample error matrix for three candidate waveforms

	1	2	3
1	1	0	1
2	0	1	0
3	1	0	1

Figure 6. Example covering matrix, corresponding to the error matrix in Figure 5

the set of waveforms is a candidate base waveform and at the very same time, the selected base waveforms should accurately model every candidate waveform within desired error if shifted and stretched in time. It is clear that as the maximum allowed waveform approximation error ε decreases, the number of base waveforms increases.

3.3 Timing analysis using multiple base waveforms

Using the proposed approach, each gate G is associated with its waveform table $T_{Prop,G}$ describing how the input waveforms are transformed into output waveforms. The waveform table specifies the type of the output base waveform, time shift (gate delay) and time stretch factor (waveform length). Alternatively, the gate delay and scale factor can be expressed using a k-factor expression which records the delay of the gate for different gate output loadings and time stretch factors *s*. During timing analysis we simply propagate base waveforms through gates similarly to propagation of ramp signals. During this propagation we compute arrival times by accumulating gate delays (time shifts) and calculate stretch factors similarly to computing slews in traditional timing analysis. The only difference with traditional timing analysis is the fact that during propagation waveforms can change in type. However if we use only one waveform type there is no difference at all. If we need to propagate signals though interconnects we compute the actual signal waveform at the output of the interconnect by using convolution of the input signal with the transfer function of the interconnect. We then fit the resulting waveform to one of the base type waveforms, selecting its type, time shift and time stretch factor minimizing the sum of squared deviations. The cost of fitting is generally much less that the cost of signal convolution used for interconnect simulation. Therefore, its effect on total computation time is not significant.

4. Results

The proposed gate delay model was implemented and tested using a set waveforms that exhibit significant coupling noise. The candidate waveforms were generated using the interconnect circuit shown in Figure 3 as well as a similar inductive circuit. As shown in Figure 4, the waveforms are not necessarily monotonic and hence present a challenging test for conventional gate delay modeling. The number of candidate waveforms was 381. In addition, we also generated a more extensive set of 2781 waveforms to test the accuracy of the proposed gate delay model.

The candidate waveforms were first applied on to an inverter in 0.18µm technology to create an error matrix with three different load capacitances of 2fF, 5fF and 10fF. These three error matrices corresponding to low, medium and high loading formed the basis of various cover matrices corresponding to different desired maximum allowable error.

In Figure 7 the number of required base waveforms vs. the gate delay error ε is shown for 10fF, 5fF and 2fF loading capacitance when

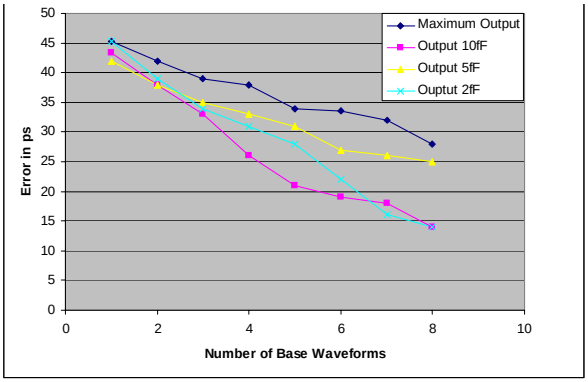

Figure 7. Obtained trade-off between delay model error and number of base waveforms for three loading and across all

approximating the input waveform of a gate. The maximum gate delay error is also shown when a single set of base waveforms is used for all loading conditions (*maximum output*). The graph shows the expected behavior that as the maximum allowable error is decreased, the number of required base waveforms increases. In Table 1, the results of the proposed waveform modeling are compared with that using a saturated input ramp. Two approaches for matching the input ramp are shown. The column *10 - 90%* uses the traditional method of matching 10 - 90% slope. The column *least square fit* uses a least square fitting approach similar to that used for fitting the base waveforms in the proposed approach. The table shows that even by using one base wave form, the error in the gate delay can be reduced from 93ps in the traditional approach to approximately 44ps in the proposed approach, which is an improvement of 52%. If the more sophisticated least square fitting approach was used with the ramp input, the error reduces from 64ps to 44ps, which is an improvement of 31%. Note that in the latter case, the two approaches have the same computational cost for STA and differ only in their used base waveforms. The error in the proposed approach using a single set of base waveforms for all loading conditions reduced to 38ps for 2 base waveforms and 34ps for 5 base waveforms, after which the improvement diminished. Hence, even a small number of judiciously chosen base waveforms can result in significant error improvement. The base waveforms selected by the proposed approach when four waveforms are used are shown in Figure 8.

Table 2 shows the results for Nand, Nor, And and Or gates compared with the results from the inverter in Table 1. The results when using a single set of base waveforms across all gates is again given in the last row. The error for the proposed approach are approximately the same as that for the inverter case. However, the traditional ramp based approach has a higher error, resulting in a error improvement of

Table 1. Results for the Input Waveform Matching for Inverter

Output Cap	Ramp Waveform		Proposed Approach		
	Least square fit	10 - 90% fit	Single W-form	Two W-form	Five W-form
10fF	64.4ps	93.3ps	43.3ps	38ps	21ps
5fF	59.3ps	91.6ps	42ps	37.5ps	31ps
2fF	64.4ps	90.6ps	44.6ps	37ps	28ps
Max across loading	64.4ps	93.3ps	44.6ps	38.ps	34ps

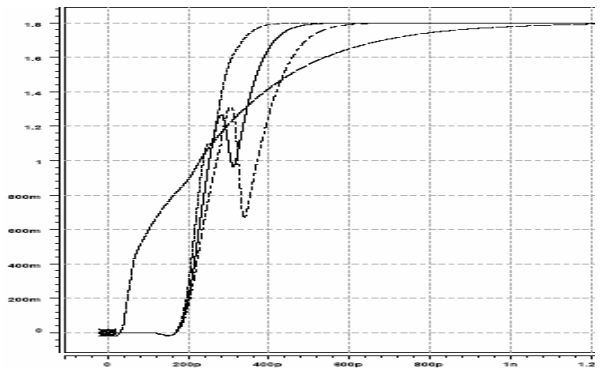

Figure 8. Base waveforms shapes selected by the proposed waveform modeling approach.

60% (from 108ps to 43ps).

In Table 3, we show the results for *output* waveform modeling for the 5 different gate types. To enforce closure, the set of base waveforms is taken to be the same as the base waveforms used in Table 2 for the input waveform modeling. The table again shows the results when the base waveforms are restricted to individual gates as well as when a single set of base waveforms is selected for all gates. As expected, the results show that the error in modeling the output waveforms is less than that for modeling the input waveforms, despite of the fact that the base waveforms for the output modeling are already predetermined.

In order to verify the correctness of our approach as many as 2781 new test waveforms were generated using an interconnect model similar to one described in the Section 3. These waveforms were then applied to the inverter gate and its output response was recorded using SPICE simulation. The inverter was also characterized with respect to a base waveform set identified previously.

The gate delay obtained using the characterization look up table using both input and output waveform modeling was then compared those measured using SPICE for all 2781 test waveforms to verify the correctness of the predicted delay. The error profile comparing the spice results with the delay computed using the characterization tables is as shown in Figure 9. A single base waveform was used in this case. The error predicted using the proposed approach was 43.4ps, while the actual maximum error measure using the test waveforms with SPICE was 44.4ps, showing a good match.

5. Conclusion

In this paper, we have presented a new delay model that accurately models waveform shapes that have traditionally been difficult to model with a simple ramp approximation, such as those due to capacitive coupling, inductive coupling and resistive shielding. Our approach is based on the generation of a large set of *candidate* waveforms from which a small set of so-called *base waveforms* is selected. The selected base waveforms are then fit using time shifting and time stretching to actual waveforms at both the input and output of a gate. We show that the problem of finding the minimum number of base waveforms needed to guarantee a particular delay model error threshold can be mapped to the unate covering problem. We demonstrated our delay model approach for a large set of capacitively coupled signal transitions and show that the delay error can be significantly reduced with only two or three base waveform shapes.

Table 2. Results for the Input Waveform Matching for different gates (10fF output loading).

Gate Type	Ramp Waveforms		Proposed Approach		
	Least Square Fit	10% to 90% fit	Single Wform	Two Wform	Five Wform
NAND	59.8ps	85.1ps	41ps	33ps	22ps
NOR	57.2ps	79.8ps	37.9ps	31ps	23ps
AND	56.7ps	108.2ps	33.9ps	21ps	7ps
OR	55.9ps	106.6ps	33ps	27ps	8ps
Inverter	64.4ps	93.3ps	43.3ps	38ps	21ps
Max. across gates	64.4ps	108.2ps	43.3ps	39ps	34ps

Table 3. Error in output waveform modeling using base waveforms from inputs modeling to enforce closure. (10fF output loading).

Gate	One Waveform	Two Waveform	Five Waveforms
AND Gate	20.3ps	13.4ps	9.1ps
OR Gate	21.4ps	13.7ps	8.9ps
NOR Gate	21.1ps	14.1ps	9.4ps
NAND Gate	22.3ps	13.9ps	9.2ps
Inverter	25.1ps	15.2ps	9.7ps
Maximum across gates	25.8ps	15.5ps	10.1ps

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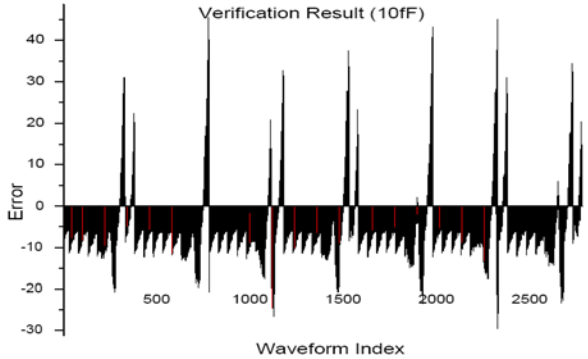

Figure 9. Delay model error when tested with 3500 test waveforms.