

# An Active Decoupling Capacitance Circuit for Inductive Noise Suppression in Power Supply Networks

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## Abstract

The placement of on-die decoupling capacitors (decap) between the power and ground supply grids has become a common practice in high performance processor designs. In this paper, we present a new *active* decap circuit that significantly increase the effectiveness of decap in suppressing power supply fluctuations. The proposed circuit senses the supply drop and drives an amplified and inverted voltage fluctuation on the decap. The active decoupling circuit is powered by a separate power supply and we study the optimal allocation of the total C4s/pads between this second power supply and the regular supply as well as the optimal allocation of the total decoupling capacitance between actively switched and traditional static decap. Finally, we demonstrate that the overhead of the proposed method is small compared to the area of the decaps. Using the proposed method, the maximum supply drop is reduced by 45% compared to the use of only traditional decap, corresponding to an increase in the effective decap of approximately 8X.

## 1 Introduction

Power supply integrity is of critical concern in high performance processor designs. Noise in the power supply network is caused by interconnect parasitics and can incur a performance penalty or can even compromise the functional stability of the design. Power supply noise is broadly classified into two categories. The supply drop (or ground bounce) caused by the resistivity of the power distribution network is referred to as IR-drop, while the supply noise resulting from the inductive parasitics of the network is commonly known as Ldi/dt-drop. With technology scaling, increasing power consumption and clock frequencies have significantly exacerbated the Ldi/dt-drop, such that it is now considered the dominant portion of the overall supply drop in high performance designs [1, 13]. Also, the IR-drop problem is addressed effectively by increasing on-chip power grid metallization whereas such techniques are less effective in reducing Ldi/dt-drop as it is primarily caused by package inductance. This has given rise to an urgent need for the mitigation of inductive noise in power distribution networks in the presence of large transient switching currents.

Decoupling capacitance between the power and ground distribution networks, commonly referred to as *decap*, provides a local charge storage which is effective in reducing the voltage drop in the presence of rapid current transients. Decap occurs naturally in the power distribution network due to parasitic capacitance between the metal lines of the grid, device capacitance of the non-switching transistors and the N-Well substrate capacitance. However, the amount of this naturally occurring decap (referred to as *implicit* decap) is typically not sufficient to meet the stringent power supply integrity constraints of high performance designs. Hence, designers often add substantial amounts of *explicit* decoupling capacitance on the die at various strategic locations.

Gate capacitance of *n* or *p* type devices is normally used to construct explicit decaps in the power grid. However, these explicit decaps result in area overhead and hence directly increases the cost

of the chip. In addition, explicit decaps increase the leakage power consumption of the chip due to their gate leakage current. With technology scaling, gate leakage has become a significant percentage of the overall leakage which places a significant limitation on the maximum amount of decap that can be introduced [2]. Recently, on-die metal-insulator-metal (MIM) decoupling capacitors have been suggested in [3] to reduce the area overhead and leakage of on-die decaps. However, MIM decaps require extra processing steps. The goal of the designer is therefore to meet the desired performance and signal integrity constraints with the least possible total amount of explicitly added decaps [4 - 7]. We refer to these explicit decaps as *passive* decaps.

Active decaps [8 - 11] employ a circuit to increase the amount of charge transfer to-and-from the power supply network during a supply voltage fluctuation. The objective of these approaches is to obtain a smaller supply drop for the same amount of explicit decoupling capacitance. Active guard ring circuits, based on the use of active decaps, were proposed in [8] and [9] to suppress substrate noise. In [10], an active decap technique was proposed to reduce crosstalk between digital and analog regions on a die. A switched-capacitor based circuit technique for generating active decaps was proposed in [11]. In [12], the use of controlled incremental frequency changes to alleviate inductive noise in dynamically voltage scaled microprocessors is explored.

In this paper, we propose a novel active decap circuit to suppress Ldi/dt noise in power supply networks. The proposed active decap circuit is powered from a separate supply network (referred to as the *active* supply) and the existing power supply pads/C4s are split between the regular supply network and the active supply network. The proposed decap circuit senses and amplifies the voltage drop in the power and ground lines of the regular supply network. This amplified and inverted voltage drop is then placed on one of the terminals of the active decap, allowing it to pump significantly more charge into the regular power grid (or absorb more charge from the ground grid) as compared to passive decaps. We study the trade-offs in the allocation of the total number of pads/C4's allocated between the regular supply network and the active supply network.

Finally, we show that the area overhead of the amplifier is small compared to the area consumed by the decaps themselves. Also, since the active supply network is dedicated only to the active decap circuits, it does not require an extensive power distribution network and hence does not lead to a significant supply grid overhead. Simulation results show that it can effectively improve the frequency response of the power distribution network. The transient voltage drop was shown to reduce by 45% compared to the use of only passive decaps, corresponding to an increase in the effective decap of approximately 8X.

The rest of the paper is organized as follows. Section 2 explains the proposed circuit in detail. Practical considerations in implementing of the proposed circuit are presented in Section 3. Section 4 presents the experimental validation of the circuit and conclusions are drawn in Section 5.

## 2 Proposed Active Decap Circuit

This section presents the proposed active decap circuit and compares its performance to passive decap. We first present the analysis of a power delivery model with passive decaps in Section 2.1. The proposed active circuit is then presented in Section 2.2 and compared with passive decaps in Section 2.3.

### 2.1 Power Delivery with Passive Decap

Figure 1 shows a commonly used model of a power distribution network with on-die passive decaps represented by  $C_d$ . The lumped inductors  $L_{Vdd}$  and  $L_{Vss}$  model the inductance attributed to the power supply network in the motherboard, socket, package and on-die inductance, whereas resistors  $R_{Vdd}$  and  $R_{Vss}$  represent the resistive parasitics in the supply network.  $I_{die}$  is the current drawn from the supply network by the on-die devices. In addition to the on-die decaps, discrete decaps are also placed at various locations (VRM decap, motherboard decap and package decap) in a power distribution network. The resonance frequencies due to these additional decaps are considerably lower [13] ( $\sim$ kHz-5MHz) as compared to the resonance frequency due to package inductance and on-die decaps ( $\sim$ 100MHz). Extra board and package decaps can be added with relative ease but such is not the case with on-die decaps due to the leakage and area constraints. Hence, in our analysis, we concentrate only on the effectiveness of on-die decaps.

Let  $\Delta V(t)$  be the transient voltage drop (ground bounce) seen by the devices on-die due to time-varying current  $I(t)$ . The decap  $C_d$  observes a net change in potential of  $2\Delta V(t)$  across its two terminals and provides a charge of  $2C_d\Delta V(t)$  to both the power and ground lines. The current,  $I_{Cd}(t)$ , provided by the decaps to the on-die devices is therefore given by:

$$I_{Cd}(t) = 2C_d \cdot \frac{d}{dt}\Delta V(t) \quad (1)$$

The DC part of on-die current  $I(t)$ , along with the rest of transient current ( $I_{pkg}(t)$ ) is supplied by the VRM through the inductors  $L_{Vdd}$  and  $L_{Vss}$  is:

$$I_{pkg}(t) = I(t) - I_{Cd}(t) \quad (2)$$

The current provided by the VRM,  $I_{pkg}(t)$ , causes the drop in the power supply  $\Delta V(t)$  as follows:

$$\Delta V(t) = I_{pkg}(t)R + L \frac{d}{dt}I_{pkg}(t) \quad (3)$$

It can be observed that the voltage drop decreases as the amount of on-die decaps is increased. The resonance frequency,  $\omega_r$ , due to the interaction of package inductance with on-die decaps is given by:

$$\omega_r = \frac{1}{\sqrt{L_{pkg}C_d}} \quad (4)$$

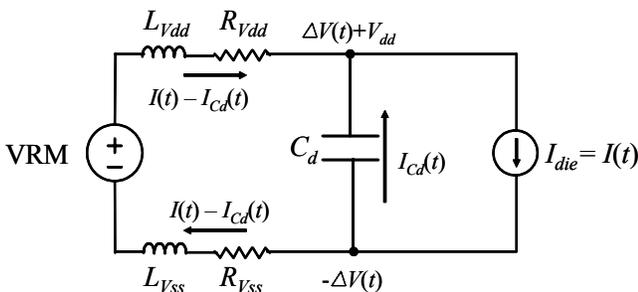


Figure 1. Model of a power supply network.

where  $L_{pkg}$  is the net inductance of the supply network ( $L_{Vdd}+L_{Vss}$  in Figure 1). As the amount of on-die decaps increases, the resonance frequency as well as peak  $Ldi/dt$  noise are lowered. The goal is, therefore, to maximize the total amount of decap  $C_d$  within the area and leakage constraints, thus minimizing both IR as well as  $Ldi/dt$  drop in the network. In the next subsection, we present the proposed active decap circuit and compare it with passive decap.

### 2.2 Active Decap Circuit

The proposed active decap circuit consists of two operational amplifiers (*opamps*) which amplify and invert the voltage drop across the power and ground lines of the supply network. The total available passive decap is divided evenly among the power and ground networks. The two opamps drive one terminal of each decap as shown in Figure 2. The opamps operate with a separate, so called *active*, supply and hence, the total number of C4s available for power delivery in the chip is divided between the active and the regular supply. For simplicity in our discussion in this section, we assume that the active supply is ideal and does not affect the gain or the current drive of the opamps. However, later in Section 4.3, we will study what percentage of the total available C4s should be dedicated to the active supply versus the regular power grid. We find that only a small percentage of the total C4s need to be allocated to the active supply and that the non-ideality of the active supply has only minor impact on the effectiveness of the technique.

We now compute the theoretical effectiveness of the proposed method. The transient voltage drop (ground bounce),  $\Delta V(t)$ , is amplified to a potential of  $-2A\Delta V(t)$  and  $2A\Delta V(t)$ , respectively, by the two amplifiers driving the  $Vdd$  and  $Vss$  decaps. As a result, each of the two decaps observes a difference in potential of  $(2A+1)\Delta V(t)$  across its terminals. Thus, the current  $I_{Cd}(t)$ , provided by the decaps to the devices is given by:

$$I_{Cd}(t) = (2A+1) \frac{C_d}{2} \cdot \frac{d}{dt}\Delta V(t) \quad (5)$$

As compared to (1), the current provided by the active decaps is therefore considerably higher if the gain  $A$  of opamp is sufficiently high. In general, for the same on-die current,  $I(t)$ , and same amount of decap,  $C_d$ , the active decap will lead to a lesser voltage drop,  $\Delta V(t)$ , provided the following condition holds:

$$(2A+1) \frac{C_d}{2} \cdot \frac{d}{dt}\Delta V(t) \geq 2C_d \cdot \frac{d}{dt}\Delta V(t) \quad (6)$$

or,  $A \geq 1.5$

If the gain of the opamp is greater than 1.5, a better power supply regulation can be achieved or the amount of decap can be reduced

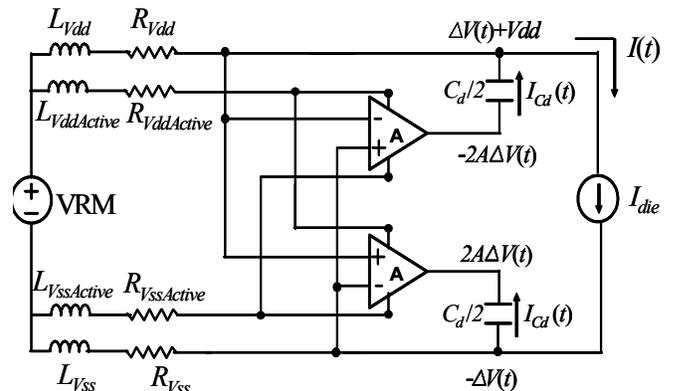


Figure 2. Proposed active decoupling capacitance circuit.

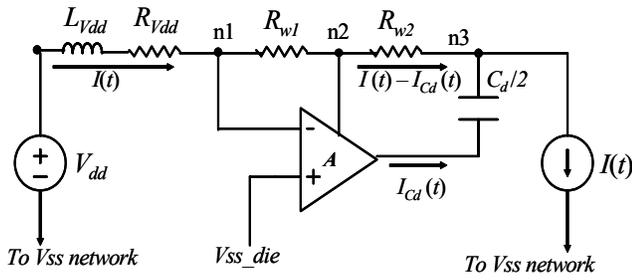


Figure 3. Need for external active supply to operational amplifiers.

for the same supply regulation. The *effective* decoupling capacitance achieved using this active circuit is:

$$C_{eff} = (2A + 1) \frac{C_d}{2} \quad (7)$$

where,  $C_d$  is the amount of decap present in the chip driven by the opamps and  $A$  is the gain of opamps. In practical implementation, the gain  $A$  is a function of frequency and decreases as frequency of operation is increased, and will be discussed later in Section 3.

It should be noted that the opamps in the active circuit must operate with an external active power supply and cannot be connected to the regular on-die power supply. Figure 3 explains why the active circuit cannot operate if its supply rails are connected to the same power supplies which provide current to the other on-die devices. Let  $I(t)$  be the current consumed by the chip and  $I_{Cd}(t)$  be the current provided by decap  $C_d$ . Then, the current flowing in the resistance  $R_{w2}$  is  $I(t) - I_{Cd}(t)$ . On the other hand, the current flowing in the package remains  $I(t)$  as shown in the figure. Thus, the only improvement in supply drop is in the IR-drop due to a reduced current now flowing through the resistor  $R_{w2}$ . The package inductance  $L_{pkg}$  has full on-chip current flowing across it, resulting in a worse inductive effect as compared to the use of passive decaps.

While separate active supply rails are needed in the proposed method, we show in Section 4.3 that only a small portion of the total C4s need to be allocated to the active supply. Furthermore, since the active supply is only connected to the active decap circuits, a full supply grid design is not needed for the active supply. Instead, C4s in the immediate vicinity of the active decap circuits can be directly routed to the circuits, thereby minimizing the routing overhead incurred by the additional supply.

### 2.3 Comparison of active and passive decaps

This subsection explains and compares the response of active decap circuit with that of passive decap, assuming ideal opamps.

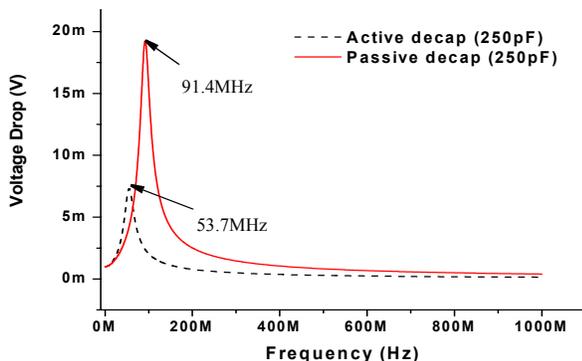
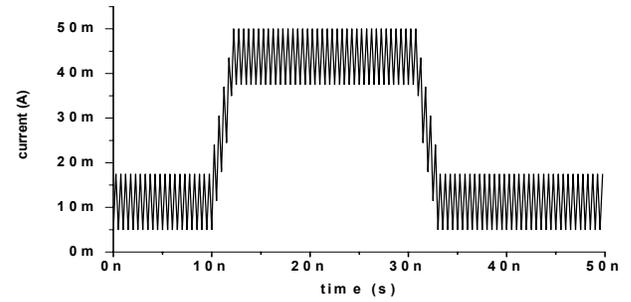
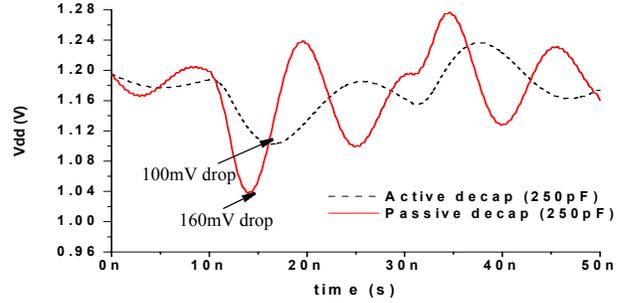


Figure 4. Frequency response of power delivery network with passive and active decaps.



(a)



(b)

Figure 5. Transient current profile (a) and voltage response (b).

The practical design constraints and opamp design are presented in Section 3.

Figure 4 compares the frequency response of the power supply network with passive decaps and active decaps. The HSPICE simulations were performed in 130nm triple-well technology with nominal supply of 1.2V. The capacitive and inductive parasitics were based on an industrial power supply grid for a high performance processor design. The simulated circuit represents a 0.7mm x 0.7mm section of the die since it is not possible to simulate a detailed model of the entire supply network. However, since the active decap circuit can be replicated across the die, the results for the whole die are similar. The capacitive and inductive parasitics were obtained using an industrial supply extracted

The total amount of decap available,  $C_d$ , (passive and active combined), was 250pF. The gain  $A$  of the ideal opamps was set to be 5 which results in an effective capacitance of  $3C_d$  using equation (7). As a result, the resonance frequency was reduced by a factor of  $\sqrt{3}$ . The resonance frequency of the grid due to package inductance with passive on-die decaps was observed to be 91.4MHz. The use of active decaps reduced the resonance frequency to 53.7MHz. Moreover, use of active decaps also led to a significant reduction in peak noise at the resonant frequency as shown in Figure 4.

Figure 5b shows the transient response of the power grid with active and passive decaps to the current profile shown in Figure 5a. The current pattern was modeled on a high performance microprocessor switching from a state of low activity operations to a state of high activity operations in 5 clock cycles and back. The processor is first in a state of low power instructions consuming 10% to 30% of its peak power. The state of the processor is then ramped from this low power mode to a high power mode in 5 clock cycles, resulting in current levels oscillating between 75% to 100%. Finally, the processor is ramped down to the low power mode again. The operating clock frequency was assumed to be 4GHz. With an opamp gain of 5, the worst-case supply drop was reduced from 160mV to 100mV, resulting in a percentage improvement of 37.5% as shown in Figure

5b. It is clear that higher reduction in supply drop can be obtained by increasing the gain of the opamp.

The results in Figure 4 and Figure 5 demonstrate the effectiveness of the proposed circuit with ideal opamps, in the presence of large current transients. The next section presents the opamp design and other practical considerations in the silicon implementation of the proposed approach.

### 3 Opamp Design

The last section described the proposed circuit with ideal opamps having fixed gain, infinite input impedance and zero output impedance. In reality, the gain of an operational amplifier is a function of operating frequency and drops as frequency is increased. Hence the net effective capacitance given in (7) decreases with increasing frequency. In order to reduce the impedance of a power supply network at the resonance frequency, the gain of the amplifier should be as high as possible. On the other hand, the bandwidth of the opamp should be high enough to suppress high frequency inductive noise as well. These are contradicting requirements since the gain-bandwidth product is usually near-constant in a given technology. In all, the opamp used in the active circuit should have the following characteristics:

1. High gain at the resonance frequency for suppressing the dominant voltage fluctuations and resonance effects.
2. High bandwidth for mitigating high frequency inductive noise.
3. High current drive in order to drive large decaps.
4. Small amplification delay for fast reaction to high frequency current transients.
5. Robustness of opamp to its own active power supply variations.

The opamp used in the proposed active circuit consists of three stages. The inputs to the opamp have common-mode voltages of  $V_{dd}$  and  $V_{ss}$ . This entails the use of level shifters as the first stage of the opamp, so as to bring the inputs to their common-mode bias levels for the gain stage. The gain stage forms the second stage of the opamp. For improving the output impedance and current drive, a high drive strength output stage is used after the gain stage.

Figure 6 shows the circuit schematic of the opamp, which amplifies the difference between  $V_{dd}$  and  $V_{ss}$  supply drops and applies it to a terminal of the decap connected to  $V_{dd}$  grid. The bias generation circuitry is not shown for clarity. As mentioned in Section 2.2, the opamp needs to operate using an active supply different from the main power supply of the other devices on die. All the bias sup-

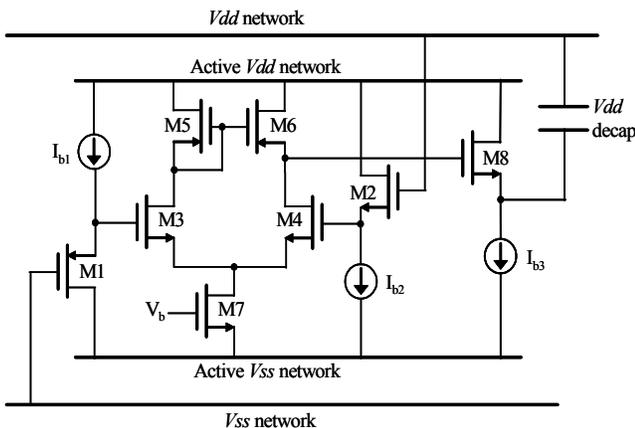


Figure 6. Operational amplifier schematic

plies and currents are generated from the active supply to the opamp. Transistors M1, M2 and bias currents  $I_{b1}$ ,  $I_{b2}$  form the input level shifters which convert the input common bias supplies of regular  $V_{ss}$  and  $V_{dd}$  to the input common-mode voltage of the gain stage, which was set at 500mV. The gain stage, which succeeds the level shifters is formed using a single-ended differential amplifier pair formed by transistors M3 and M4. Transistors M5 and M6 are the active current mirror loads to the diffamp and M7 provides its biasing current. The diffamp is followed by a source follower (M8 and  $I_{b3}$ ) as the output stage, which reduces the output impedance and provides high current drive capability to the amplifier.

The gain of the above opamp,  $A$  has a dominant pole at frequency  $\omega_0$  and can be approximated as follows [14]:

$$A = \frac{A_0}{\left(1 + j\frac{\omega}{\omega_0}\right)} \quad (8)$$

where  $A_0$  is the gain of the opamp at  $\omega=0$ .

Let us consider a power grid network consisting only of active decaps,  $C$  and no passive decaps. Then, the effective on-die capacitance in the circuit  $C_{eff}$  is given by:

$$C_{eff} = \left(2 \frac{A_0}{\left(1 + j\frac{\omega}{\omega_0}\right)} + 1\right) \frac{C}{2} \quad (9)$$

assuming that the total decap  $C$  is evenly distributed for the  $V_{dd}$  and  $V_{ss}$  lines. The impedance of the power supply network in presence of active decaps is expressed as follows:

$$Z(s) = \frac{(R + sL)\left(1 + \frac{s}{s_0}\right)}{\frac{s^3 LC}{s_0} + \left(LC(1 + 2A_0) + \frac{RC}{s_0}\right)s^2 + \left(\frac{RC_d}{2} + A_0 RC + \frac{1}{s_0}\right)s + 1} \quad (10)$$

where  $L$  is the package inductance of the grid,  $C$  is the total active decap present in the grid and  $s_0 = j\omega_0$ .

Equation (9) shows that the effective decap starts reducing after  $\omega_0$ . As a result, the package inductance becomes a dominant part of the overall power supply network's impedance, thereby resulting in a linear increase in impedance with increasing frequency as shown in (10). To improve the high frequency behavior, a small amount of passive decaps is therefore used in conjunction with the active decaps to suppress high frequency noise. This is explored further in Section 4.2.

## 4 Results

The proposed active decap circuit was designed in 130nm triple-well technology with a nominal supply of 1.2V and tested with HSPICE simulations. The next subsection presents the layout and simulations of the opamp used in the proposed active decap circuit.

### 4.1 Opamp Simulations

Figure 7 shows the layout of the opamp with a drive capability of 5pF. Several of these opamps are used to drive banks of decaps placed at different locations on the die. The area of the opamp was  $14.1\mu\text{x}11.8\mu$ . In this technology, this area amounts to approximately 0.39pF of capacitance. The area overhead of the opamp, when compared to the area needed for decap insertion is therefore small at

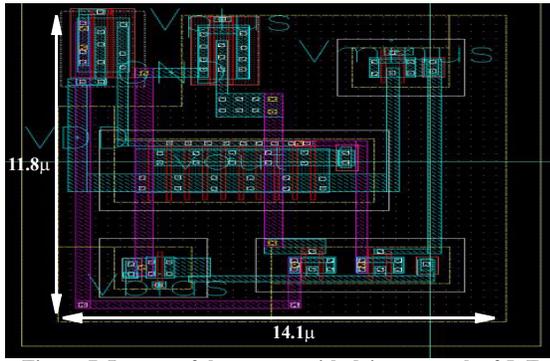


Figure 7. Layout of the opamp with drive strength of 5pF.

approximately 8%. The area overhead of the opamp design is addressed by reducing the total decap by this amount, resulting in a slightly lower total available decap. However, this reduction in available decap is easily compensated by the much larger effective capacitance that results from the active decap circuit.

Figure 8 shows the simulated gain of the opamp as a function of frequency while Figure 9 shows the transient response of the opamps obtained when used to drive a decap of 10pF (5pF each of  $V_{dd}$  and  $V_{ss}$  decaps). The gain of  $V_{dd}$  decap and  $V_{ss}$  decap were 14 and 14.2 respectively. The bandwidth of the two opamps were 197MHz and 190MHz respectively. The two signals at the extreme top and bottom of the Figure 9 are the supply fluctuations in  $V_{dd}$  and  $V_{ss}$  grid respectively. Using input level shifters, the common-mode voltages of these supply fluctuations (1.2V and 0V respectively) are converted to a DC voltage of 500mV, the bias voltage of the gain stage. In the figure, the “level shifter outputs” signals represent the signals input to the gain stage of the opamp.  $V_{ss\_decap}$  and  $V_{dd\_decap}$  signals are the output of the output stage of the opamps used to drive the decaps connected to  $V_{dd}$  and  $V_{ss}$  grid respectively.

## 4.2 Comparison of Active and Passive Decaps

In this subsection, we compare the frequency and transient response of the power supply drop with different ratios of active and passive decaps present in the supply network. Figure 10 compares the frequency response of the voltage drop for 4 different cases:

Case 1: 250pF passive decap

Case 2: 50pF active decap + 180.5pF passive

Case 3: 150pF active decap + 80.5pF passive

Case 4: 230.5pF active decap.

Note that in all but the first, all passive case, the total available decap is reduced slightly to account for the area overhead of the active decap circuit.

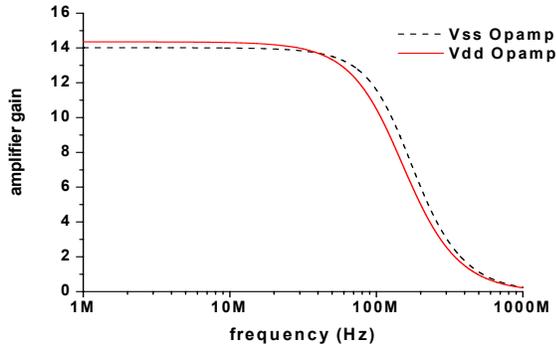


Figure 8. Gain of the opamp.

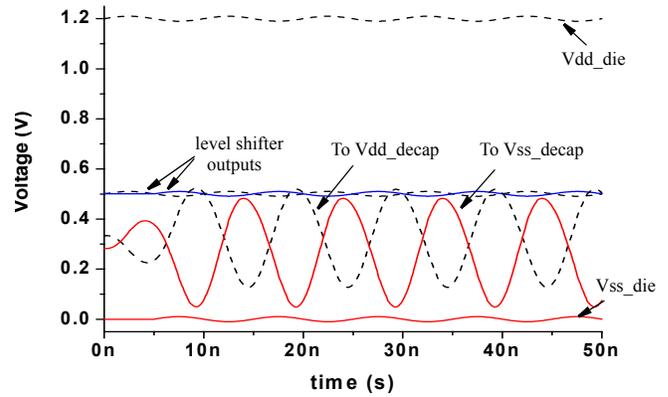


Figure 9. Transient response of the opamp.

As shown in Figure 10, the use of active decaps in Case 2, 3 and 4 results in a reduction in the worst case supply voltage drop observed at resonance. Case 1, with only passive decaps present in the grid, has a single resonance frequency at 110MHz. Case 4, which only has active decaps and consequently the maximum amount of effective decap, has the maximum suppression of the inductive noise at resonance frequency and also the maximum lowering of the resonance frequency. In particular, the resonance frequency is lowered to 35.7MHz from 110MHz, indicating an effective decap of 2nF, an 8x increase in the amount of decap. However, the effective capacitance starts to decrease rapidly with frequency resulting in an increase in supply drop at high frequencies, although the peak voltage drop still remains at a much lower value as compared to the one in Case 1. Cases 2 and 3, which use a combination of active and passive decaps, show noise suppression at all the frequencies. These cases also show a very slight second resonance at a frequency higher than the one in Case 1 due to the interaction between package inductance and passive decap present in the grid. As the amount of passive decap in the grid is reduced (active decap is increased), the first resonance peak is suppressed and the second extra resonance peak increases.

Figure 11 compares the transient response of the voltage drop for different ratio of on-die active and passive decaps present in the power grid. Figure 11a shows the current profile used, which resem-

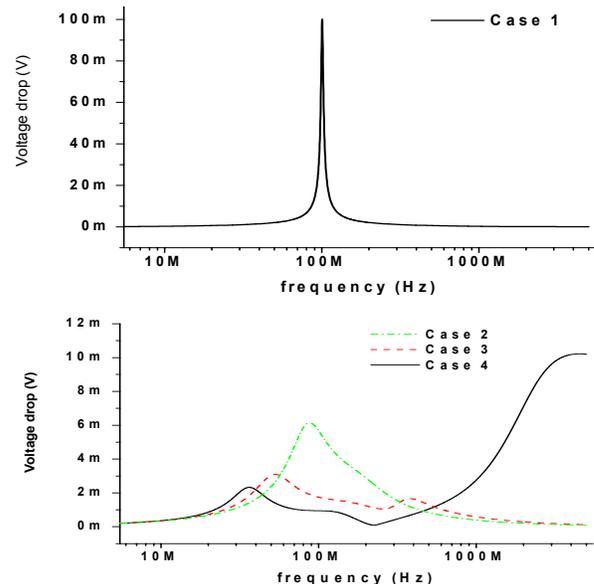


Figure 10. Comparison of frequency response of power grid with different decap sizes.

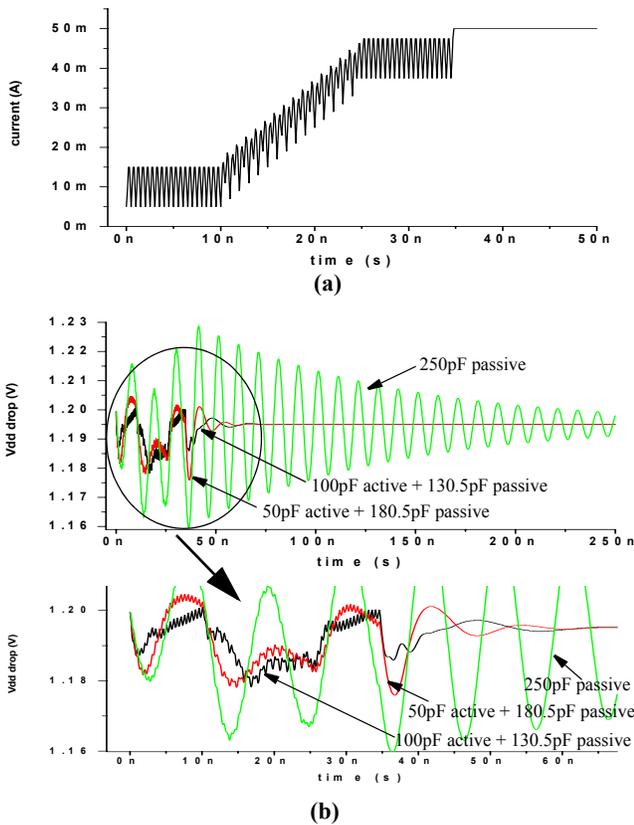


Figure 11. Comparison of transient response of power grid with different decap sizes.

bles the ramp-up of a microprocessor for low-power instructions to high-power instructions in a 15 cycles. The clock frequency of the design was assumed to be 4GHz in the experiment. Figure 11b shows the transient response for three configurations: 250pF passive, 50pF active + 180.5pF passive and 100pF active + 130.5pF passive decaps. The worst-case supply drop is reduced from 40mV (in 250pF passive case) to 22mV (in 100pF active + 130.5pF passive case) resulting in a 45% reduction in worst voltage drop. In addition, the low frequency ringing is much lesser with the usage of active decaps.

### 4.3 Impact of C4 Distribution

Figure 12 shows the worst-case voltage drop as a function of the percentage of total C4s allocated to the active supply. As the number of C4s allocated to the active supply is increased beyond a limit, the overall package inductance of the regular supply increases, thus worsening the  $Ldt/dt$  noise in the regular supply. In addition, the IR drop in the regular supply also increases with lesser number of pads allocated to the regular supply. This results in an increase in the voltage drop in the regular grid. On the other hand, if only a few pads are allocated to the active supply, the fluctuations in the supply provided to the opamps increase, thus lowering their respective gains and drive strengths. Figure 12 shows that the worst-voltage drop is at its minimum when 6% of the total C4s (3 C4s) are allocated to the active supply and the rest 47 C4s are allocated to the regular supply.

## 5 Conclusions

An active decap circuit was proposed to suppress the inductive noise in power distribution networks. The proposed circuit senses the supply drop and drives an amplified and inverted voltage fluctu-

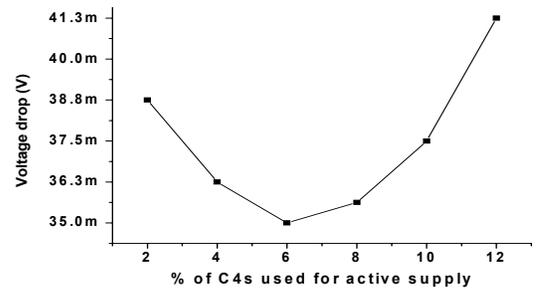


Figure 12. Voltage drop as a function of C4 allocation

ation on the decap. The active decoupling circuit is powered by a separate power supply and we studied the optimal allocation of the total C4s/pads between this second power supply and the regular supply as well as the optimal allocation of the total decoupling capacitance between actively switched and traditional static decap. Using the proposed method, the maximum supply drop is reduced by 45% compared to the use of only traditional decap, corresponding to an increase in the effective decap of approximately 8X.

## 6 Acknowledgements

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