Analysis and Optimization of Sleep modes in Subthreshold Circuit Design

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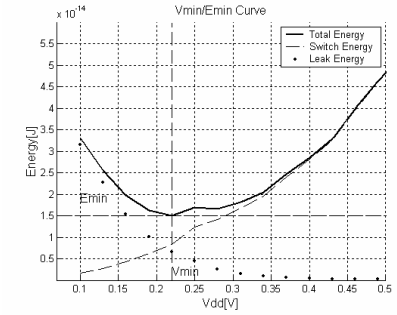
ABSTRACT

Subthreshold operation is a promising method for reducing power consumption in ultra-low power applications, such as active RFIDs and sensor networks. It was shown that operating at the so-called V_{min} supply voltage results in optimal energy operation, where V_{min} typically falls below the threshold voltage. However, all previous subthreshold analyses ignore the leakage current in standby mode. Hence, for applications where operation at V_{min} results in completion of the task well ahead of the required deadline, the energy consumption can be significantly under estimated. In this paper, we investigate the effect of the non-zero standby energy on the optimal energy consumption in subthreshold operation. We first analyze energy consumption both with and without a cutoff technique in standby mode. Two parameters are proposed to capture the cutoff structure's effect on the energy consumption. Second, a methodology to minimize the total energy consumption is addressed. The right selection of the cutoff structure is examined by comparing three different structures. Then, a co-optimization method to optimize the size of the cutoff structure concurrently with the supply voltage, is proposed. This approach reduces energy by 99.2% compared to standby energy unaware optimization.

1. INTRODUCTION

Ultra low power operation has become a key concern in VLSI design. Traditionally, voltage scaling has been used as a method to reduce energy-per-operation due to the quadratic dependence of dynamic energy on supply voltage. This has lead to the use of so-called *just-in-time* computation where the supply voltage is lowered to the point where a task is completed at exactly the time of its deadline with significant energy savings.



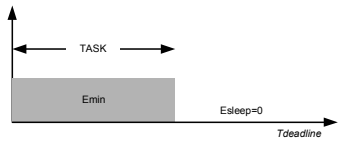
$$E = E_{switch} + E_{leak} = \frac{1}{2} n C V_{dd}^{\,2} \left[\alpha + \eta \cdot n \cdot e^{\left(-\frac{V_{dd}}{mV_T}\right)} \right] \quad \text{[EQ1][1]}$$

Figure 1 V_{min}/E_{min} Curve with Zero Sleep energy

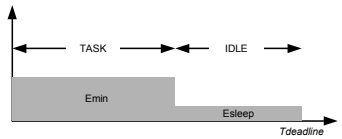
As the supply voltage is lowered, the circuit delay increases and hence the ration of leakage energy over dynamic energy increases as devices spend more time leaking. Particularly as the supply voltage falls below the threshold voltage of the devices, the delay increases exponentially leading to a rapid increase in the leakage energy. In [1], it was shown that there exists a supply voltage call V_{min} below which the reduction in dynamic energy with supply voltage cannot overcome the increase in leakage energy with supply voltage. Hence, the energy-per-operation reaches its optimum E_{min}, at the supply voltage V_{min} as shown in Figure 1 and lowering the supply voltage below V_{min} only increases the energy consumption.

Just-in-time operation is only energy efficient if the supply voltage falls above V_{min}. For typical designs, V_{min} was shown to fall around 300mV resulting in a frequency of operation in the hundreds of kHz range [3][4]. However, numerous ultra-low power applications, such as active RFIDs, sensor networks and implantable medical devices require substantial lower operating frequencies, ranging from 100's to 1000's of Hz or even less [5]. Since these applications are also extremely power constrained, operation at V_{min} is considered a viable option for them. Hence, determination of V_{min} and reliable operation at V_{min} has received significant research in recent years [1][2][8][9].

We refer to the completion time of a task when the processor is operating at V_{min} as T_{min}.



(a) Task is completed before Tdeadline at Vmin, assuming only Emin consumed



(b) Task is completed before Tdeadline at Vmin, consuming Emin + Esleep

Figure 2 Illustration of Task Scheduling at Different Deadlines

For many sensor applications, operating at the energy optimal voltage V_{min}, T_{min} will fall well in advance of the required deadline time, $T_{deadline}$. For the time that remains between T_{min} and $T_{deadline}$, they therefore enter a standby or sleep mode where the clock has been disabled. However, all previous minimum energy analyses were performed with the assumption that the leakage energy in this standby mode is zero, as shown in Figure 2(a) [1][2]. While the energy consumption in sleep mode can be significantly reduced, some leakage current will always remain, as shown in Figure 2(b). If the device spends relatively little time in standby mode, the impact of this standby energy is negligible. However, if the device spends the vast majority of time in standby mode, as is the case for many sensor applications, the standby energy can be many time that of the energy consumed in active mode. The omission of the standby energy consumption in previous minimum energy analyses was first noted in [6]. However, no detailed analysis of its impact on V_{min} and the cutoff structures was presented.

In this paper, we therefore present a new analysis of the minimum energy operation for applications that have performance requirements that fall well below the performance obtained at V_{min}. We first examine operation in the absence of any cutoff structures, where only the clock is gated in standby mode. In this case, the energy optimal supply voltage can scale far below the traditional V_{min} as $T_{deadline}$ is increased beyond T_{min}. We also show that ignoring the standby energy results in highly suboptimal energy consumption.

We then examine three different cutoff structures, namely MTCMOS, DTCMOS, and stack forcing. We show that all cutoff structures present a trade-off between leakage reduction and operating frequency degradation. In super-threshold operation, the operating frequency loss due to cutoff structures, such as MTCMOS, is typically small and limited to 10% or less [7]. However, in subthreshold operation the circuit delay is exponentially dependent on the supply voltage and hence has a much higher performance impact. Since the leakage power is substantial in active mode, the performance penalty introduces a significant energy penalty. Hence, we find that the sizing of cutoff structures is non-trivial and represents a trade-off between standby mode leakage energy and active mode leakage energy.

Since leakage current is weakly dependent on supply voltage, finding the optimal operation for very large values of $T_{deadline}$ involves a co-optimization of the sizing of the cutoff structure and the operating voltage. In other words, by increasing V_{dd} above V_{min}, we can achieve the small size of the cutoff structure which reduces the standby mode leakage energy. Also, the higher V_{dd} allows the operation to move into the regime of less active mode leakage energy. Though the active switching energy increases due to the increased V_{dd}, however the gain from the leakage energy from both standby and active modes affords this approach. We present results showing that optimization of only the sizing of the cutoff structure can improve the energy consumption by 98% for a $T_{deadline}$ that is 1000x that of T_{min}. By performing a co-optimization of both the sizing and the supply voltage, this energy reduction increases to 99.2%, along with 93% area saving for the cutoff structure, demonstrating the importance of accurate accounting of standby energy in subthreshold design.

The remainder of this paper is organized as follows: In Section 2, we extend the existing analytical energy optimization analysis to include standby energy. In Section 3, we examine three common cutoff structures and present the proposed optimization methodology. We also present comparison between when optimizing their sizes with a fixed supply voltage, V_{min}, and when co-optimizing of sizes and supply voltage together. In Section 4 we present our conclusions.

2. Impact of non-zero standby energy on E_{min}

The leakage, switch and total energy consumption with voltage scaling is shown in Figure 1 and demonstrates the existence of an energy minimum, E_{min}, at supply voltage V_{min}. The expression of the minimum energy consumption, as derived in EQ1 is also shown. However, this and other previous analyses overlooked the possible standby leakage. In order to examine how non-zero standby energy affects the V_{min}/E_{min} curve, we first investigate the case in which a circuit should finish a task at $T_{deadline}$, which is longer than T_{min}, the delay of the circuit when operating at the traditional V_{min} supply voltage. We define the delay of the circuit at the traditional V_{min} as T_{min} and define the ratio of $T_{deadline}$ over T_{min} as K_{duty}: $K_{duty}=T_{deadline} / T_{min}$. In other words, K_{duty} expresses the deadline compared to the completion time of the task at V_{min}. Hence, for $K_{duty} > 1$, there is non-zero standby time unless the supply voltage is lowered below V_{min}.

Initially, we assume that there is no cutoff structure present and then examine different cutoff structures in subsequent sections. Without cutoff structures, the total energy can be expressed as:

EQ2, which is modified from EQ1, shows that same leakage current flows for the standby time as well as the active time and hence has a higher total energy.

$$\begin{aligned} E_{Total} &= E_{switch} + E_{leak} + E_{sleep} \\ &= E_{switch} + t_{delay} P_{leak} + (T_{deadline} - t_{delay}) \cdot P_{leak} \\ &= E_{switch} + T_{deadline} P_{leak} \end{aligned} \quad \text{[EQ2]}$$

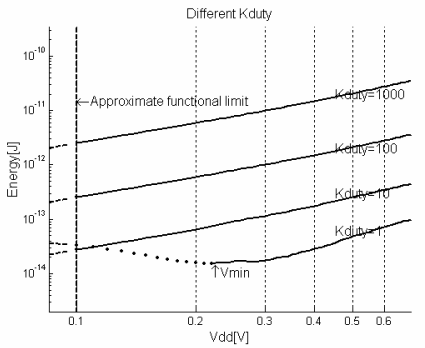


Figure.3 V_{min} /E_{min} Curve with different K_{duty} with Sleep Energy

Note that both E_{switch} and $T_{deadline}$·P_{leak} in EQ2 have monotone increasing behavior with V_{dd}, thus forcing the optimal supply voltage below V_{min}, as shown in Figure 3. The region of the dotted line for $K_{duty} = 1$, represents that $T_{deadline}$ cannot be met over this voltage range. Note also that the voltage was not scaled below 100mV, which is the approximate minimum functional limit for subthreshold operation.

2.1 The effects of cutoff structures on E_{min}

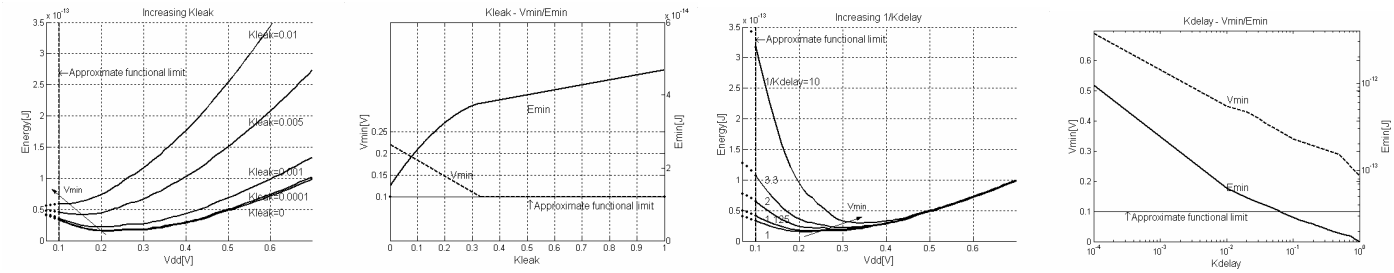
As shown in Figure 3, using no cutoff structure significantly increases the total energy consumption for large values of K_{duty}. Therefore, cutoff circuitry such as MTCMOS is commonly introduced to reduce the energy consumption in standby mode. Note that there are two eminent effects of the cutoff circuitry on the main circuit. The major effect of the circuitry is to reduce the leakage current during the standby mode, which is the main purpose of the circuitry. However the cutoff circuitry can degrade the performance of the main circuit as a side effect. This is caused by the reduced swing between virtual supply rails. The reduced swing induces a smaller gate-source voltage, thus degrading current driving capacity of the gate, which in turn degrades the performance [7]

Both two effects should be considered to understand the impact of the cutoff structure on V_{min}/E_{min}. We therefore propose two parameters in EQ3 to capture these effects. The first parameter, denoted by K_{leak}, leakage reduction factor, indicates how much the leakage in the sleep mode reduces compared to the leakage current without any cutoff structure. The second parameter, the delay degradation factor, denoted by $1/K_{delay}$ indicates the ratio of the delay increase caused by the cutoff circuitry.

$$\frac{1}{K_{delay}} = \frac{t_{delay\_w/\_cutoff\_circuitry}}{t_{delay\_w/o\_cutoff\_circuitry}} \quad \text{[EQ3]}$$

$$K_{leak} = \frac{I_{leak,w\_sleep\_structure}}{I_{leak,w/o\_sleep\_structure}}$$

As can be seen, both parameters can only take on values between 0 and 1.We first examine the behavior of the E_{min} with an imaginary cutoff structure. EQ4 shows the total energy when a cutoff structure with characteristics K_{leak} and $1/K_{delay}$ is used. The parameter T_{min} denotes the main circuit delay at V_{min} without the cutoff structure and P_{leak} denotes the leakage power without the



(a) V_{min} /E_{min} Curve **(b) K_{leak} - V_{min} /E_{min}** **(c) V_{min} /E_{min} Curve** **(d) K_{delay} - V_{min} /E_{min}**

Figure 4 V_{min} /E_{min} Change with K_{leak} and K_{delay}

cutoff structure.

$$E_{Total} = E_{switch} + E_{leak} + E_{sleep} \quad [EQ4]$$
$$= E_{switch} + \frac{1}{K_{delay}} t_{delay} P_{leak} + (K_{duty} T_{\min} - \frac{1}{K_{delay}} t_{delay}) \cdot K_{leak} P_{leak}$$

E_{switch} denotes the switch energy, which, theoretically, is also affected by the cutoff structure since the cutoff structure limits the voltage swing. However this was found to be a secondary effect, which can be ignored without significant loss in accuracy.

We now examine E_{min} for different values of K_{leak}, and $1/K_{delay}$. In Figure 4(a), K_{leak} is sweep from 0 to 0.01. K_{leak} =1 implies that there is no leakage reduction. Large values of K_{leak} increases the total energy as expected from the equation. Furthermore, for large values of K_{leak}, V_{min} should be decreased to reduce the increase of the E_{sleep}, as shown in the Figure 4(b)

Figure 4(c) shows the effect of the $1/K_{delay}$ on E_{leak} and V_{min}. Note that E_{leak} is small at superthreshold voltages because of the small t_{delay}. Therefore the effect of the $1/K_{delay}$ is generally negligible at the superthreshold operation. On contrary, the effect of $1/K_{delay}$ is pronounced at the low voltage at which t_{delay} is large and E_{leak} has a substantial portion of total energy. As a result, V_{min} increases as $1/K_{delay}$ increases, as shown in the Figure 4(d).

Figure 4 shows that E_{min} and V_{min} have a strong dependence on the characteristics of the cutoff structure in subthreshold operation. The value of $1/K_{delay}$ primarily affects E_{leak}, while the value of K_{leak} affects E_{sleep}. Hence, as the values of $1/K_{delay}$ and K_{leak} change for different cutoff structures, either E_{leak} or E_{sleep} can become the more dominant portion of the total energy. In response, the optimal operating voltage will try to minimize this dominant energy component. Hence, as $1/K_{delay}$ increases E_{leak}, V_{min} will increase to reduce the circuit delay and thereby E_{leak}. On the other hand, as K_{leak} increases E_{sleep}, it becomes advantageous to increase circuit delay and reduce V_{min}. Therefore, the two factors $1/K_{delay}$ and K_{leak} present conflicting influences on V_{min} and require detailed analysis for optimal energy operation.

2.2 MTCMOS cutoff structures

For an actual MTCMOS cutoff structure, as shown in Figure 5 the constants $1/K_{delay}$ and K_{leak} are not independent, but are related to each other through the value of V_{dd} and the MTCMOS footer width.

First, we derive $1/K_{delay}$ for an MTCMOS structure in EQ5 where V_{swing} is the voltage across virtual rails. The expression for K_{leak} is given in EQ6. In this equation, it is assumed that the voltage across the footer is V_{dd} in the standby time, due to the high resistance of the footer compared to the general circuitry. Accordingly, it is shown that K_{leak} is a linear function of the footer width.

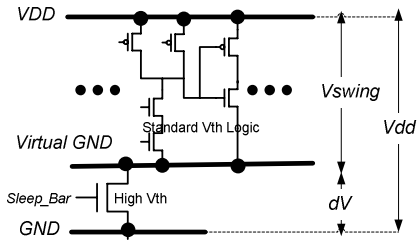


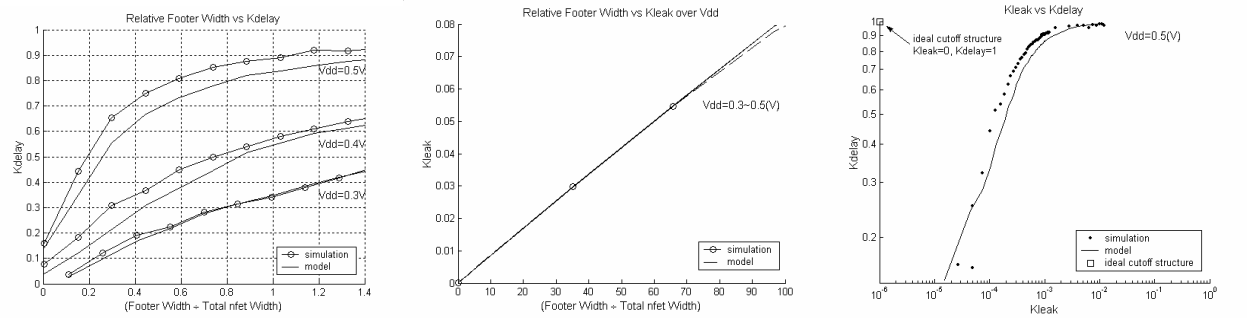
Figure.5 MTCMOS Circuit

$$\frac{1}{K_{delay}} = \frac{t_{delay\_w/\_mtcmos}}{t_{delay\_w/o\_mtcmos}} \quad [EQ5]$$
$$= \frac{CV_{swing}}{CV_{dd}} \cdot \frac{\mu C_{ox} \frac{W}{L} V_T^2 (1-m) e^{\frac{-V_{swing}}{mV_T}} (1 - e^{\frac{-V_{swing}}{mV_T}})}{\mu C_{ox} \frac{W}{L} V_T^2 (1-m) e^{\frac{-V_{dd}}{mV_T}} (1 - e^{\frac{-V_{dd}}{mV_T}})} = \frac{V_{swing}}{V_{dd}} e^{\frac{V_{dd} - V_{swing}}{mV_T}}$$

$$K_{leak} = \frac{I_{leak,w\_sleep\_structure}}{I_{leak,w/o\_sleep\_structure}} \quad [EQ6]$$
$$= \frac{\mu_{eff,hvt,n} C_{ox} \frac{W_{hvt,n}}{L_{eff,hvt,n}} \exp(\frac{-V_{th,hvt,n}}{mV_T})(1 - \exp(-\frac{V_{dd}}{V_T})}{\mu_{eff,svt,n} C_{ox} \frac{W_{svt,n}}{L_{eff,svt,n}} \exp(\frac{-V_{th,svt,n}}{mV_T})(1 - \exp(-\frac{V_{dd}}{V_T})} = k \cdot W_{hvt,n}$$

Figures 6 (a) and (b) show the dependency of $1/K_{delay}$ and K_{leak} with the footer width and the supply voltage, respectively. The value of $1/K_{delay}$ can easily approach 1 by increasing the footer width at the high voltage, while it more slowly increases at the low voltage. On the other hands, the K_{leak} is simply linear function of the footer width across a wide voltage range. The plots in Figure 6 (a) and (b), compare the accuracy of the proposed model against spice simulation, demonstrating acceptable accuracy. The final plot in Figure 6 (c) shows the interdependence between K_{leak} and $1/K_{delay}$ as the width of the MTCMOS device is swept. The ideal cutoff structure point lies at K_{leak} =0 and K_{delay} =1. This plot provides a means to compare the efficacy of different cutoff structures for subthreshold design, as discussed further in Section3.

Using $1/K_{delay}$ and K_{leak}, we now derive the energy equation, EQ7, by plugging EQ5 and EQ6 into EQ4. E_{switch} and E_{leak} can be substituted from EQ1. Note that the energy equation is a function of V_{dd}, K_{leak}, K_{delay} and technology constants. In Figure 7, we plot the expression in EQ7 to illustrate how total energy changes with the different footer width and the V_{dd} in subthreshold operation. First, for superthreshold supply voltage (> 450mV), E_{leak} is relatively small compared to E_{switch}. Therefore the effect of the $1/K_{delay}$ on E_{leak} is negligible for the total energy. Hence, K_{leak} can be reduced linearly with the footer width while E_{switch} is also reduced slightly with smaller footer width due to the reduced Vswing. Therefore reduced footer width tends to minimize the total energy at superthreshold supply voltages.



(a) Width - K_{delay} **(b) Width - K_{leak}** **(c) K_{leak} – K_{delay}**

Figure 6 K_{leak} and K_{delay} change with Width and V_{dd}

$$E_{Total} = E_{switch} + E_{leak} + E_{sleep}$$
$$= \frac{1}{2} \cdot n \cdot CV_{dd}V_{swing} \cdot \alpha$$
$$+ \frac{1}{2} nCV_{dd}{}^2 \eta \cdot ne^{\frac{-V_{dd}}{mV_T}} \cdot \left(\frac{V_{swing}}{V_{dd}} e^{\frac{V_{dd}-V_{swing}}{mV_T}} \right) \quad \text{[EQ7]}$$
$$+ (K_{duty} t_{norm} - e^{\frac{V_{dd}-V_{swing}}{mV_T}} \cdot t_{\min}) \cdot k \cdot W_{hvt,n} \cdot I_{leak,w/o\_mtcmos} V_{dd}$$

$$E_{Total} \approx K_1 V_{dd} V_{swing} + K_2 V_{dd}{}^2 e^{\frac{-V_{dd}}{mV_T}} \left(\frac{V_{swing}}{V_{dd}} e^{\frac{V_{dd}-V_{swing}}{mV_T}} \right) + K_3 K_{duty} k W_{hvt,n} V_{dd}$$

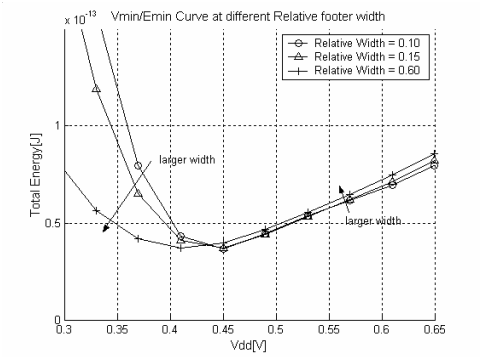


Figure.7 V_{min} /E_{min} with different footer width, K_{duty}=100

On the other hands, at low voltage, E_{leak} must be taken into consideration. In this case, increasing footer width helps to reduce $1/K_{delay}$ as a large width increases on-conductance and increases Vswing. However E_{sleep} is proportional with the footer width. Therefore the energy initially decreases with increasing width and after a point starts to increase again due to increased E_{sleep}. Hence, at subthreshold operation, there is an optimal footer width that depends not only on $1/K_{delay}$ and K_{leak} but also on K_{duty}. For example, a large value of K_{duty} makes E_{sleep} more dominant in the energy equation reducing the optimal footer width.

3. Energy Minimization

In the Section 2, the change of the V_{min} /E_{min} curve with non-zero sleep energy condition was analyzed. As shown, the total energy in subthreshold operation is a strong function of the size and type of cutoff structure. In this section, we therefore first compare the K_{leak} and K_{delay} of different cutoff structure quantitatively. In doing so, it can be determined how effective each cutoff technique can be, compared to an ideal cutoff technique.

Secondly, we propose a co-optimization method in this section, which optimize the footer size of the cutoff structure as well as the supply voltage. Since EQ7 is a function of K_{duty}, this co-optimization also depends on K_{duty}.

3.1 Comparison of cutoff structures

Values of K_{leak} =0 and K_{delay} =1 for a cutoff structure imply that the structure can eliminate the leakage completely during the standby time along with no delay penalty in the active time.

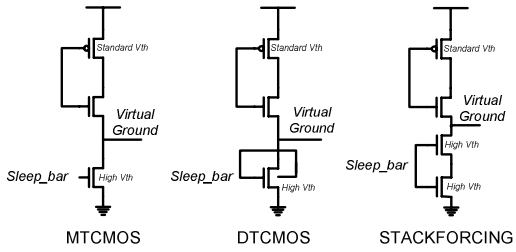


Figure 8 MTCMOS, DTCMOS, and Stackfocring MTCMOS

Figure 8 shows three well-known cutoff structures, which are MTCMOS, DTCMOS, and Stack-Forcing. DTCMOS is similar to MTCMOS except that the gate and the body of the footer are tied to increase on-current. Therefore DTCMOS is expected to have less $1/K_{delay}$ compared to the MTCMOS. The stack-forcing structure places two footers in series to improve the off current. These series-connected footers induce negative V_{gs} in the upper footer, which exponentially increase its off-resistance [7]. Therefore its K_{leak} should be smaller then that of MTCMOS; however $1/K_{delay}$ will also be worse due to increased resistance.

At a 500mV operating voltage, the K_{leak}-K_{delay} curves of each structure are shown in the Figure 9. For the same value of K_{leak}, it is clearly shown that DTCMOS has the least $1/K_{delay}$, and thus the smallest E_{leak}. The stack-forcing cutoff structure has better K_{delay} than MTCMOS but is worse than DTCMOS and, in addition, can not achieve high values of K_{delay}.

This difference of K_{leak} and K_{delay} eventually affects the energy. In EQ7, other parameters are constant at a given voltage regardless of the kinds of the cutoff structures. Over the wide voltage range, this ordering of K_{leak} - K_{delay} curve among the three techniques is maintained. Therefore, the DTCMOS cutoff structure, among the three, offers the best combination of K_{leak}-K_{delay} parameters, which in turn minimize the total energy. Note that the DTCMOS incurs a higher implementation complexity than traditional MTCMOS. In addition, the forward bias voltage between body and source/drain may cause large current at high voltage, which limits its usage. For consistency, we therefore focus on regular MTCMOS in the remainder of our analysis, although the same concepts apply to DTCMOS and stack forcing as well.

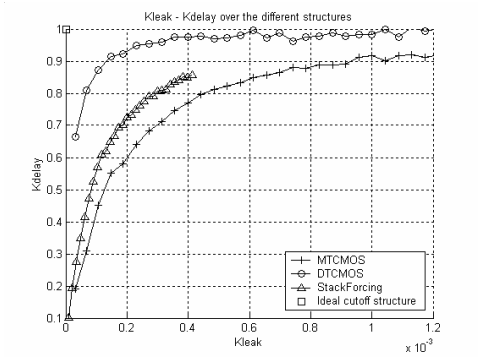
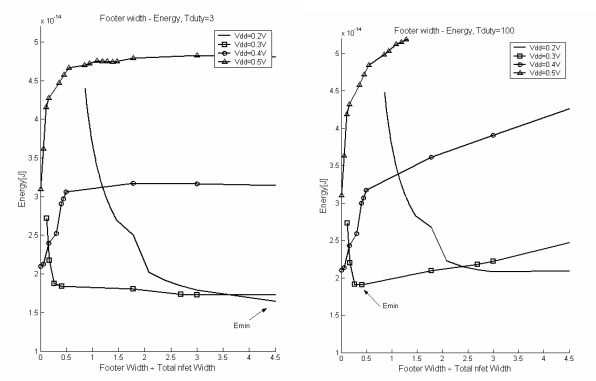


Figure.9 K_{leak} - K_{delay} curves with different cutoff structure

3.2 Co-Optimization of V_{dd} and footer width

In the conventional optimum voltage analysis in the subthreshold operation[1], V_{min} was selected without considering the sleep energy. We have shown, however, that the sleep energy can significantly affect the V_{min}/E_{min} values. In addition, we also showed that the cutoff structure impact the V_{min} /E_{min} values as well. Given a fixed supply voltage, the footer width can change the total energy consumption. Therefore, it is necessary to optimize not only the supply voltage but also the footer width to fully minimize the total energy consumption under non-zero sleep energy.

For small values of K_{duty}, we examine how to optimize V_{min} and the footer width together. If K_{duty} is unity, the largest energy saving can be achieved by supplying the conventional V_{min} without any cutoff structure. Adding cutoff structures induce extra delay, which increase E_{leak}. Because there is no standby time, i.e. K_{duty} =1, the sleep leakage reduction is of no use in this case.



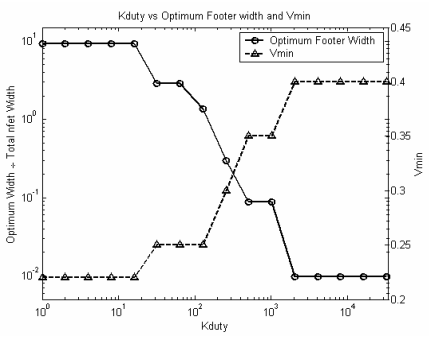
(a) K_{duty} =3 **(b) K_{duty} =100**

Figure.10 Energy-Width Curves at different Voltages

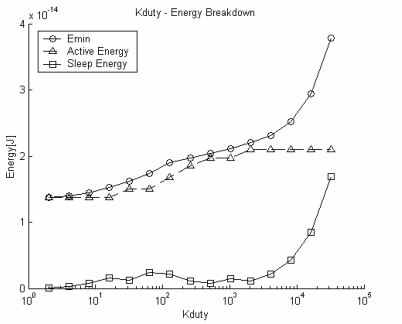
For small values of K_{duty} > 1, the optimum V_{dd} will be similar to the conventional V_{min} without the cutoff structure and the footer width will be large. A small K_{duty} implies that the E_{sleep} is small; therefore the increase of the E_{sleep} due to increased width is negligible to the total energy. Rather, the increased the footer allows nearly same active mode leakage energy with small performance penalty at around V_{min}, which minimizes the total energy.

In the Figure 10 (a), each curve represents the change of the total energy with the footer width for small K_{duty}. Note that standby energy is negligible due to the small K_{duty}. For high V_{dd}, such as 0.5V and 0.4V, the energy curve is increased with the width due to dominance of E_{active}. However, for small V_{dd}, such as 0.3V and 0.2V, small width exponentially increases the delay, eventually resulting in large energy. However, note that as the width increases, the energy at the low V_{dd} decreases and becomes less than the energy consumption at high voltage. For example, in Figure 10(a), the energy curve of 0.2V is larger at small width, but becomes smaller at large width than the energy curve of 0.3V. Therefore for the small K_{duty}, it is better to use large width and small V_{dd} together to minimize the total energy consumption.

Figure 10(b) shows the same energy curve with large values of K_{duty}. Because of the large value of K_{duty}, E_{sleep} is no longer negligible. Therefore, increasing width may increase the total energy consumption. Because of the increased E_{sleep}, the energy consumption at 0.2V with large footer cannot become smaller than the energy curve at 0.3V as in Figure 10(a). Instead, the 0.3V curve has a minimum point in at reduced the footer width. Therefore V_{min} is increased while the footer width is reduced for the energy minimization for the large K_{duty}.



(a) K_{duty} - V_{min} and Optimum Footer width



(a) K_{duty} – E_{min} breakdown into E_{active} and E_{sleep}

Figure.11 New V_{min} and Optimum Footer Width at different K_{duty}

The Figure 11 (a) shows how V_{min} and the optimum footer width change as K_{duty} increases. For the small K_{duty}, the optimum width is extremely large and V_{min} approaches the conventional V_{min} value. Naturally, the extremely large footer size may be a problem from the layout area's perspective and could be omitted with relatively low energy loss.

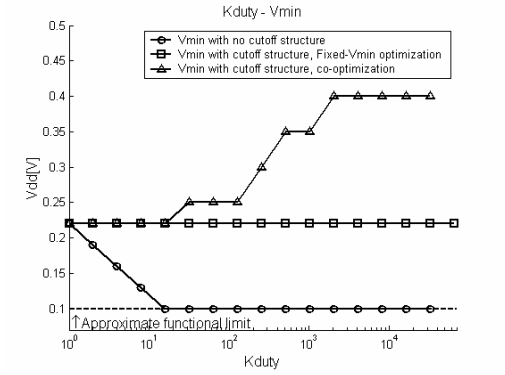
For a large values of K_{duty}, both V_{min} and footer size change to achieve the minimum energy consumption. Because of the large K_{duty}, E_{sleep} is no longer negligible, shown in Figure 11 (b) and thus the footer size is reduced for E_{sleep}. This change of the footer size elevates V_{min} to avoid exponentially increased delay, potentially resulting in larger energy consumption. Moreover this small footer size forces the voltage between virtual rails to approach conventional V_{min}, which is helpful to reduce active energy. Finally the leakage current during the standby time is nearly constant over different supply voltage making this increase in V_{min} feasible from an energy perspective.

3.3 Comparison of the optimization methods

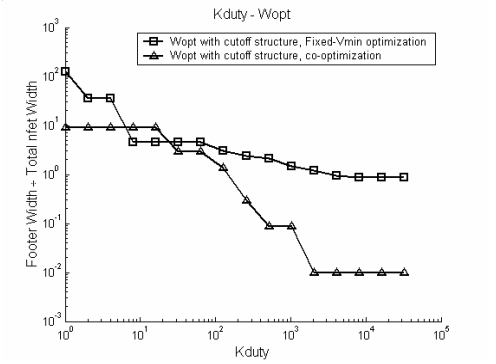
In this final section, three strategies to minimize the energy consumption with non-zero standby energy are compared. The first approach is to use no cutoff technique. Only supply voltage can be optimized to minimize the energy consumption. In the second approach, referred as fixed-V_{min}-optimization, a cutoff structure is used and the footer width is optimized while a conventional fixed V_{min} is used. The final approach is to optimize both the footer width and the supply voltage, referred to co-optimization.

Figure 12 (a) shows the change of V_{min} at each strategy. In the first strategy, the V_{min} is reduced to the functional limit V_{dd} as long as the task can be completed in K_{duty}. The fixed-V_{min}-optimization uses the conventional V_{min}. In case of the co-optimization, the V_{min} increases with K_{duty}, as explained in the Section 3.2. Figure 12(b) indicates the behavior of the optimum footer width. In the fixed-V_{min}-optimization, the footer width is reduced less compared to the co-optimization, due to the low supply voltage as expected.

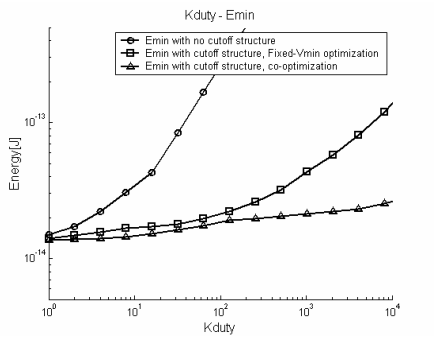
Finally, the total energy consumption of each strategy is shown in the Figure 12 (c). Even at relatively small K_{duty}, the first strategy induces significantly large energy consumption. In addition, the difference of the energy between fixed-V_{min} -optimization starts to increase at larger K_{duty}. Therefore the co-optimization is required to minimize the energy consumption, in particular large K_{duty} that exceeds 1000. Note however, that for many sensor applications, values of K_{duty} can easily exceed 10,000, resulting in a 99% energy loss without use of the proposed co-optimization



(a) K_{duty} – V_{min} over Three Strategies



(b) K_{duty} – Optimum Footer Width over Three Strategies



(c) K_{duty} – E_{min} over Three Strategies

Figure 12 Comparison of three optimization Strategies.

4. Conclusion

In this paper, the interaction of the optimal energy, supply voltage and cutoff structures are investigated for subthreshold design. We show that ignoring standby leakage current in subthreshold can significantly impact the energy efficiency of the design. Furthermore, we show that counter to intuition, applications that spend a large portion of time in standby mode require an increased supply voltage compared to the traditional V_{min} combined with a much smaller cutoff transistor width. We also proposed two metrics to compare the effectiveness of cutoff structures in subthreshold operation. Finally, we show that by using the proposed co-optimization of voltage and cutoff width, more that 99.2% energy reduction can be obtained for applications with large values of K_{duty}.

References

[1] B. Zhai, D. Blaauw, D. Sylvester, K. Flautner, *"Theoretical and Practical Limits of Dynamic Voltage Scaling"*, DAC, pp. 868-873, June, 2004

[2] B. Calhoun, A. Chandrakasan, *"Characterizing and modeling minimum energy operation for subthreshold circuits"*, ISLPED, no.3, pp.90-95, Aug 2004

[3] A. Wang, A. Chandrakasan, "A 180-mV subthreshold FFT processor using a minimum energy design methodology", IEEE J. Solid-State Circuits, vol.40, no.1, pp.310-319, Jan 2005

[4] B. Zhai, L. Nazhadili, J. Olson, A Reeves, M Minuth, R Helfand, S. Pant, D. Blaauw, T. Austin, "A 2.60pJ/Inst Subthreshold Sensor Processor for Optimal Energy Efficiency", Symp. On VLSI Circuits, pp.154-155,2006

[5] L. Nazhadili, M. Minuth, T. Austin, *"SenseBench: toward an accurate evaluation of sensor network processors"*, Workload Characterization Symposium, pp.197-203, Oct, 2005

[6] H. Chung, E. Hong, K. Kim, S. Cho, *"Optimum Supply Voltage and Sleep Transistor Sizing for Energy Minimization in Latency-Constrained MTCMOS Circuits"*, International Symposium on System-On-Chip, pp.365-368, Nov, 2006

[7] J. Kao, A. Chandrakasan, D. Antoniadis, *"Transistor Sizing Issue and Tool for Multi-Threshold CMOS Technology"*, DAC, pp. 409-414, June, 1997

[8] B.C. Paul, A. Raychowdhury, K. Roy, "*Device optimization for digital subthreshold logic operation*," IEEE Trans. Elect. Devices, pp. 237-247, Feb, 2005

[9] T. Kim, H. Eom, J.Keane, and C.Kim, "*Utilizing Reverse Short Channel Effect for Optimal Subthreshold Circuit Design*," International Symposium on Low Power Electronics and Design, Oct, 2006