22.9 A Charge-Injection-Based Active-Decoupling Technique for Inductive-Supply-Noise Suppression

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Aggressive scaling and increasing clock frequency have exacerbated inductive (Ldi/dt) supply noise, decreasing the robustness of power delivery networks. Ldi/dt is further aggravated by commonly used power-reduction techniques such as power/clock-gating and frequency stepping in DVS systems. On-die passive decoupling capacitance (decap), which has traditionally been used for suppressing Ldi/dt noise, has become expensive due to its area and leakage power consumption overhead. As a result, several circuits [1-3] have been reported that actively regulate the supply against sudden surges in load current. However, these techniques deliver only limited charge [1], are suited only for resonance damping [2] or require an additional high-voltage supply [3]. Recently, adaptive frequency-management techniques [4,5] for compensating supply current transients have also been reported.

We demonstrate an active circuit to detect and suppress excessive supply-voltage undershoots and overshoots caused by large current transients or by excitation of supply resonance. A nominal-voltage active supply, V_{DDA}, is used to inject extra charge into the power grid during excessive undershoots. The use of a nominal-voltage V_{DDA} eliminates the need for any high-voltage supplies and enables use of decaps and transistors with nominal oxide thickness. Furthermore, this method has the advantage that the active decap bank, C_a, behaves as a passive decap when the supply voltage is within safety margins. For a voltage regulation tolerance $k \cdot V_{DD}$, the decap amplification factor is $(0.5 + 1/k)$, which is significantly higher than that in the regulator of [1]. A typical voltage regulation tolerance of $k = 10\%$ yields a decap amplification factor of 10.5×.

Figure 22.9.1 shows a simplified model of a power delivery network without and with our active circuit for supply-noise suppression. Also shown is a typical unregulated supply-noise waveform with pre-specified undershoot and overshoot thresholds, V_H and V_L. In the noise suppression technique, a small fraction of the total pads available for V_{DD} are allocated to V_{DDA} such that the total number of pads is kept constant. The total area of the passive decap, C_p, is reduced to incorporate C_a and account for the area overhead of the active circuit. C_a is connected between V_{DD} and V_{SS} through T_0, and acts as a normal passive decap when the supply voltage is within safe bounds. When a supply drop below V_L is detected, T_0 is turned off and T_1 ramps up the negative terminal of C_a from 0 to V_{DDA}, injecting a charge C_a V_{DDA} into the power grid. To prevent excessive overshoots, a shunt load T_2 is turned on while C_a is simultaneously recharged.

One of the key concerns in overshoot/undershoot regulation is detection speed. Analog detection techniques are either slow or consume a large amount of quiescent current. Therefore, we use a fully digital solution, with a simulated response time of 330ps, where two sets of clocked comparator banks (one each for undershoot and overshoot detection) are used for differential sampling of V_{DD} and V_{SS} noise at a high frequency (Fig. 22.9.2). A level-shifter first translates V_{DD} and V_{SS} noise to a common-mode reference, V_{ref}, of 600mV. This implementation uses an external reference voltage for V_{ref}. However, V_{ref} can be generated on-chip and any noise in V_{ref} affects the common-mode voltage only, making the differential sensing immune to noise. The translated waveforms, V_+ and V_- are differentially sensed by 2 banks of 6 clocked comparators. Transistors M_l and M_r in each comparator are skewed to create switching thresholds (V_H or V_L) between V_+ and V_-. Calibration voltages $C_{l,un}$, $C_{r,un}$ ($C_{l,ov}$, $C_{r,ov}$) provide post-silicon tuning of V_H (V_L), if required. An effective sampling rate of 20GS/s, which captures ~100 samples before the first supply droop maximum, is achieved using a 6-phase (ϕ_1-ϕ_6) 3.33GHz sampling clock. The comparator outputs are ORed together and buffered to generate S_{normal}, S_{ov} and S_{un}.

A configurable load-current generator (10 to 120mA), with variable duty cycle and period is implemented using an array of variable-width transistors connected between V_{DD} and V_{SS}. The low and the high-periods of the load-current are independently tunable from 500ps to 2μs. A V-I converter-based drop detector circuit [6] is implemented to measure the supply noise. The supply noise measurements are verified using two probe pads.

A test-chip (Fig. 22.9.7) is fabricated in a 0.13μm 1.2V triple-well CMOS process. The unregulated and regulated test-cases are implemented for an iso-area iso-pad comparison. The unregulated case uses 3 V_{DD} pads, 3 V_{SS} pads and 760pF of C_p. For the regulated case, 1 pad is re-allocated to V_{DDA} resulting in 2 regular V_{DD} and 3 V_{SS} pads. A small amount of decap was allocated for V_{DDA} to prevent excessive ringing. The values of C_p', C_a and decap for V_{DDA} are 430pF, 220pF and 90pF, respectively. The active circuit area, which includes the sampling-clock generator, undershoot/overshoot detectors and switches $T_{0\text{-}2}$, is equivalent to the area of 10pF decap (1.54% of the total decap area). The power overhead of the active circuit is measured to be less than 1% of the peak power consumption of 48mW.

Figure 22.9.3 shows a comparison of the measured on-die supply noise with and without supply regulation for an average die. In the top of Fig. 22.9.3, the excitation load-current ramps up from 0 to 40mA and back, representative of the wake-up and turn-off of a power/clock-gated module. Active regulation reduces the peak-to-peak supply drop from 298mV to 126mV, an improvement of 57%. The steady-state IR-drop remains the same in regulated and unregulated cases. During resonance (bottom of Fig. 22.9.3), the peak-to-peak supply drop reduces from 549mV to 133mV, an improvement of 75%.

Figure 22.9.4 plots the measured worst drop and improvement as a function of peak load-current (I_{max}) for one die. At high loads, the injected charge gets limited by the size of C_a and T_1. The best improvement of 57.7% is measured for an I_{max} of 40mA. Figure 22.9.5 shows the measured regulated worst drop as a function of V_{DDA}. The regulated supply exhibits a second dip immediately after the first one, which is due to the recharging of C_a once V_{DD} is above V_L. The injected charge increases with V_{DDA}, resulting in a reduction in the first dip. As V_{DDA} is increased above 1.2V, the second dip becomes more prominent, increasing the worst drop.

Figure 22.9.6 (left) shows the frequency dependence of the supply noise, demonstrating a significant improvement in the frequency response of the supply network. A statistical analysis, shown in Figure 22.9.6 (right), is performed on 38 chips for step current-loads to evaluate the effect of a single global setting of C_r and C_l for all chips as opposed to individual tuning of each die. The minimum, maximum and average drop improvements for a global calibration setting are 47.1%, 59.6% and 55.9%, respectively. When each die is tuned for its best calibration, the minimum, maximum and average improvements increase to 51%, 59.7% and 57.6%, respectively, indicating only a marginal improvement and showing that the overhead of individual die calibration can be avoided.

Acknowledgements:
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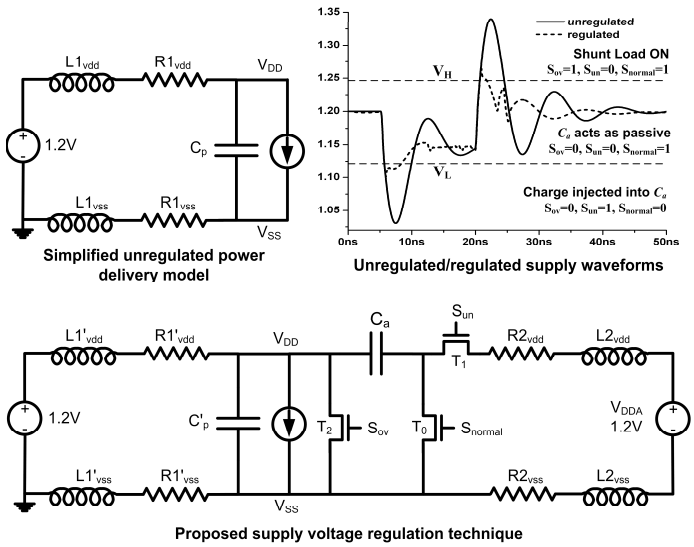

Figure 22.9.1: Power delivery model without and with active noise suppression.

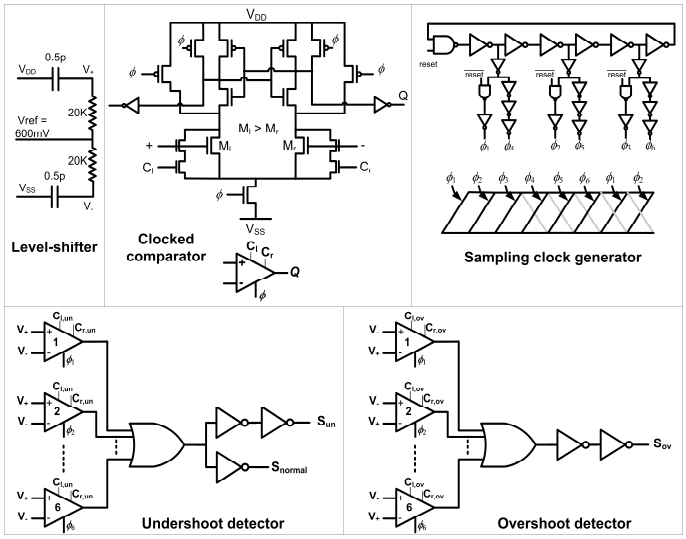

Figure 22.9.2: Schematics of undershoot/overshoot detector circuits.

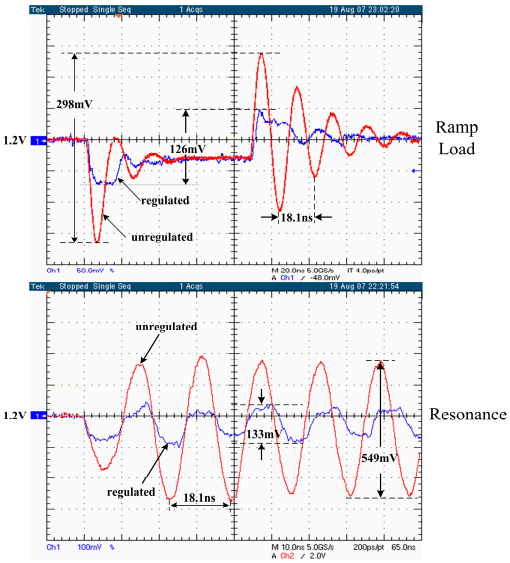

Figure 22.9.3: Measured unregulated/regulated supply noise waveforms.

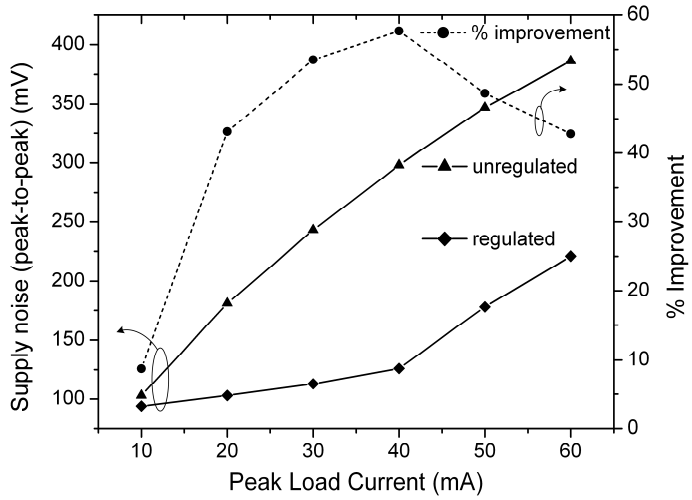

Figure 22.9.4: Measured unregulated/regulated peak-to-peak supply noise and percentage improvement vs. load-current.

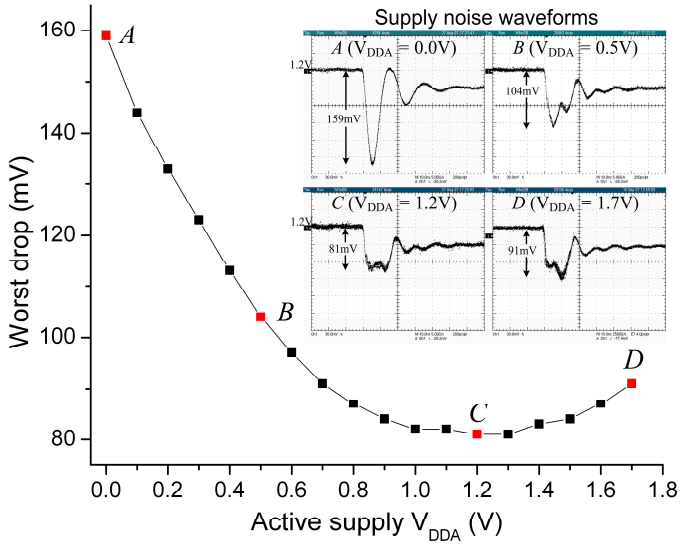

Figure 22.9.5: Measured regulated worst drop as a function of V_{DDA}.

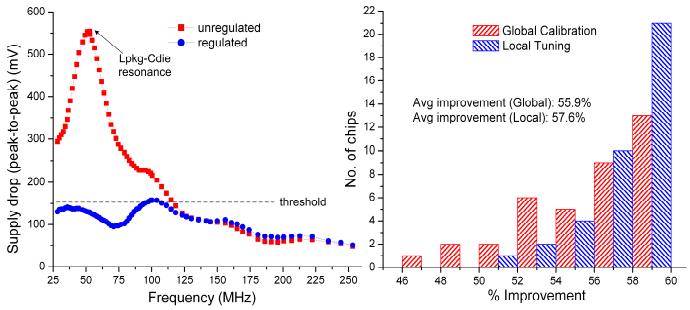

Figure 22.9.6: Measured unregulated/regulated peak-to-peak noise vs. frequency and distribution of percentage improvement using global calibration or local tuning.

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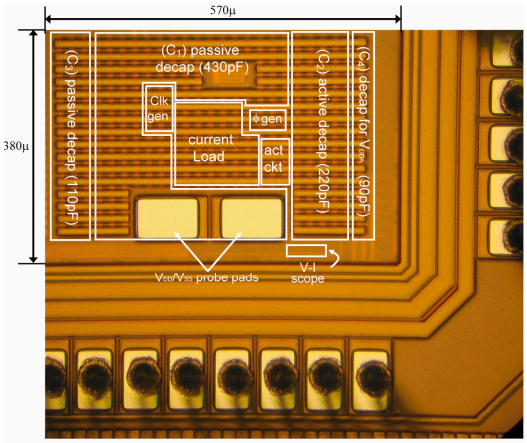

Test case	Pad Allocation				Decap Allocation			
	V_{DD}	V_{SS}	V_{DDA}	Total	Passive (C_p)	Active (C_a)	V_{DDA} decap	Total
Unregulated	3	3	0	6	760pF (C_1+C_2+C_3)	-	-	760pF
Regulated	2	3	1	6	430pF (C_1)	220pF (C_2)	90pF (C_4)	740pF

Figure 22.9.7: Die micrograph and chip implementation details.

