True Random Number Generator With a Metastability-Based Quality Control

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***Abstract*—We present a metastability-based True Random Number Generator that achieves high entropy and passes NIST randomness tests. The generator grades the probability of randomness regardless of the output bit value by measuring the metastable resolution time. The system determines the original random noise level at the time of metastability and tunes itself to achieve a high probability of randomness. Dynamic control enables the system to respond to deterministic noise and a qualifier module grades the individual metastable events to produce a high-entropy random bit-stream. The grading module allows the user to trade off output bit-rate with the quality of the bit-stream. A fully integrated true random number generator was fabricated in a 0.13 μm bulk CMOS technology with an area of 0.145 mm^2.**

***Index Terms*—Entropy, random noise, random number generation.**

I. Introduction

RANDOM number generators are essential components for a wide range of applications. In security systems they provide the secret keys or tokens for authentication and encryption. They are also applied to various problems in simulation software. Random number generators that use a physical source of randomness are commonly called True Random Number Generators (TRNG). Solid-state devices have innate sources of randomness such as thermal noise and telegraph noise. However, due to the nature of these sources, their input referred magnitudes are very small. Hence, TRNGs are very sensitive to undesired deterministic noise sources including power supply noise, temperature variation and, in extreme cases, deliberate malicious noise attacks. In addition, process variation is a static source of variation that sets a limit on the control range and operation of the TRNG. We present a metastability-based TRNG that has the ability to counteract process and temperature variations and can respond to deterministic noise events. It can also grade the quality of the output bit-stream according to the actual probability of randomness of the system, regardless of the output value.

Many different variations of TRNG designs have been presented in the past [1]–[4], using various methods to extract physical sources of randomness. The design presented in [1] uses an oscillator sampling technique with an amplified thermal noise source. A TRNG that harvests random telegraph noise of single oxide-traps and incorporates redundancy for added robustness is presented in [2]. A TRNG that combines different extraction methods and combines their outputs is presented in [3]. In general, TRNGs use feedback mechanisms to control their operating point. A metastability-based TRNG that uses a feedback loop to set a zero to one ratio of 50% was presented in [4]. In addition, TRNGs have reported the use of correctors to eliminate correlation and long runs of zeros and ones in the output bit-stream [2], [4]. The von Neumann [5] and XOR correctors are the most common designs utilized for these purposes. The post processing performed by these correctors operates directly on the bit values of the bit-stream.

The proposed TRNG method uses a metastable system to generate individual bits that result from the effect of thermal noise. The innovation of the proposed TRNG method is that control of the metastable operation is performed without observing the value of the generated output bits. Instead, the resolution time of each metastable event is recorded, regardless of the zero or one outcome. The resolution time is defined as the time that it takes the system to resolve from the metastable point to one of the two stable states, either a value of zero or one. The original noise level when the system was metastable is determined using the measured resolution time and utilizing this data the probability of having a significant dominant amount of random noise is computed. This allows the control module to grade the quality of the output bit-stream and to tune the system for the maximum probability of randomness. Furthermore, the proposed method allows the user to trade-off between the quality of the bit stream and the bit production rate.

In this work, we present a test chip with a fully integrated TRNG fabricated in a 0.13 μm 8-metal-layer bulk CMOS technology. It is implemented in an area of 0.145 mm^2 and consumes 1 mW of power. Randomness and entropy tests that were performed on this new design demonstrate the quality of the output of the TRNG. The impact of process and temperature variations is reported for 26 chips and testing results of the metastability-based feedback control are presented.

The remainder of this paper is organized as follows. In Section II we revisit some fundamental concepts of metastability that are the basis of operation for the TRNG. We present the implementation and circuit operation in Section III. The measured results, including analysis of the entropy of the system, impact of variation and the randomness tests, are presented in Section IV. Conclusions are given in Section V.

II. Metastability and TRNG Fundamentals

In this section, we review basic concepts of metastability that are fundamentally necessary to understand the method used by

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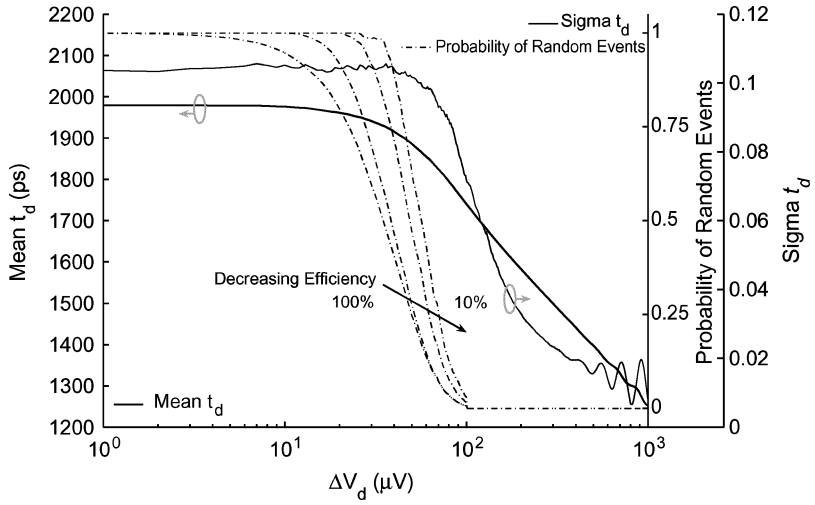


Fig. 1. Statistical properties of $t_d(\overline{t_d},\ \sigma t_d)$ and probability of a random event for varying efficiencies (100%, 70%, 40%, 10%). The arrow indicates the direction of decreasing efficiency.

the TRNG. We then describe the basic operating properties of the metastable-based control and grading.

The main component of the proposed TRNG is a latch that is biased in the metastable region. In this state, the final output of the system will be determined by the random noise of the devices. However, if the initial latch voltages are not exactly at the metastable point, due to mismatch introduced by process variation or external deterministic noise, the latch will have a deterministic output value. The key observation of our method is that the probability of randomness of a metastable event can be determined by measuring the time it takes the latch output to resolve. In the metastable region, the resolution time (t_d) can be modeled as $t_d = \tau_r \cdot \ln(K_f \Delta V_f / \Delta V_i)$, where τ_r and K_f are device and circuit dependent constants, ΔV_f is the final voltage difference of the latch nodes and ΔV_i is the initial voltage difference from the metastable point [6]. The metastable point is defined as the pair of voltages of the two latch nodes that cause the system to be metastable in the absence of noise. This point depends on the mismatch of the devices and the difference in the output loading of the nodes [7], [8]. However, in the presence of noise, the system is biased with some initial voltage difference, ΔV_i, from the exact metastable point. ΔV_i has two components: a deterministic component, ΔV_d, which captures external noise, power supply noise, and other non-random events; and the thermal random noise V_n. By observing t_d, it is possible to compute the original voltage differential ΔV_i and determine the probability that the final metastable outcome is dominated by thermal noise. A metastable event is considered to be dominated by the thermal random noise when the magnitude of the random noise is higher than the deterministic noise, regardless of the direction of resolution.

The dependence of t_d to ΔV_d is illustrated in Fig. 1, where sets of metastable events are simulated with different values of ΔV_d for a system that contains a Gaussian random noise source. For these runs, the value of ΔV_f is set as a constant to half the power supply voltage. For each ΔV_d a set of 1000 events are simulated. In an ideal system without noise, it would be expected that as ΔV_d approaches 0, the mean of $t_d(\overline{t_d})$ tends to infinity and sigma of $t_d(\sigma t_d)$ to 0. However, in a system with noise as ΔV_d is reduced, the $\overline{t_d}$ and σt_d increase and finally saturate to a value that only depends on the amount of noise in the system, as shown in Fig. 1.

In our simulations, the magnitude of ΔV_d and V_n are compared for each individual metastable event to determine which controlled the final bit outcome. This enables us to calculate the probability of generating a bit where the outcome is determined by the random noise as opposed to the deterministic component. In Fig. 1, when $\Delta V_d \gg V_n$, the probability of obtaining a random bit is low because the system is dominated by the deterministic noise, therefore, the $\overline{t_d}$ and σt_d are also small. As ΔV_d is reduced, the probability of random outcomes as well as the value of $\overline{t_d}$ and σt_d increase as the system becomes dominated by thermal noise. It is therefore possible to tune a latch into the metastable region by evaluating the statistics of t_d. Using individual measurements of t_d in a feedback control loop would cause the output bit-stream to be highly correlated. For that reason, the determination of whether deterministic or random thermal noise controlled the final outcome must be performed statistically since the noise is a random variable.

In addition to using statistical analysis to tune the system into metastability, the t_d values of individual metastability events are used to grade the quality of the output bits when $\Delta V_d \approx V_n$. Based on the range of generated t_d values, the user can set a threshold that determines the minimum bound for a bit to be considered random. The t_d threshold can be recomputed to respond to different environmental PVT conditions if needed. By adjusting the t_d threshold, the user can also set a trade-off between bit-production rate and bit-stream quality. Furthermore, this grading increases the sensitivity of the probability of a random event to changes in $\overline{t_d}$. As shown in Fig. 1, as the t_d threshold is increased and the system's efficiency (defined as the ratio between the post-filtering bit-rate and the maximum achievable bit-rate without filtering) is reduced, the randomness of the events as a function of ΔV_d is shifted toward the right. The probability of a random event is plotted for efficiencies of 100%, 70%, 40%, and 10% as indicated by the arrow.

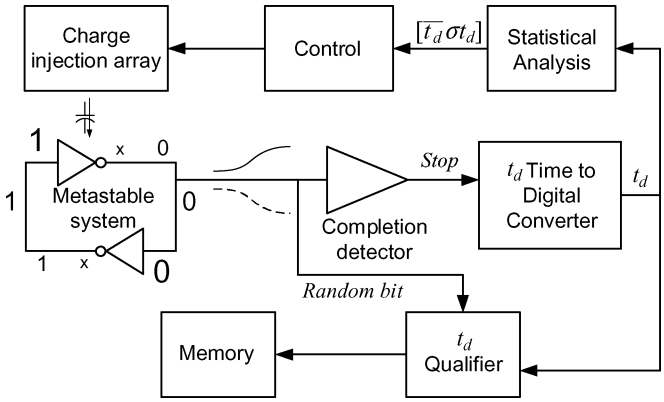


Fig. 2. True random number generator block diagram.

A very important application of the quality control of the bits based on their corresponding t_d occurs in extreme cases when the TRNG is tampered with or in an environment with large magnitudes of external deterministic noise. In such an environment, the expected t_d for the generated bits is small, causing the grading system to drop a large fraction or all produced bits. This will prevent the user from using bits that have been compromised by deterministic events. In contrast, a TRNG which uses a corrector that manipulates the output bits would not have any information for the user on the quality of the bits produced.

III. Circuit Implementation

In this section, we provide a more detailed description of the modules for the TRNG. The block diagram of the TRNG is shown in Fig. 2. The system is divided into three major components.

1) The random bit generator includes the metastable system, completion detector and a time-to-digital converter (TDC). It operates each cycle and produces the random output bit as well as its associated digital value of t_d.
2) The control system consists of a module that extracts the statistical information for a set of t_d measurement samples, 128 for this TRNG, and the control module that determines the feedback value to tune the metastable latch.
3) A grading module compares the generated output bit t_d with a predefined t_d threshold and stores the bit in memory if the generated t_d is greater than the threshold.

The metastability latch, shown in Fig. 3, is the key component of the TRNG. This latch is based on two cross-coupled inverters that have been sized for equal rise and fall delays, resulting in an equal metastable voltage for both inverters (i.e., $V_M \approx V_q \approx V_{qb}$). The latch sizing and maximum load are constrained such that the bandwidth of the region of operation lies where Thermal noise dominates over Flicker noise. However, the bandwidth of the region of operation must not be over constrained to avoid difficulty in meeting the resulting resolution time for the TDC. The latch has switches (M5–M9) that are used to bias and turn it on/off. The steps utilized to produce one random bit are illustrated in Fig. 4.

1) *Reset* the latch by collapsing the virtual nodes V_{ddx} and V_{ssx} to V_{intref}, a value close to $V_{dd}/2$, by setting $Bias = 1$ and $Start = 0$.

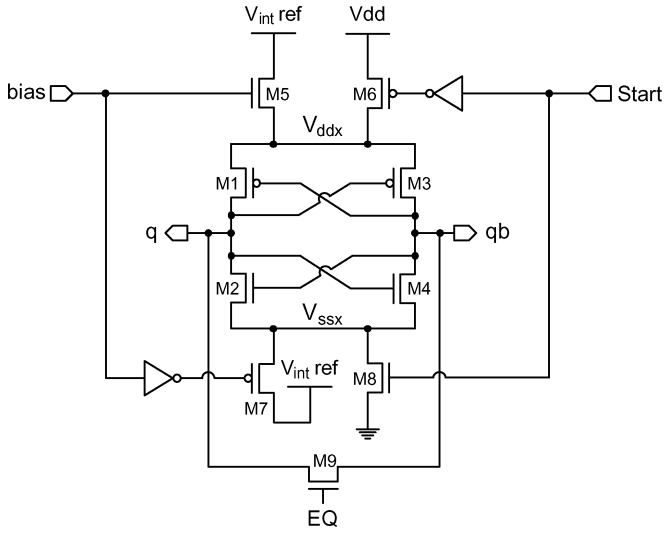


Fig. 3. Metastable latch circuit.

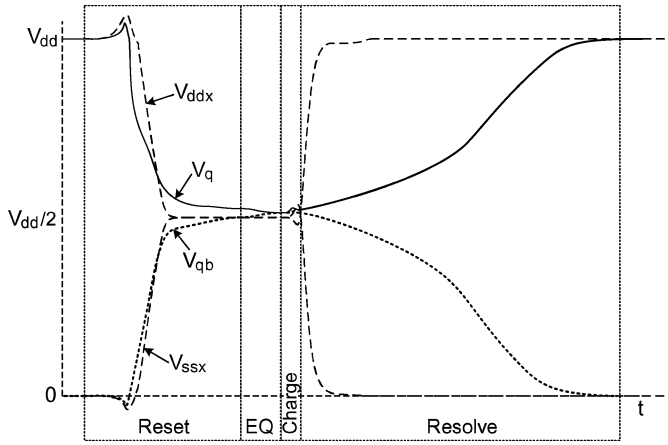


Fig. 4. Single bit generation sequence for a metastable event.

2) *Equalize* the output nodes by asserting the EQ signal.
3) Release EQ and induce charge on node q as programmed by the control module.
4) Activate the latch by restoring the virtual nodes V_{ddx} and V_{ssx} to full V_{dd} by asserting $Start$ and releasing $Bias$. The latch output *resolves* to its final state and the $Stop$ signal is generated.

In this TRNG each bit generation cycle takes 20 ns, four cycles of a 200 MHz clock.

A TDC is used to determine t_d by measuring the time difference between the $Start$ and $Stop$ signals (Fig. 5). This module must satisfy two basic requirements: first it must have a fine resolution to enhance the control of the TRNG based on t_d; second it must have a wide range to measure either very fast deterministic or very long metastable events. The resolution and range are technology and circuit dependent constraints. At a certain resolution, increasing resolution further does not provide any additional accuracy in the statistics of t_d, thus relaxing the implementation complexity of the TDC design. For this TRNG in particular, the resolution was chosen to be 50 ps after performing extensive statistical simulations. The TDC is composed of a fine thermometer encoded counter with a 50 ps resolution and a

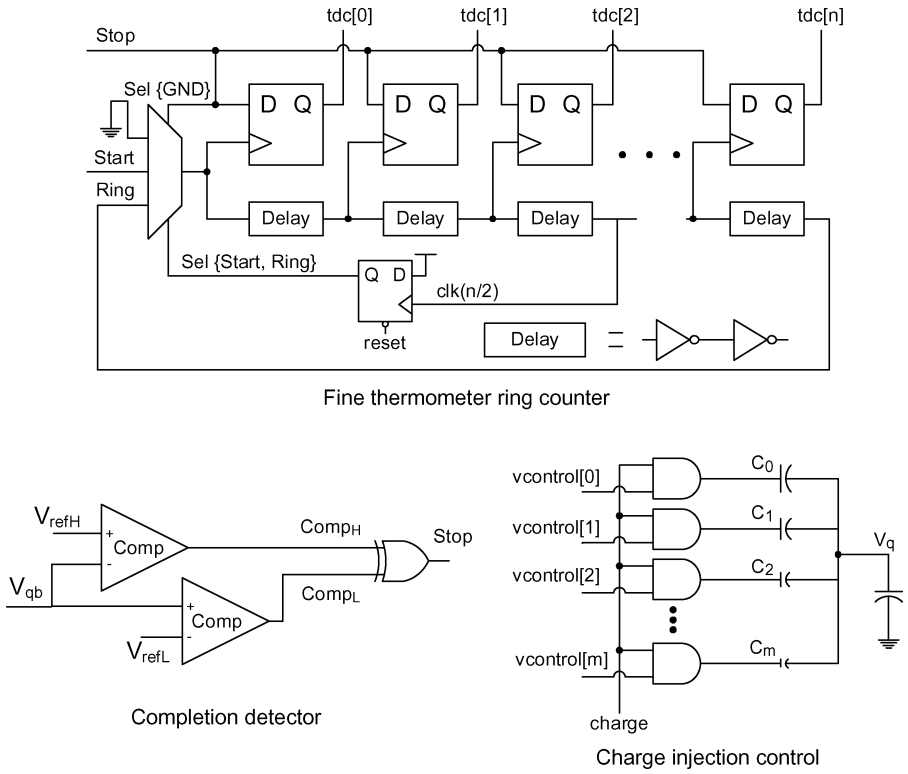


Fig. 5. t_d time-to-digital converter (TDC), completion detector and charge injection circuit.

coarse counter that extends the range to 20 ns. The fine counter contains an array of flip-flops clocked by delayed versions of the $Start$ signal that sample the $Stop$ signal in discrete times, producing a thermometer code. This thermometer code is decoded to generate an absolute measure of time in terms of TDC units. Two inverters, sized for equal fall and rise times, were used as the delay elements for the $Start$ signal. In order to decouple the system from the main clock signal and avoid the clock distribution variation from affecting the delay measurement, the delay line of the TDC is connected as a ring and the coarse counter is incremented every time the $Start$ pulse propagates through the ring. The $Stop$ signal is generated using a pair of complementary differential comparators as illustrated in Fig. 5. Reference voltages are set to 25% and 75% of V_{dd}, 300 mV and 900 mV, respectively. It can be observed that these analog comparators can be replaced with digital skewed inverters, thus saving area, power and the generation of the reference voltages V_{refL} and V_{refH}.

The TRNG has a control system that monitors the t_d of the bits produced and keeps the system in a state where the probability of a random event is high. The control algorithm's goal is to maximize the $\overline{t_d}$. The control module does not act in a bit-production cycle basis, but gathers a set of 128 t_d samples and generates the statistics of mean and sigma of t_d. A control iteration occurs when a new set of statistical data is produced and a new configuration for the feedback loop is generated. The same control configuration is used for a set of 128 bit-generation sequences.

The main component of the feedback loop is a charge injection array that biases the node q of the latch, as described in step (3) of the random bit generation sequence. It is designed using

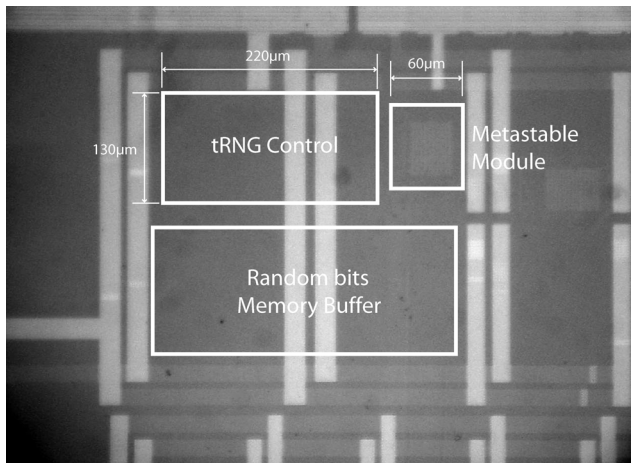


Fig. 6. TRNG test chip die photo. Fabricated in 0.13 μm bulk CMOS technology.

an array of capacitors that are conditionally charged via a control word programed by the control algorithm (Fig. 5). The capacitors are implemented using overlapping metal structures in metal layers M4 and M5. Since this structure is very sensitive to external noise, shields in M3 and M6 are introduced. The capacitor values range from 0.25 to 100 fF, which translates to control of the induced voltage on node q with a resolution of 10 μV and a 16 mV range.

An 8 kb memory was used as a buffer to store the generated random bits and their corresponding t_d. In this test chip, the t_d qualifier shown in Fig. 2 was implemented externally in software. A comparator with a programmable reference can serve the same purpose in hardware.

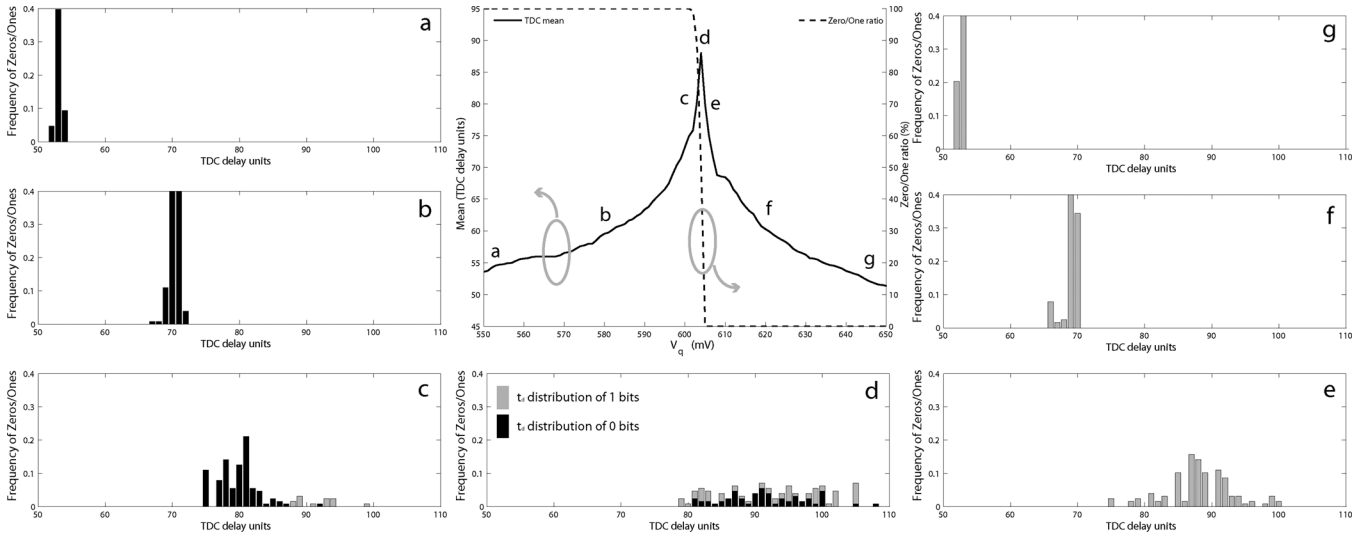


Fig. 7. Measured t_d distributions for different bias points (a–g).

A scan chain was implemented in the test chip to scan out the contents of the output memory buffer. This operation is performed every control iteration to store the random bits externally. The calculation of the mean and the control algorithm are also performed externally. These operations however can be implemented on-chip by a dedicated arithmetic unit or by a CPU. Unfortunately, in this test chip, the serial scan chain limits the practical throughput of the system to 200 kb/s. In theory, however, if a high speed bus was implemented, the maximum bit-rate of the TRNG would be 50 Mb/s.

The TRNG was fabricated in a 0.13 μm bulk CMOS technology with 8 metal layers. The die photo is shown in Fig. 6. The TRNG, including a 8 kb output memory buffer, is implemented in an area of 0.145 mm^2.

IV. Experimental Results

In this section, we present measured results from the fabricated test chips. An analysis of the t_d distributions and the output bit-stream randomness are included. In addition, the response of the system to process and temperature variations and external noise is presented.

Fig. 7 shows the mean of the measured distributions of t_d and the associated values of the random bits for sets of 128 samples as the injected charge is swept. The center figure shows the mean of t_d as the deterministic control voltage is swept. The different letters (a–g) show representative points in the sweep. Each bar graph corresponds to one of the indicated operating points. The t_d frequency for output bits that are equal to 0 are plotted in black. The analog is shown for bits equal to 1 in gray. As expected, biasing the system well below (a–c) or above (e–g) the metastable point, which fell at approximately 604.1 mV, results in bits with small t_d values and a small observed t_d variation. The output bits are either all zeros or all ones depending on the side of the metastable point at which the system is biased. However, as the system approaches the metastable point $\overline{t_d}$ and σt_d increase rapidly. At the metastable point, indicated by (d), $\overline{t_d}$ and σt_d are maximum and the ratio of zeros to ones in the output bit-stream reaches 50%. It is important to note that the rapid increase in $\overline{t_d}$ allows for very good control feedback.

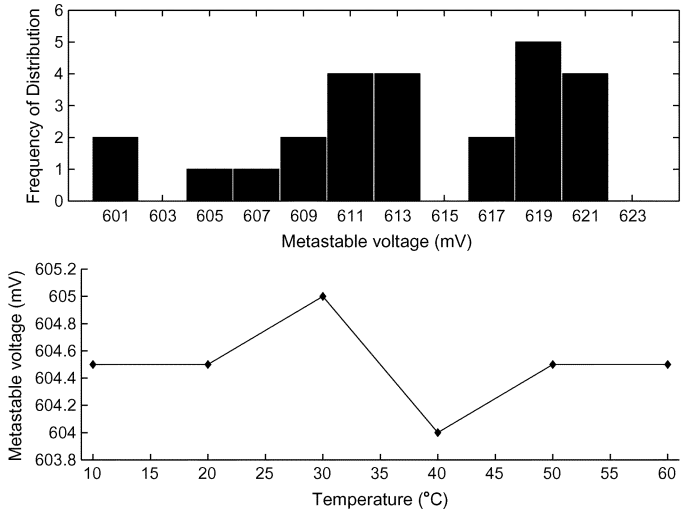


Fig. 8. Metastable point across process variation in 26 dies and temperature variation from 10 °C to 60 °C.

To measure the robustness of the design, 26 chips were tested to find the variation in the metastable voltage (Fig. 8). The mean metastable point was 614.71 mV with a standard deviation of 6.28 mV. To analyze the effect of temperature variation, measurements of the metastable point were performed for one chip across a temperature range of 10 °C to 60 °C. The maximum metastable point variation was 1 mV. In addition, the statistical behavior of t_d across the measured temperature range matched very well with that at room temperature. The control system has the required range to compensate for the temperature variation and can be designed to account for larger process variation.

Fig. 9 shows the operation of the control algorithm for the test chip as it responds to deterministic noise. $\overline{t_d}$ is plotted as the configuration of the control module is changed to maximize the value of $\overline{t_d}$. The time axis units are set to control iteration cycles. The system locks into metastable operation after iteration

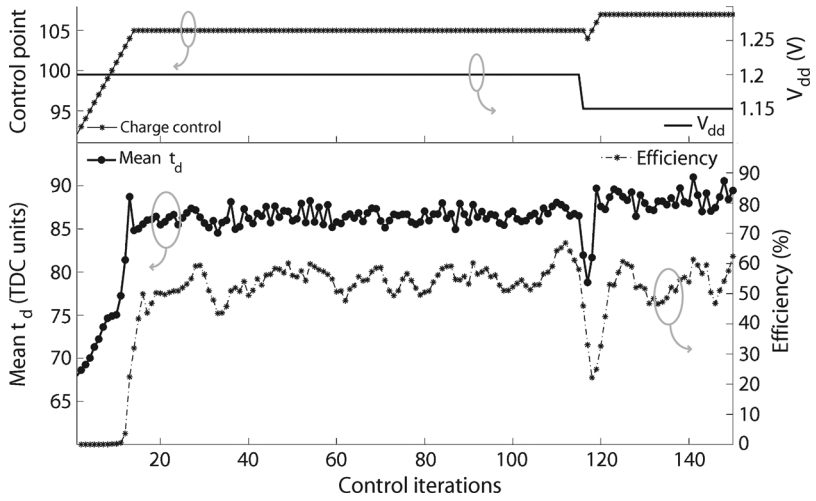


Fig. 9. Dynamic control system response to a voltage droop.

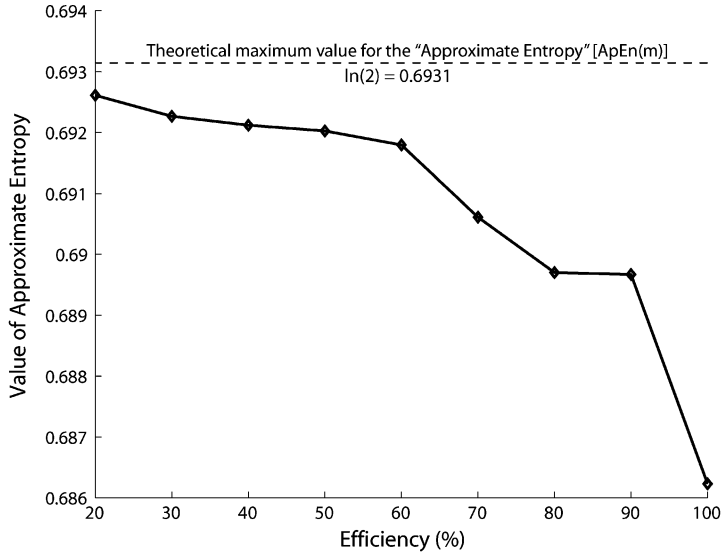
10. At iteration 115, a 50 mV supply voltage droop is induced in the power supply as shown by the V_{dd} trace. The $\overline{t_d}$ is reduced dramatically by more than 5 TDC-units as the metastable point is shifted due to the induced noise. The system responds in 10 iterations by adjusting the configuration of the control and stabilizes with a new maximum of $\overline{t_d}$. The new stable operating point has a higher t_d due to the degradation in the drive strength resulting from the voltage droop. The efficiency of the system when filtering with a constant t_d threshold tracks very well to the behavior of t_d showing that more filtering is needed for events that have lower values of t_d.

The random bit-stream that is obtained when operating the TRNG at stable periods of operation has been subjected to several tests to analyze its entropy and check if it contains the expected properties of a true random source. The random bits were generated by the TRNG at its maximum clock frequency of 200 MHz and stored in the 8 kb on-chip memory buffer. At the end of a control iteration cycle, the contents of the memory buffer (random bits and t_d) were extracted using the low frequency scan chain. The tests were performed using varying levels of system efficiency which were controlled by setting different t_d threshold values for the module that grades the output bits. For the tests, the t_d filtering threshold was swept from 75 to 96 TDC-units.

The entropy of the system was measured using the Approximate Entropy measure $(\mathrm{m} = 10)$ as used by the "Approximate Entropy Test" contained in the National Institute of Standards and Technology (NIST) tests [9]. In Fig. 10, it is shown that the entropy of the system is very high. When the efficiency of the system is reduced, the entropy increases further. This supports our expectation that metastable events that have a higher resolution time have a higher probability that the bit was generated by a random noise event. In a similar way, if deterministic noise is induced into the system under a malicious attack, the grading module would filter out the bits that are caused by those events, since their associated t_d values would be low. However, it is possible that under normal operating conditions, a random noise event could generate a large input referred voltage that causes the metastable latch to resolve very quickly. This means that the grading module would drop bits that contain higher probabilities of randomness. This case, although unfortunate, is more acceptable than using output bits that have been induced by deterministic noise or malicious tampering.

The TRNG output bit-stream was finally tested for properties of randomness using the NIST tests shown in Fig. 10. The level of significance used for all the tests was $\alpha = 0.01$. Sets of 100 sequences of 128 bits each were used for the tests: Frequency, Block Frequency (block size of 32), Cumulative Sums and Runs. The minimum passing rate proportion for the above mention sample size and significance level is 0.96. The criteria for the uniformity of the $Pvalues$ is $Pvalue_T \geq 0.0001$. A passing label is given for tests that fulfill the two requirements of uniform $Pvalues$ and passing rate proportionality. The Spectral DFT, Rank and Linear Complexity (block size of 500) tests were performed for a single sequence of 1 M bits. The success of a test is indicated when the $Pvalue \geq 0.01$ for a significance level of $\alpha = 0.01$. Due to area constraints, the amount of on-chip storage was limited to 128 bits per control iteration. The 1 M bit sequence was created by concatenating 128-bit sequences that were individually scanned out after each control iteration. It should be noted that since the 128-bit sequences were created at different time instances, the characteristics of randomness between the bits after concatenation could be different than that if a 1 M bit sequence was generated in a single control iteration.

The results from the randomness tests show that the TRNG failed some of the tests at the highest efficiency. This behavior was expected since at the maximum bit-rate, some bits would have been the product of the deterministic noise found in the system. It is at this point that previous true random number generators have had the need to include a corrector to modify the output bits by directly manipulating the bit values. In our proposed approach, we lower the efficiency of the system by grading the quality of the individual bits and as a result we pass the tests that had previously failed. This filtering was based not on the bit values, but on the properties of the event that generated them.



Efficiency (%)	NIST Randomness Tests						
	Frequency	Block Frequency	Cumulative Sums	Runs	Spectral DFT	Rank	Linear Complexity
100	pass	pass	pass	fail	fail	pass	pass
90	pass	pass	fail	fail	fail	pass	pass
80	pass	pass	pass	fail	fail	pass	pass
70	pass	pass	pass	fail	fail	pass	pass
60	pass	fail	pass	fail	fail	pass	pass
50	pass	pass	pass	fail	fail	pass	pass
40	pass	pass	pass	fail	fail	pass	pass
30	pass	pass	pass	fail	fail	pass	pass
20	pass	pass	pass	pass	pass	pass	pass

Fig. 10. Approximate entropy measure and NIST randomness test results for different system efficiencies.

V. Conclusion

A fully integrated 0.13 μm True Random Number Generator has been implemented and tested. The metastability-based control is capable of producing random output bits with high entropy. In addition, the output stream does not need a corrector to pass NIST randomness tests. This is achieved by grading individual bits, not based on logic values, but on the resolution times of the metastable events that produced them. The dynamic control module that tunes the latch into the metastable region responds for both process and temperature variations, as well as external noise sources.

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