

Designing Robust Ultra-Low Power Circuits

Dennis Sylvester, Scott Hanson, Mingoo Seok, Yu-Shiang Lin, David Blaauw
University of Michigan, Ann Arbor dennis@eecs.umich.edu

Ubiquitous sensing systems, with a single node or thousands of nodes, are quickly becoming a viable technology option with the advancement of circuit and sensor design. In such a system, the most basic building block is an inexpensive sensor node with data processing and storage, off-chip communication, sensing elements, and a power source all linked within a robust package ideally with a volume on the order of 1mm^3 . The sensor node must have a lifetime on the order of months or years. Due to the limitations of power sources, the most pressing implication of this lifetime requirement is that the power consumption of all components must be minimized.

Due to the quadratic dependence of switching energy on supply voltage V_{dd} , dramatic energy reductions can be achieved in digital logic by reducing V_{dd} . It has long been known that CMOS circuits continue to function with V_{dd} well below the V_{th} , so aggressive voltage scaling into the subthreshold regime ($V_{dd} < V_{th}$) is possible with careful design. Recently there has been significant progress in designing very low voltage processors and memories [1-3]. Much of this work has focused on improving active power consumption or energy efficiency (measured in pJ per instruction). For example, [1] showed an 8-bit processor with 1.5kb instruction memory and 1kb data memory in $0.13\mu\text{m}$ CMOS. The processor targets mobile sensor applications where energy consumption is the primary metric and performance is a secondary concern. Logic blocks were synthesized using a carefully chosen limited set of low fan-in CMOS standard cells, and the memories were implemented using a robust latch-based memory [2]. Energy consumption was found to be minimized at $V_{dd} = 350\text{mV}$ at $3.52\text{pJ/instruction}$ running at 354kHz , representing nearly an order of magnitude improvement in energy efficiency versus normal superthreshold operation. The presence of an energy minimum [4] is an important concept for low voltage designers. Despite a reduction in switching energy with V_{dd} , delay increases exponentially at low V_{dd} causing leakage energy ($V_{dd} \cdot I_{leak} \cdot t_{delay}$) to increase and eventually create an energy minimum.

While energy is dramatically reduced at low V_{dd} , subthreshold operation suffers from an exponential sensitivity to process- and temperature-induced V_{th} variations. Previous work has shown that random V_{th} variability caused by random dopant fluctuations (RDF) can be addressed by increasing gate sizes and by increasing the number of logic gates between sequential elements [5]. Systematic V_{th} variation is also of concern but can be addressed more directly by applying body

biases to compensate for systematic PFET/NFET mismatch. The processor from [1] uses body bias to reduce variability. Due to the large sensitivities, modulating V_{th} with body bias is more effective at ultra-low V_{dd} than normal operation and frequency variations are eliminated with the application of a body bias while energy variations are reduced significantly.

Many applications requiring extremely low power also exhibit low duty cycles, implying that standby mode power consumption is critical. A 30pW standby mode processor is demonstrated in [6]; key innovations include a novel approach to power gating, data memory compression, a new low leakage memory cell and adaptive leakage management in data memory (Figure 1). The design is implemented in a mature $0.18\mu\text{m}$ process – this node was chosen specifically to achieve ultra-low standby mode power while also providing the same footprint (1mm^2) as a thin-film battery that will be used to power the chip for multi-year lifetimes in an implantable medical device. The authors of [7] more rigorously analyze technology selection for low-voltage designs and show that for many sensor-type applications older technologies are preferable.

Several key issues must be explored in future work in this area. For logic and memory design, improving performance and attacking variability merit further attention, along with leakage reduction in memories (Figure 1). The power consumption of off-chip communication is also problematic. Low power radio design will likely dictate the viability of ubiquitous sensing systems. Additionally, the power budget for a ubiquitous computing element is ultimately limited by the power source, so the design of on-chip power sources (e.g., on-chip battery or energy scavenging circuits) is extremely important. Also, power management in the form of efficient voltage conversion has not been sufficiently studied. The future of ubiquitous computing systems will rely on innovation in each of these areas and on continued exploration of the low voltage design space.

References

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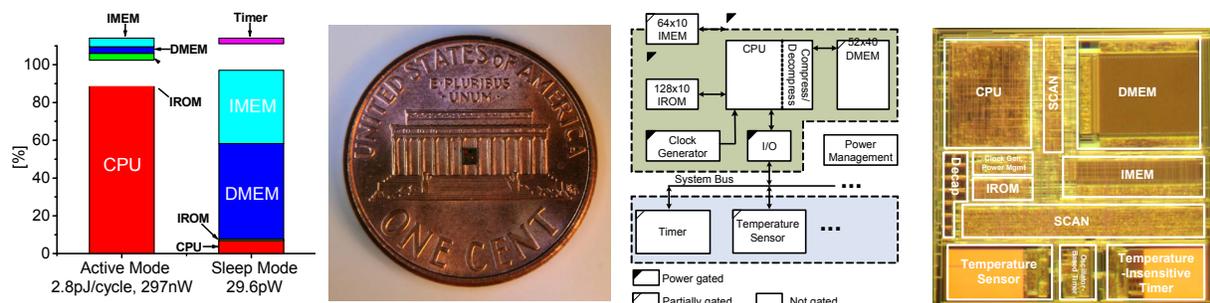


Figure 1. Phoenix processor active and sleep mode power breakdowns; die size comparison; overall system architecture; die photo [6].