Circuit Techniques for Suppression and Measurement of On-chip Inductive Supply Noise

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ABSTRACT

Increasing power consumption and clock frequency have significantly exacerbated the Ldi/dt drop, which has emerged as the dominant fraction of the overall power supply drop in high performance designs. We present the design and validation of a high-voltage, charge-pump based active decoupling circuit for the suppression of on-chip inductive power-supply noise. We also propose a low-power, high-resolution, digital on-chip oscilloscope technique, based on repetitive sampling, for measurement of high-frequency supply noise. The proposed circuits were implemented and fabricated in a 0.13μm CMOS process. Measurement results on the prototype demonstrate 48% and 53% reduction in power supply noise for rapidly switching current-loads and during resonance, respectively. On-chip supply noise is measured using the proposed on-chip oscilloscope and the noise waveforms are compared with those obtained from a traditional supply noise monitor and direct on-chip probing using probe pads.

1. INTRODUCTION

Aggressive technology scaling has exacerbated inductive (Ldi/dt) supply noise, impacting the robustness of power delivery networks. Ldi/dt is further aggravated by commonly used power reduction techniques such as power/clock-gating of macro blocks and frequency stepping in dynamic voltage scaled designs. Traditionally, decoupling capacitance or passive decap connected between V_{DD} and V_{SS} metal lines has been effectively used to suppress supply noise transients. However, the area and the leakage overhead places a limitation on the maximum amount of passive decap that can be added on the die.

Methods for IR-drop mitigation, such as increasing the on-chip power grid metallization are less effective in reducing Ldi/dt drop which is primarily caused by package inductance. This has given rise to an urgent need for the suppression of inductive noise in power distribution networks in the presence of large load-current transients. Active supply voltage regulation techniques employ circuits to enhance the amount of charge transfer to-and-from the power supply network during excessive supply-voltage fluctuations. The objective of these approaches is to reduce the supply drop for the same amount of explicit decoupling capacitance or to minimize the total decoupling-capacitance area for the same worst-case supply drop.

Several circuits have been proposed which enhance the charge transfer to or from decaps to suppress supply noise transients. In [1], a Miller-coupling based capacitance enhancement technique was proposed to reduce crosstalk between digital and analog regions on a die. A switched-capacitor circuit with two decap-banks switched between series and parallel configurations was proposed in [2]. In [3], a band-pass filter is used to detect supply noise resonance and an artificial shunt load is periodically switched on and off to dampen the resonance. A supply regulation technique using only nominal voltage supplies was presented in [4]. In [5], a shunt high voltage supply is connected to the regular power grid when power-gated logic blocks wake up from the sleep state. Several adaptive frequency-management techniques [6] have also been proposed to compensate for supply transients. These techniques employ supply-drop monitors at various locations on the die and the frequency of operation is altered to compensate for fluctuations in the power supply. In [7], the use of controlled incremental frequency changes to alleviate inductive noise in dynamically voltage scaled microprocessors was explored. In addition to these, several micro-architectural control techniques [8] such as selective issue, pipeline throttling and selective wake-up of clock-gated modules have also been proposed.

In this paper, we present a high-voltage, charge-pump based digital circuit technique for the suppression of inductive supply noise. The proposed circuit detects and suppresses excessive supply voltage fluctuations due to both sudden surges in load or due to excitation of supply resonance. The proposed circuit delivers a significantly larger amount of charge while ensuring that the charge transfer into the V_{DD} network is identical to that out of the V_{SS} network. This eliminates the possibility of any bounce in on-chip V_{DD} and V_{SS} relative to off-chip voltage references which can possibly interfere with the IO operation.

We also propose a power-efficient all-digital on-chip oscilloscope for accurate measurement of high-frequency supply noise. The proposed oscilloscope uses subsampling [9] to repetitively sample the supply noise waveform, capturing its time-shifted snapshots, each snapshot consisting of 38 sample points with 50ps resolution. The snapshots are then combined off-chip to reconstruct the complete supply noise waveform. The proposed circuit achieves a bandwidth of 20GS/s and is much more power efficient than analog supply drop monitors.

The proposed circuits for supply noise suppression and measurement were integrated in a prototype fabricated in a 0.13μm, triple-well CMOS technology. Measurement results on the prototype demonstrate 48% and 53% reduction in power supply noise during rapidly switching loads and during resonance, respectively. The on-chip supply noise waveforms, measured using the proposed on-chip oscilloscope are compared with those obtained from a traditional supply noise monitor and direct on-chip probing using probe pads. The measurements show good correlation in both the IR and the Ldi/dt drops.

The remainder of this paper is organized as follows. Sections 2 and 3 present the description of the supply noise suppression and measurement circuits, respectively. Section 4 presents the details of the prototype implementation and measurement results, and conclusions are drawn in Section 5.

2. SUPPLY NOISE SUPPRESSION

Figure 1(a) shows a simplified model of an unregulated power delivery network. The impedance of the power and ground distribution networks is modeled as a series combination of lumped elements, L_{VDD}-R_{VDD} and L_{VSS}-R_{VSS}, respectively. The total amount of non-switching as well as explicitly added on-die decap is represented by the lumped capacitance C_P. A time-varying current

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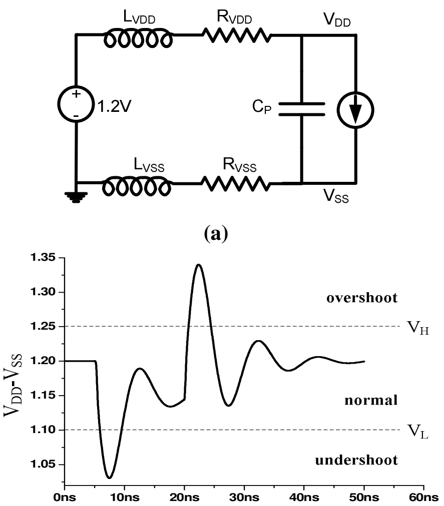


Figure 1. A simplified power delivery model (a) and a typical supply noise waveform with supply voltage thresholds (b).

source models the switching current of all the logic blocks in the chip. Figure 1(b) shows the unregulated supply voltage waveform with undershoot and overshoot supply voltage thresholds, V_L and V_H, respectively. V_L and V_H can be determined based on the performance constraints on the design. Three regions of operation: *normal* ($V_L<V_{DD}<V_H$), *undershoot* ($V_{DD}<V_L$) and *overshoot* ($V_{DD}>V_H$), are defined based on the amplitude of supply noise.

Figure 2 shows the schematic of the proposed supply noise suppression circuit technique. The proposed circuit employs decap banks, C_A, which store a higher than nominal supply voltage, V_{DDH}, across their terminals. C_A is connected between V_{DDH} and V_{SS} when the supply voltage is above the undershoot threshold, V_L (S_N=1, S_{UN}=0, S_{OV}=0). When a supply drop below V_L is sensed (S_N=0, S_{UN}=1, S_{OV}=0), T_0 turns off and T_1 turns on, discharging C_A from V_{DDH} to V_{DD}. The amount of charge transferred to the regular grid is $C_A(V_{DDH}-V_{DD})$. An artificial load T_2 is turned on to prevent excessive overshoots (S_N=0, S_{UN}=0, S_{OV}=1), sensed when the supply voltage bounces above the overshoot threshold, V_H.

For implementing the proposed supply-voltage regulation technique, a small portion of the total pads available for V_{DD} are allocated to V_{DDH} such that the total number of used pads is constant. Also, the total available decap-area is split between the passive decap C'_P and the decap bank C_A, while also accounting for the area overhead of the active circuits. The active decap bank, C_A, and transistors T_0 and T_1 are implemented using thick-oxide transistors to alleviate reliability concerns.

For a voltage regulation tolerance of k·Vdd, the proposed circuit results in a decap amplification factor of $0.5+(V_{DDH}-V_{DD})/k\cdot V_{DD}$ as

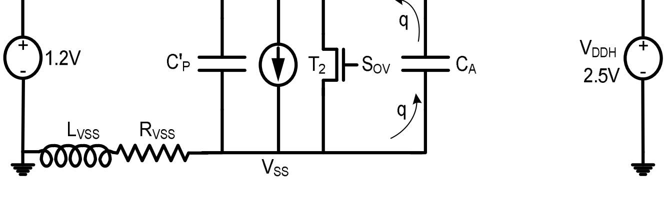


Figure 2. Proposed supply voltage regulation technique.

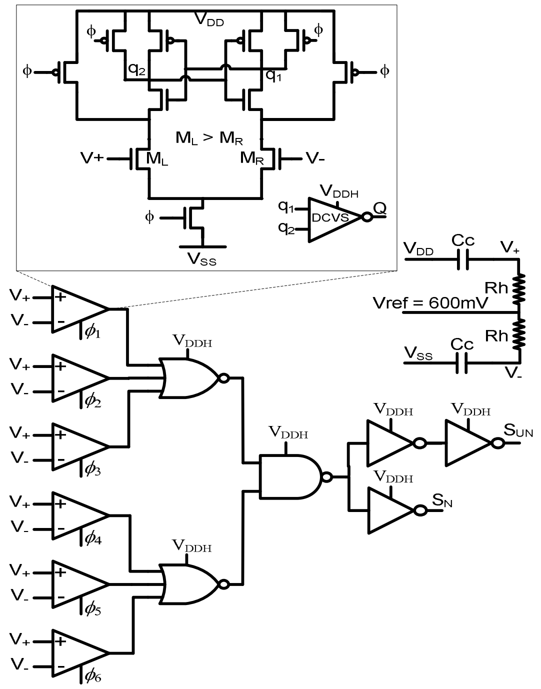


Figure 3. Level shifter and noise undershoot detector circuit.

compared to the use of only passive decap. During supply voltage undershoots, C_A is disconnected from V_{DDH} and forms a loop across V_{DD} and V_{SS}, enabling an equal amount of charge transferred into the power grid and out from the ground grid. This symmetric charge transfer ensures that the regular supplies V_{DD} and V_{SS} do not exhibit any bounce or spikes when switches T_{0-1} are turned on or off. Most of the prior published circuits [1,4,5] are inherently asymmetric and pump more charge into V_{DD} compared to the charge extracted out of V_{SS}, which may cause latch-up or errors in data transfer between different voltage domains.

The control signals S_N, S_{UN} and S_{OV} in Figure 2 are generated by integrated undershoot and overshoot detectors. The detectors are similar in design to the circuits presented in [4]. A level shifter (Figure 3) first couples V_{DD} and V_{SS} noise to a common reference voltage of 600mV. The translated waveforms V_+ and V_- are sampled by a bank of digital comparators clocked at 6 phases (ϕ_1-ϕ_6) of a 3.33GHz clock. The gain transistors M_L and M_R of the comparators are skewed to create thresholds V_H and V_L. The transistors in the comparators are implemented with larger than minimum length to minimize manufacturing variations. The comparator outputs use a DCVS stage for level conversion of outputs from V_{DD} to V_{DDH}. The outputs of the comparators are ORed together and buffered to generate S_N and S_{UN}. The overshoot signal S_{OV} is generated in a similar manner by another bank consisting of 6 clocked comparators. The latency of S_N, S_{UN} and S_{OV} generation was 380ps in simulations.

The next section describes the design of the proposed digital on-chip oscilloscope for supply noise measurement.

3. SUPPLY NOISE MEASUREMENT

Several circuits have been published to measure the on-chip supply noise. Circuits proposed in [10,11] constitute a sample-hold circuit to sample the supply voltage and a V-I converter circuit. The V-I converter circuit consists of a high-conductance transistor to convert the supply voltage samples into current, which is then amplified using a current mirror and transmitted off-chip using a transmission line. Current-based sensing is particularly attractive due to its robustness to coupling noise. However, the use of an analog V-I converter with high gain, followed by current amplifiers makes this technique power inefficient. A-D converters have also been proposed to convert the analog samples of supply noise into a digital code [12] which is then transmitted off-chip. This approach has high area overhead, making it less effective for fine-grained supply noise measurement. An analog circuit that reports whether power supply or ground voltage at the location of comparators within a microprocessor core crosses a pre-defined threshold voltage in every clock cycle was presented in [13].

The analog circuits have large power overhead and their non-linearity may adversely affect the accuracy of the detector in the presence of large fluctuations in supply voltage. To address these concerns, we propose a power-efficient and accurate all-digital on-chip oscilloscope. The proposed oscilloscope samples the supply noise waveform with a high frequency clock and generates its time-shifted snapshots, which are then combined off-chip to reconstruct the original waveform. Since the supply noise fluctuations are non-periodic in nature, the device-under-test (DUT) executes the same test-case repeatedly.

In the proposed on-chip oscilloscope (Figure 4), the measurement process is invoked by asserting a reference voltage, Vref, and the *trigger* signal. In this work, the reference Vref is supplied from off-chip. Since the supply voltage observed by the on-chip devices is V_{DD}-V_{SS}, we are interested in measuring V_{DD}-V_{SS} and not the absolute V_{DD}. Therefore, the reference voltage, Vref, is translated to on-chip V_{SS} using an RC network. Cc is realized using a MIM-cap in order to minimize leakage. The on-chip oscilloscope consists of a coarse delay generator and a fine delay line. The coarse delay generator consists of a counter which asserts the *sample* signal whenever a user-specified (scanned-in) 12-bit count is attained after *trigger* has been asserted high. The fine delay line then generates time-shifted versions of the *sample* signal (s_1-s_{38}), with 50ps resolution. A set of clocked comparators sample the supply noise with the time-shifted versions of *sample* signal, resulting in an effective sampling rate of 20Gbps. The number of comparators is determined by the frequency of *clk* and the chip test time.

A calibration control signal, Δ_{calib}, connects the fine delay line in feedback to form a ring oscillator. During calibration, the divided ring oscillator frequency is measured off-chip and the delay of individual delay element is determined. The output of the clocked comparators is scanned-out as a thermometer code, indicating

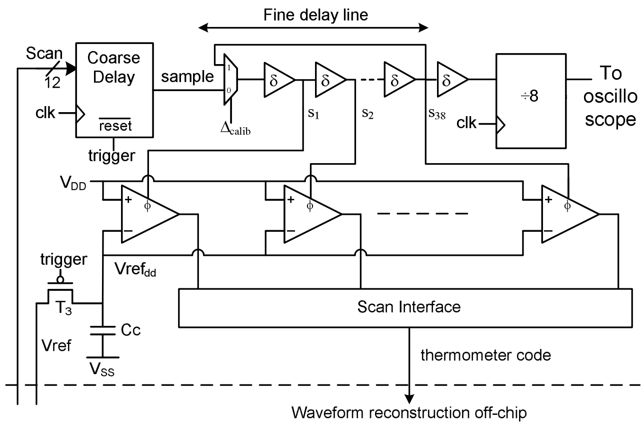


Figure 3. Digital on-chip oscilloscope for noise measurement.

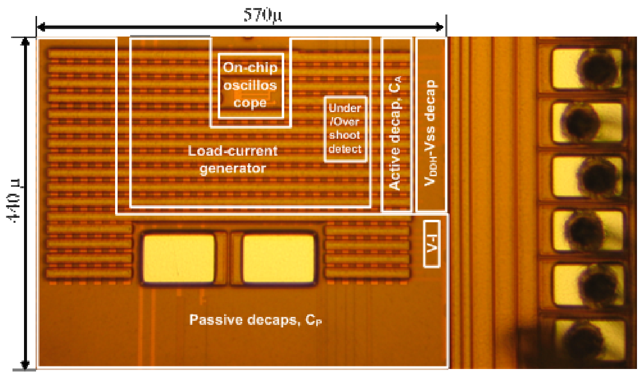


Figure 4. Die Micrograph.

whether each sample of V_{DD}-V_{SS} is greater or less than Vref. The test-case is repeatedly executed on the DUT, with different Vref and coarse delay values and the complete supply noise waveform is constructed off-chip.

The next section presents the implementation details of the prototype and measured results.

4. PROTOTYPE IMPLEMENTATION DETAILS AND MEASUREMENT RESULTS

The proposed supply voltage regulation and measurement techniques were implemented in a test-chip (Figure 5), fabricated in a 0.13µm, 1.2V CMOS process and packaged in a 108-pin PGA package. The test chip consists of unregulated and regulated test-cases, implemented for an iso-area and iso-pad comparison. The unregulated test-case used 3 V_{DD}, 3 V_{SS} pads and 670pF of C_P, while the regulated test-case had 1 V_{DDH}, 2 V_{DD}, 3 V_{SS} pads, 356pF of C'_P and 165pF of C_A. The total white space available for decaps in the regulated test-case was reduced to account for the area overhead of undershoot/overshoot detectors and the sampling clock (ϕ_1-ϕ_6) generator. A configurable load-current generator (10mA-120mA),

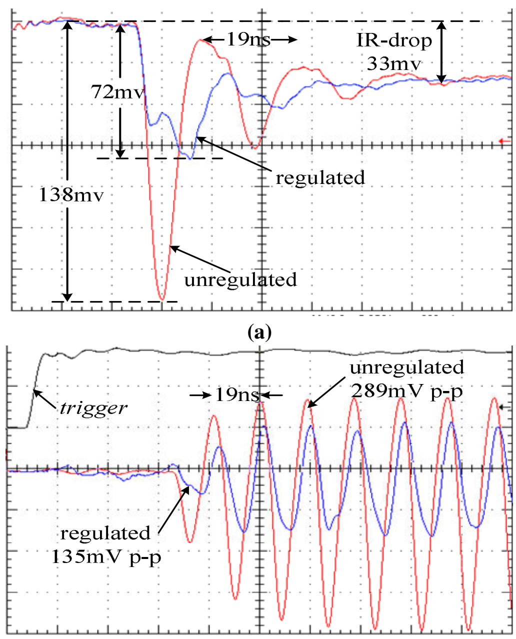
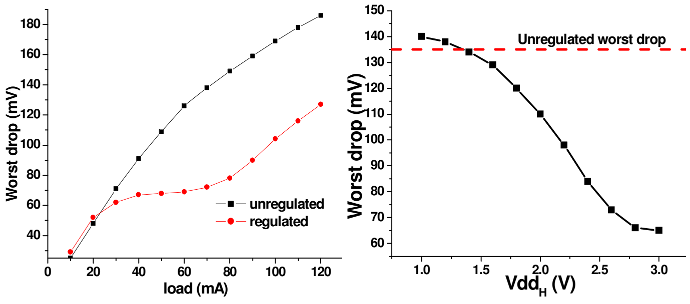


Figure 5. Measured unregulated and regulated supply noise waveforms for step load (a) and during resonance (b).



(a) (b)

Figure 6. Measured worst drop as a function of load (a) and as a function of V_{DDH} (b).

with variable duty cycle and period (0.5ns-2µs) was implemented using an array of transistors connected between V_{DD} and V_{SS}. The proposed on-chip oscilloscope was used for the measurement of supply noise. An analog V-I converter based supply drop monitor [10] was implemented to validate the supply noise measurements. The measurements were also verified by direct on-chip probing of supply voltage at the top-level metal layers using probe pads.

Figure 6 shows a comparison of the measured on-die supply noise with and without supply regulation for a typical die. In Figure 6(a), the excitation load-current ramps up from 0 to 70mA, representative of the wake-up of a power/clock-gated module. Active regulation reduces the overall supply drop by 48% from 138mV to 72mV, and Ldi/dt drop by 63% from 105mV to 39mV, which represents a decap amplification factor of 9.9X. During resonance (Figure 6(b)), the peak-to-peak supply drop reduces from 289mV to 135mV, an improvement of 53%. The resonance frequency of the first droop was measured to be 52.7MHz. Figure 7(a) shows the measured worst supply drop as a function of peak load-current for one die. Figure 7(b) shows the measured regulated worst supply drop as a function of V_{DDH}. Figure 8 shows the measured supply noise waveforms for the ramp load with 70mA peak current demonstrating the reduction in worst supply drop with increasing V_{DDH}.

Figures 9(a) shows V_{DD}-V_{SS} waveforms measured using the V-I monitor and the on-chip oscilloscope, respectively, for ramp loads and during resonance. Both IR and Ldi/dt drops show good correspondence. A comparison with probe pads for resonance is shown in Figure 9(b). The difference in the amplitude of supply noise observed by the measurement circuits and the on-chip probes can be attributed to the probing of the top-layer grid by the probe pads which does not account for full IR drop in the power grid. The power consumption of the on-chip oscilloscope and the V-I monitor were measured to be 1mW and 29mW, respectively, showing that the on chip scope is significantly more power efficient.

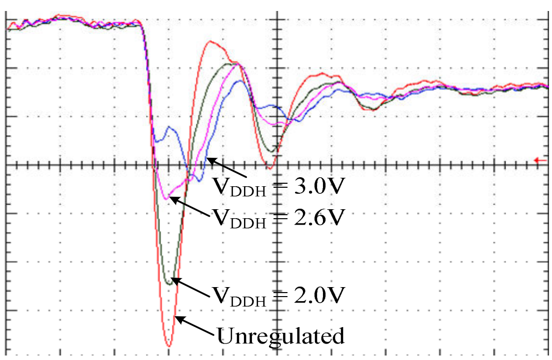
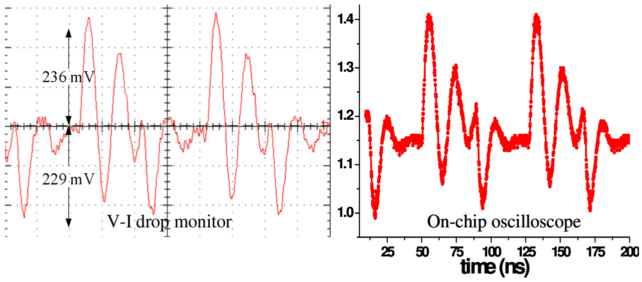
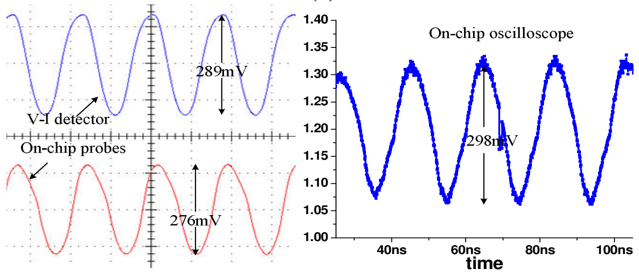


Figure 7. Measured supply noise as a function of V_{DDH}.



(a)



(b)

Figure 8. Measured supply noise waveforms using the V-I converter-based circuit and using the proposed on-chip oscilloscope, for ramp load (a) and during resonance (b).

5. CONCLUSIONS

In this paper, a high-voltage supply based supply noise suppression technique and a digital, subsampling based supply noise measurement technique were presented. Measurements on a 0.13m CMOS prototype demonstrate noise reduction by 48% and 53% for ramp loads and during resonance, respectively. Supply noise measurements from the proposed measurement circuit were validated against a traditional analog supply drop monitor and direct on-die probing and show good correlation.

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