An Ultra Low Power 1V, 220nW Temperature Sensor for Passive Wireless Applications

Yu-Shiang Lin, Dennis Sylvester and David Blaauw
Dept of EECS, University of Michigan
1301 Beal Ave, Ann Arbor, MI 48109-2122
{yushiang,dennis,blaauw}@eecs.umich.edu

Abstract- This work presents a low power temperature sensor that is suitable for passive wireless systems. The test chip is fabricated with a 0.18μm CMOS technology and the total area is 0.05mm^2. With temperature inaccuracy of -1.6°C/+3°C from 0°C to 100°C , the temperature sensor consumes only 220nW at 1V under room temperature. The data conversion rate is 100 sample/s with an output resolution of 0.3°C, which is sufficient for most sensor applications.

I. Introduction

Since the last decade, smart temperature sensors have growing demands on VLSI, automotive, and wireless sensing applications due to their low cost. Monitoring VLSI chip temperature plays a key role on long-term system level reliability and performance. Rapidly increasing transistor numbers require embedded sensors with small area and low power that can be spread over the chip for temperature management [1]. Sensors that produce low power consumption not only helps with power grid integrity but also alleviates self-heating issues. Recently, growing interests in building monitoring systems with wireless telemetry or RFID cards demand even more stringent power consumption [2, 3]. The energy range which is defined as the distance from the transponder and reader that is just enough to operate the transponder can be extended by cutting down the power dissipation [4]. In the work reported in [5], the temperature sensor consumes 10μW compared to 2μW by the reader for their passive RFID transponder. This means that the power consumption of the temperature sensor is highly related to the working distance of such wireless systems.

Smart temperature sensor ICs were first developed using bandgap reference and analog-to-digital converters (ADCs) [6, 7]. Such sensors typically are able to achieve better than $\pm 1°C$ accuracy with calibration. Combining with offset cancellation, dynamic element matching and room-temperature calibration, accuracy of $\pm 0.1°C$ with 247.5μW power consumption was reported [8]. Time-to-digital converter (TDC) was also proposed to measure the temperature by tracking a pulsed signal along a delay line [9]. In this work, our goal is to implement a temperature sensor with sub-μW power dissipation with acceptable accuracy for ultra low power passive wireless sensor applications. In the section II, the architecture of our proposed circuits will be discussed and the power consumption will be analyzed. Measurement results will be shown in section III and is followed by the conclusion in section IV.

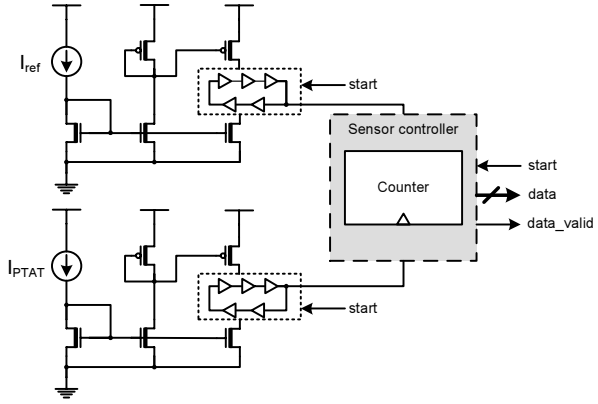

Figure 1: Temperature sensor block diagram.

II. Low power temperature sensor design

Fig. 1 shows the block diagram of the temperature sensor. Temperature insensitive current source I_{ref} and proportional to absolute temperature (PTAT) current source I_{PTAT} are generated seperately. Each current source is mirrored and fed into the current-starved ring oscillator to translate the temperature information into frequency. Afterwards, the clock signals are fed into an UP-counter that is triggered by a *start* signal in order to produce a digitized output. The sensor controller decides when the conversion should start and responds by a *data_valid* signal when the data is available. The key blocks of this work is to generate current sources I_{ref} and I_{PTAT} with low power dissipation and is still able to maintain reasonable temperature characteristics.

Generating I_{PTAT} is a commonly used technique in bandgap reference design for compensating the complementary to absolute temperature (CTAT) current sources. Fig. 2 shows the schematic for such purpose that was originally implemented with bipolar circuits

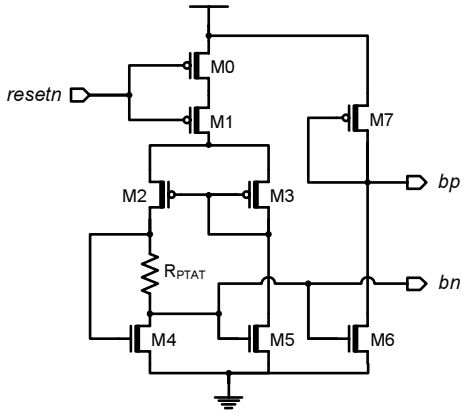

Figure 2: Schematic for I_{PTAT} generation.

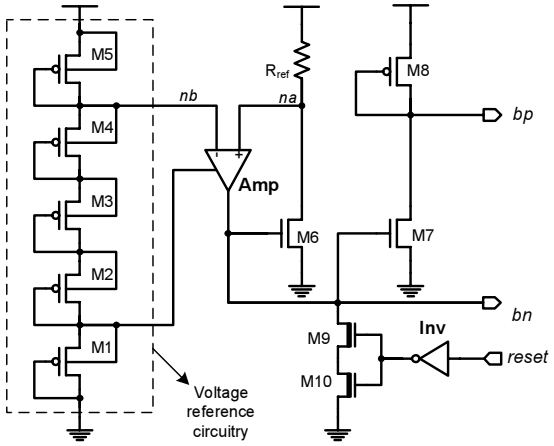

Figure 3: Schematic for I_{ref} generation.

[10]. CMOS transistors can be used in place of bipolar transistors when operating in the subthreshold region. In this way, we can reduce the power consumption of this block significantly, which accounts for roughly 30% of the total power dissipation. When V_{gs} is less than V_{th} and V_{ds} is larger than three V_T, the drain current of transistor M4 and M5 can be approximately written by:

$$I_{sub} = \mu C_{OX} \cdot \frac{W}{L} \cdot {V_T}^2 \cdot \exp\left[\frac{V_{gs} - V_{th}}{nV_T}\right] \tag{1}$$

where V_T and V_{th} are the thermal voltage represented by kT/q and V_{th} is the threshold voltage of the transistor, respectively. Through current mirror transistors M2 and M3, the current through resistor R_{PTAT} can be expressed as

$$I_{R_{PTAT}} = \frac{nV_T}{R_{PTAT}} \ln\left[\frac{W_5 W_3 L_4 L_2}{W_4 W_2 L_5 L_3}\right] \tag{2}$$

Assuming that V_{th} mismatch is ignored. By properly biasing the circuit, the output current is proportional to V_T. The sensitivity to the geometric variations can be minimized by designing a large value in the log function. Large transistor sizes also help to reduce the impact on threshold voltage due to random doping fluctuations.

The temperature insensitive current source is generated by a self-biasing technique. The circuit diagram is shown in Fig. 3. M1 through M5 are diode-connected transistors used to provide bias voltages that are proportional to the supply voltage. The voltage of *nb* is replicated to node *na* through negative feedback loop consisting of transistor M6, resistor R1 and the amplifier. Therefore, the drain current of M6 can be defined by $(V_{dd} - V_{na} - V_{os})/R_{ref}$, where V_{os} is the input offset voltage of the amplifier. The fractional temperature coefficient (TC_F) of I_{d6} is

$$TC_F(I_{d6}) = \frac{1}{I_{d6}} \cdot \frac{dI_{d6}}{dT} \tag{3}$$

$$= \frac{1}{V_{dd} - V_{na} - V_{os}} \cdot \left(\frac{dV_{na}}{dT} - \frac{1}{R_{ref}} \cdot \frac{dR_{ref}}{dT}\right) \tag{4}$$

To reduce the non-ideal temperature effect on the sensor we do the following: 1) the resistor is chosen so that the second-order temperature coefficient (TC2) is minimized; and 2) transistors M1-M5 should be identically sized to eliminate the first term of Eq. 4.

It is noted that in this work, the voltage reference circuitry in Fig. 3 was implemented as a voltage divider. Thus, I_{ref} is inversely proportional to the supply voltages and lead to changing output value with power supply noises. To fix this issue in the future, the voltage reference should be re-designed to have constant output regardless of the supply voltage.

Both I_{ref} and I_{PTAT} blocks generate analog voltages *bn* and *bp* to provide the starving voltage for the ring oscillator. Temperature information in I_{ref} and I_{PTAT} are translated into frequency for the signals *clk_i* and *clk_l*. In Fig. 4, the sensor controller is shown as well as the timing diagram. *clk_i* and *clk_l* are used to clock the q-counter and the d-counter, respectively. When *start* is 0, both counter outputs are cleared. Triggered by input signal *start*, the controller asserts output *data_valid* after the q-counter gets overflowed 2^{10} cycles later. *data_valid* immediately stops both counters from changing their content until *start* goes to 0 again to reset the states. The temperature sensor including the I_{ref} and I_{PTAT} blocks are implemented so that they can be deactivated during sleep state by asserting *reset* signal. When high conversion rate in not required, the

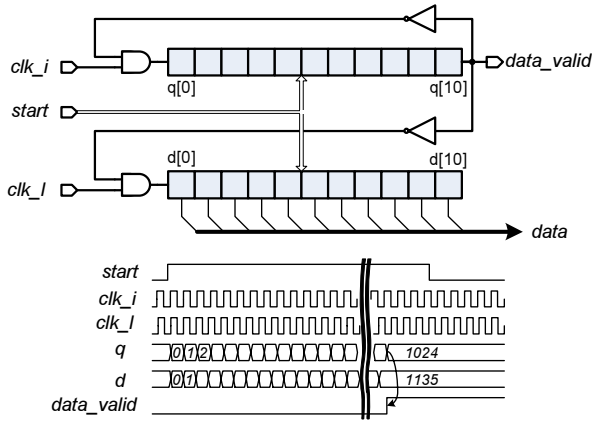

Figure 4: Block diagram and timing diagram of the sensor controller.

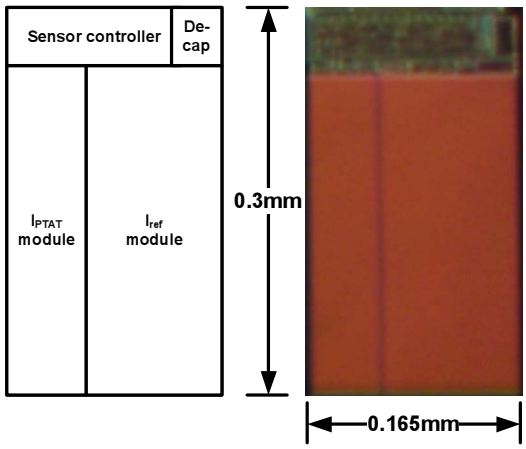

Figure 5: Die photo of the temperature sensor.

temperature sensor can be periodically deactivated to save power.

The total power of our proposed temperature sensor can be written as follow:

$$P_{tot} = V_{dd} \cdot [(n+1)I_{PTAT} + (m+1)I_{ref}] + P_{ctrl} \quad (5)$$

where n, m are the multiplication constants of current mirrors. P_{ctrl} is the power consumption of the sensor controller. For simplification, static power consumption is neglected in this first order analysis. Therefore, P_{ctrl} can be expressed as $\alpha C_c V_{dd}^2 f_{clk}$ given the total capacitance C_c, effective activity factor α and clock frequency f_{clk}. Considering f_{clk} as a function of I_{ref}, I_{PTAT} and V_{dd}, Eq. 5 can be re-written as

$$P_{tot} = k1 \cdot \frac{V_{dd}}{R_{PTAT}} \cdot V_T + k2 \cdot \frac{V_{dd}^2}{R_{ref}} \quad (6)$$

where k1 and k2 are geometry and process related constants. It is shown that 1) the power consumption of the sensor is a linear function of temperature; and 2) power consumption can be proportionally reduced by using large resistors. The size of resistors are determined by the target current consumption of 200nA and by matching I_{ref} and I_{PTAT} at room temperature. In this work, 6.2MΩ and 3.2MΩ P+ poly resistors are chosen for R_{ref} and R_{PTAT}, respectively.

III. Measurement Results

The chip was implemented in a 0.18μm 1P6M digital CMOS process. The total area of the temperature sensor module is 0.05mm^2. The die photo is shown in Fig. 5. In this test chip, 85% of the area is dominated by the resistor for biasing the current sources.

The measurement is setup inside a TestEquity environment chamber TE-105A. The power consumption is measured by a Keithley electrometer 6517A and the results are shown in Fig. 6. The supply voltage is set to 1V while the nominal supply voltage for this technology is 1.8V. The power consumption increases from 200nW to 310nW from 0°C to 100°C, which matches the expected trend from Eq. 6. The slope at higher temperature is larger mainly because leakage components become non-negligible in this region. It is noted that there is a trade-off between power consumption and area. While most area are dominated by the resistors, reducing the resistance by half also reduce total area by 43%. In the same time, the conversion rate is also doubled because of the boost in ring oscillator's starving current. In this test chip, *clk_i* is running at 100kHz for an equivalent of 100 samples/s. This is sufficiently fast for most applications, and in fact we can lower the conversion rate to lower the reading noise as will be shown in Fig. 8.

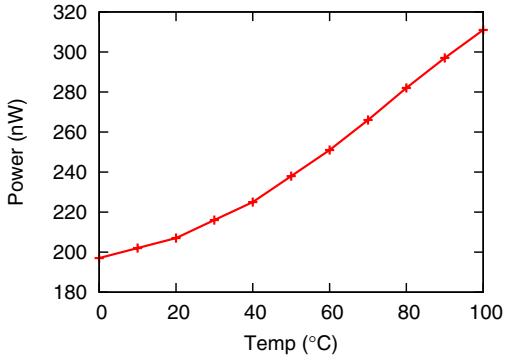

Figure 6: Power consumption of the temperature sensor.

The temperature inaccuracy of 5 test samples after two-point calibration are shown in Fig. 7. The temperature error is ranging from -1.6°C to +3°C over the

Table 1: Comparison of temperature sensors.

Sensor	Inaccuracy ($^\circ C$)	Power Consumption	Technology	Area (mm^2)	Temperature range ($^\circ C$)	Conversion rate (samples/s)
[6]	± 1	$7\mu W$	$2\mu m$	1.5	-40∼120	50
[7]	± 1	1mW	$0.6\mu m$	3.32	-55∼125	40k
[8]	± 0.1	$247.5\mu W$	$0.7\mu m$	4.5	-55∼125	1∼10
[9]	-0.7/+0.9	$10\mu W$	$0.35\mu m$	0.175	0∼100	10k
[5]	-1.8/+2.2	$10\mu W$	N/A	N/A	0∼100	∼2
[3]	± 1	$0.9\mu W$	$0.18\mu m$	0.2	27∼47	N/A
This work	-1.6/+3	$0.2\sim0.31\mu W$	$0.18\mu m$	0.05	0∼100	100

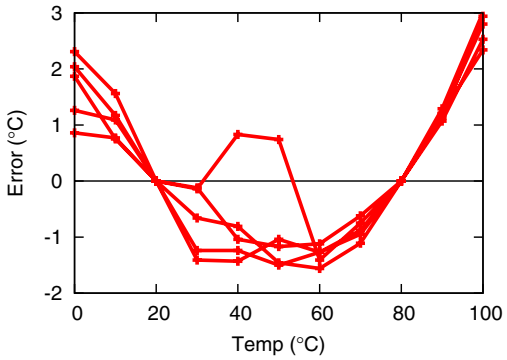

Figure 7: Temperature inaccuracy of the temperature sensor with two-point calibration at 20°C and 80°C.

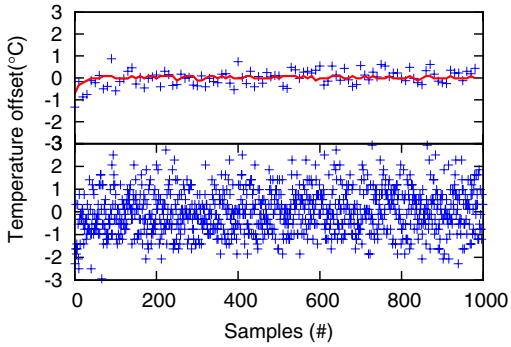

Figure 8: Temperature inaccuracy over samples (top: 10 samples/s; bottom: 100 samples/s; solid line: actual temperature).

sweeping range from 0°C to 100°C. With 11 bits output from the sensor controller, the temperature resolution is 0.3°C.

Table 1 lists the previous works on smart temperature sensors and compares the key circuits parameters to this work. It can be seen that our proposed temperature sensor adopts an approach that is favorable for low power operation at the expense in terms of temperature inaccuracy. The total area of our test chip is comparable or even smaller than other works after considering the translation of different technologies.

Fig. 8 shows the long term characteristics of the sensor by setting up the chip in the temperature chamber (top: 10 samples/s; bottom: 100 samples/s). After taking 1000 samples successively, the 3σ inaccuracy value over the samples is 2.5°C. By lowering the conversion rate to 10 samples/s, the 3σ inaccuracy is reduced to 0.28°C by averaging the samples. The actual temperature is also shown in solid line in Fig. 8.

IV. Conclusion

In this work, we implemented an ultra low power temperature sensor for passive wireless applications. At room temperature, it consumes merely 220nW while continuously running. By utilizing a temperature independent current source I_{ref} and PTAT current source I_{PTAT}, the temperature information can be synthesized and translated into digital output in a conversion rate of 100 samples/s. Measured data shows that the temperature inaccuracy of the temperature sensor is -1.6°C/+3°C from 0°C to 100°C.

References

[1] D. Duarte et al. Temperature sensor design in a high volume manufacturing 65nm cmos digital process. *CICC*, pages 221–224, Sept 2007.

[2] F. Kocer and M. Flynn. An RF-powered, wireless CMOS temperature sensor. *IEEE Sensors Journal*, 6(3):557, 2006.

[3] Zhou S. and Wu N. A novel ultra low power temperature sensor for UHF RFID tag chip. *ASSCC*, pages 464–467, Nov 2007.

[4] K. Finkenzeller. *RFID handbook*. John Wiley & Sons, 2003.

[5] K. Opasjumruskit et al. Self-powered wireless temperature sensors exploit rfid technology. *Pervasive Computing, IEEE*, 5(1):54–61, Jan.-March 2006.

[6] A. Bakker and J. Huijsing. Micropower CMOS temperature sensor with digital output. *JSSC*, 31(7):933–937, July 1996.

[7] M. Tuthill. A switched-current, switched-capacitor temperature sensor in 0.6-μm CMOS. *JSSC*, pages 1117–1122, 1998.

[8] M. Pertijs, K. Makinwa, and J. Huijsing. A CMOS smart temperature sensor with a 3σ inaccuracy of ± 0.1°C from -55°C to 125°C. *JSSC*, 40(12):2805–2815, Dec. 2005.

[9] P. Chen et al. A time-to-digital-converter-based CMOS smart temperature sensor. *JSSC*, 40(8):1642, 2005.

[10] K. Kimura. Low voltage techniques for bias circuits. *IEEE Tran. on Circuits and Systems*, 44(5):459, May 1997.