

A 0.5V Sub-Microwatt CMOS Image Sensor with Pulse-Width Modulation Read-Out

Scott Hanson, ZhiYoong Foo, David Blaauw, Dennis Sylvester

University of Michigan, Ann Arbor

hansons@umich.edu

Telephone: (734)615-8930, Fax: (734)763-9324

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Abstract

Energy minimization is a critical goal in size-constrained wireless sensors. Sensing elements are traditionally power hungry and require special attention in low energy systems. In this work, we study ultra-low power image sensors. In particular, we explore the use of aggressive voltage scaling in CMOS image sensors for applications ranging from retinal prostheses to battlefield monitoring and surveillance. We begin with a discussion of the challenges faced by a traditional 3T active pixel sensor as the supply voltage scales to 0.5V and below. We then discuss an image sensor with pulse-width modulation read-out that is optimized for 0.5V operation. A 0.13 μm test-chip with a 128x128 pixel array is shown to be functional with V_{dd} as low as 0.45V with energy consumption of 140nJ/frame at $V_{dd}=0.5\text{V}$ (8.5 frames per second) and power consumption of only 700nW at $V_{dd}=0.5\text{V}$ (0.5 frames per second). A focus is also placed on quantifying the noise implications of low voltage operation on the test-chip, which has a measured signal-to-noise ratio of 23.4dB in saturation at $V_{dd}=0.5\text{V}$.

Keywords: image sensor, low power, low voltage

I. Introduction

Rapid advances in circuit, sensor, power source and packaging technologies have led to the development of cubic centimeter wireless sensors [1] and will soon make cubic millimeter wireless sensors a reality. Due to the size constraints on power sources in such wireless sensing systems, energy minimization is one of the primary challenges. Energy-efficient circuit techniques like supply voltage (V_{dd}) scaling and power gating have helped to address this challenge for digital circuits, but the energy overhead of sensing remains a challenge. In this work, we focus on energy minimization in CMOS image sensors which have applications ranging from retinal prostheses [2] to battlefield monitoring and surveillance [3].

Operating circuits at reduced V_{dd} can deliver substantial energy reduction for digital circuits and has been investigated extensively in recent work [4][5]. However, voltage scaling has been limited in analog circuits, where small voltage headroom and transistor mismatch reduce the signal-to-noise ratio (SNR). Since CMOS image sensors are composed primarily of analog circuits, V_{dd} is typically set substantially above 1V. Recent work has demonstrated CMOS image sensor operation at 1.35V [15] and 1.2V [16], and we continue that trend with a look at the implications of aggressive voltage scaling to 0.5V and below.

We first investigate the challenges created by voltage scaling in a conventional three transistor active pixel sensor (APS) structure. We find that a reduction in signal range and an increase in noise lead to degradation of the signal to noise ratio (SNR) at low voltage. This degradation to SNR must be addressed to achieve the full energy benefit of low voltage operation.

Multiple techniques can be used to recover lost SNR; we describe one solution that uses a pulse-width modulation (PWM) structure to reduce noise. Unlike conventional CMOS image sensors, which use an in-pixel source follower to drive the photodiode voltage onto the bitline, the image sensor proposed in this work uses an in-pixel comparator to do analog-to-digital conversion within the pixel. The in-pixel comparator creates a pulse with width that is linearly related to the photodiode voltage. We describe the implementation of a 128x128 pixel PWM image sensor test-chip with a pixel structure optimized for low voltage operation [6]. Test-chip measurements show that the image sensor functions with V_{dd} as low as 0.45V. At $V_{dd}=0.5V$ the image sensor consumes 140nJ/frame at 8.5fps and draws only 700nW at 0.5fps, both lower than

any previously reported image sensor. As we discuss later in this work, the reduced power consumption observed at low voltage comes at the cost of increased noise. Despite efforts to reduce noise through the use of the PWM structure, process variations inevitably introduce large current variations as voltage reduces, leading to spatial noise and a measured SNR of 23.4dB at 0.5V.

We begin in Section II with a discussion of the implications of voltage scaling in conventional CMOS image sensors. We show that reduced voltage swing, increased sensitivity to process variations, and a reduced on-current to off-current ratio lead to a reduced SNR at low voltage. We continue our exploration of low voltage image sensing in Section III by considering an implementation of a low voltage image sensor with PWM read-out. We discuss test-chip measurements in Section IV and finally present conclusions in Section V.

II. Voltage Scaling Challenges for CMOS Image Sensors

Aggressive supply voltage (V_{dd}) scaling has the potential to deliver dramatic energy reductions to CMOS image sensor arrays, though low voltage operation is fraught with difficulties for both digital and analog circuits. As V_{dd} is reduced from typical values (e.g., 1.2V in a 0.13 μm technology) toward the device threshold voltage, the current drawn by transistors changes from drift-based strong-inversion current to diffusion-based weak-inversion current. Though the minimum V_{dd} has often been limited to the sum of the NFET and PFET threshold voltages ($V_{th,n}+V_{th,p}$) for digital circuits and a much larger value for analog circuits, most digital and simple analog circuits continue to function correctly into the subthreshold regime ($V_{dd}<V_{th,n}$ or $V_{dd}<V_{th,p}$). Inverters have been shown to maintain functionality with V_{dd} as low as 65mV [1], and full microprocessors have been proven functional with V_{dd} below 200mV [7][8][9]. Recent efforts have also demonstrated correct operation of multiple analog building blocks near 0.5V [10].

Though CMOS image sensors contain both analog and digital circuits, analog circuits are typically more sensitive to voltage scaling and are the focus of this section. We look, in particular, at the challenges posed by the conversion of an analog pixel voltage into a digital light intensity. For the sake of generality, we focus on the typical 3T active pixel sensor (APS) with an analog-to-digital converter (ADC) shared at the column level (Figure 1). The model of Figure 1 includes a single pixel with a source follower (the pull-up device M1, an access

transistor M2, and a current source M3 shared by the column). It additionally includes N unaccessed pixels, which are modeled as leaking access transistors. Voltage scaling creates three key challenges for this structure: reduced voltage swing, increased sensitivity to process variations, and a dramatic reduction in the on-current to off-current ratio (I_{on}/I_{off}) of a typical device. We consider each of these challenges in turn using simulations of a $0.13\mu\text{m}$ technology with $V_{th,lin}\sim 400\text{mV}$ and $V_{th,sat}\sim 350\text{mV}$. We show that each challenge reduces signal levels or increases noise, effectively reducing SNR.

A. Reduced Voltage Swing

The most obvious consequence of low voltage operation is a reduced voltage swing at the input and output of the source follower, which has the effect of reducing signal levels (thus decreasing SNR). We illustrate this voltage swing reduction using the bitline model of Figure 1 with only a single pixel on the bitline (i.e., $N=0$), and assume that the ADC tied to the bitline is capable of correctly resolving 1mV changes on the input. The source follower current source (M3) is biased such that M1 is saturated at $V_{dd}=1.2\text{V}$ and remains unchanged as V_{dd} is reduced. As shown in Figure 2, the output range of the converter composed of the source follower (M1, M2, M3) and the ADC reduces approximately linearly with V_{dd} as a result of reduced voltage swing at the input and output of the source follower. The output range values in Figure 2 are normalized to the minimum resolvable signal of 1mV.

The data in Figure 2 show a prohibitively small output range below $V_{dd}=1\text{V}$ and that the output range approaches zero at $V_{dd}=0.4\text{V}$. However, the current source (M3) is biased to ensure saturation in M1 at $V_{dd}=1.2$. This biasing is unattractive at low voltage since M1 cannot reach strong inversion. If M3 is alternatively biased to ensure that M1 remains in the subthreshold region, the output range at $V_{dd}=0.4\text{V}$ can be increased by a factor of 6 as shown in Figure 2. Note that, even with the subthreshold bias point, the output range degrades by a factor of 5.8 when moving from $V_{dd}=1.2\text{V}$ to $V_{dd}=0.4\text{V}$.

B. Increased Sensitivity to Process Variations

While the use of subthreshold-biased devices is critical to increasing the output range, subthreshold current is exponentially-dependent on V_{th} . Small fluctuations in V_{th} lead to large current variations, effectively shifting the transfer characteristic of the in-pixel source follower.

Small vertical offsets in the transfer characteristic can be corrected using correlated double sampling, particularly at high voltage. However, large vertical offsets and horizontal offsets present great challenges, particularly with the small headroom available at low voltage. This variability in the transfer characteristic introduces noise into the image in the form of fixed pattern noise (FPN) and photo-response non-uniformity (PRNU), effectively reducing SNR.

To explore this problem quantitatively, again consider the bitline model from Section IIA with $N=0$ and device M3 biased such that device M1 is in the subthreshold region. Monte Carlo simulations (1000 iterations) are run with models for both global correlated process variations and local uncorrelated (i.e., random) process variations. Vertical offset is corrected for the transfer curve at each iteration (i.e., correlated double sampling is performed), and noise is estimated as the standard deviation of the signal value at the maximum input level. Figure 3 shows the calculated SNR as a function of V_{dd} . At $V_{dd}=1.2\text{V}$, the SNR is 51dB or approximately 370:1. Note that this ratio is significantly less than the output range of 570 predicted in Figure 2 due to process variation-induced noise. Additionally, the SNR reduces by 22.6dB for a 13.7X output range reduction when V_{dd} is reduced from 1.2V to 0.4V. This is greater than the 5.8X range reduction observed in Figure 2, which suggests that the effects of voltage scaling are magnified by process variability. Test-chip measurements presented in Section IV confirm that increased noise due to process variations is a significant problem at low voltage that must be addressed.

C. Reduced I_{on}/I_{off}

To this point, we have considered only the noise produced by a single in-pixel source follower in isolation. In a real system, many pixels share the same bitline, and un-accessed pixels introduce noise in the accessed pixel. This issue is relatively unimportant at high voltages, since the saturation current of a single device is greater than the leakage current of that device by a factor of 50,000 or more. However, this presents a great challenge when subthreshold bias currents are used at low voltages since subthreshold currents may only be greater than leakage currents by a factor of 100 (and the margin can be even smaller for different bias points). Consequently, the cumulative leakage from the un-accessed pixels becomes comparable to the read current, and significant noise is injected through the shared bitline. This problem is further

exacerbated by variations, particularly random variations that introduce mismatch within a bitline.

To quantify this problem, once more consider the model from Section IIA with device M3 biased such that M1 is in the subthreshold region. In addition to the case with $N=0$, we also consider $N=127$ and $N=1023$ (i.e., bitline sizes of 128 and 1024). Monte Carlo simulations presented in Figure 3 reveal that SNR reduces by 4.5dB for a 40% range reduction when the bitline size is increased from 1 to 128. An additional 50% range reduction occurs when the bitline size is increased from 128 to 1024.

The three challenges presented in this section point to reduced signal range and increased noise at low voltage, resulting in a dramatic drop in SNR. Previously proposed techniques such as the use of multiple integration periods [14] can be used to recover some of the lost SNR, but specific attention to low voltage device characteristics will be necessary to fully enjoy the energy benefits of low voltage operation. In the next section, we introduce a CMOS image sensor optimized specifically for low voltage operation. Furthermore, the proposed image sensor addresses the bitline noise problem described in this section.

III. A Low Voltage Image Sensor Implementation

The energy benefits of low voltage operation are potentially immense, but this energy benefit comes at the cost of reduced SNR, as demonstrated in the previous section. In this section, we continue to explore the energy-noise trade-off of low voltage operation within the context of a low voltage image sensor test-chip. The image sensor is optimized for low voltage operation and uses a PWM read-out to address bitline noise problems. Details of the PWM concept, the test-chip and pixel architectures, and physical implementation follow.

A. PWM Concept

Bitline noise was identified as a significant problem for low voltage image sensors in Section II. We use a structure that eliminates bitline noise by driving the bitline with a digital signal rather than an analog signal. Instead of buffering the integrated photodiode voltage onto the bitline using a source follower as in the 3T APS pixel, the pixel converts the integrated photodiode voltage into a pulse with a width linearly related to the voltage level. By using this PWM read-out, the bitline may be driven by a digital buffer with drive current that far exceeds

that of a source follower. Unlike the 3T APS pixel, this large drive current can be easily distinguished from the cumulative leakage current of un-accessed devices. Similar approaches have been proposed previously [13][14][15], with [15] demonstrating robust operation down to $V_{dd}=1.35V$.

Figure 4a shows the column architecture for an image sensor with PWM read-out, and Figure 4b shows timing waveforms for a typical read operation. Like the 3T APS structure, the PWM pixel contains a reset transistor with a photodiode. In place of the source follower found in the 3T APS structure, the PWM pixel contains a comparator and a tri-state buffer (which can be a simple pass transistor or a full buffer). In typical operation, the voltage on the photodiode node $pd[0]$ is first pulled up by the reset transistor (Step 1). The reset signal is then released and photocurrent is integrated at $pd[0]$ (Step 2). After integration, a pulse-width counter shared at the bitline-level begins incrementing to measure time, and the photodiode voltage is compared with the signal $ramp[0]$ using the in-pixel comparator. Though a transfer gate is not used to isolate the photodiode from the comparator input, the comparison phase is fast, and the voltage at $pd[0]$ changes negligibly during comparison to $ramp[0]$. When the ramp voltage equals the photodiode voltage, the output of the comparator flips (Step 3), and the tri-state buffer discharges the bitline, freezing the pulse-width counter at a value linearly related to the incident light intensity (Step 4).

B. Test-Chip Architecture

A CMOS image sensor with PWM read-out has been implemented in a 128x128 pixel array. The top-level architecture is shown in Figure 5. Shift registers in the row driver sequentially select rows in the 128x128 pixel array to perform integration and read operations. During read operations, bitlines for each of the 128 columns are fed to a bank of 10-bit counters, which are used for pulse-width-to-digital conversion. Counter outputs (i.e., the digital pixel values) are stored in a 1280-bit buffer that may be scanned out at high speed during test. Integration and read operations are controlled by a small finite state machine (FSM), ramp generator, and clock generator. Multiplexors enable the selection of off-chip FSM, ramp, and clock signals to permit maximum flexibility.

C. Pixel Architecture

The pixel structure used in this work is shown in Figure 6. Like the general pixel described in Figure 4, the proposed pixel contains three components: a reset block, a comparator, and a read buffer. The reset block pulls up the voltage on the photodiode node pd during reset. Device M1 sets the voltage at pd below V_{dd} to ensure a linear response from the comparator block. The comparator is implemented as a two-transistor structure which will be described in the next section. The read buffer (devices M5 and M6) is implemented as a two transistor structure identical to the read buffer used in the 8 transistor SRAM cell used for robust low voltage operation [11]. Though the read buffer could be implemented as a single pass transistor (as in the 3T APS structure), the output current from the comparator can be very small when the voltage at pd is small. It was shown in Section IIC that small read current can be easily overwhelmed by bitline noise. The read buffer amplifies the read current, driving the bitline strongly and overriding bitline noise.

D. Two Transistor Comparator

To save pixel area and improve fill-factor, we use the two transistor (2T) comparator structure composed of devices M3 and M4 in Figure 6. Assuming that devices M3 and M4 are biased in the subthreshold region, the currents I_{M3} and I_{M4} are given by Equations 1 and 2, where m is the subthreshold slope factor, V_{th} is the threshold voltage, and v_T is the thermal voltage. Subthreshold transistors act as excellent current sources due to the minimal dependence of current on drain-source voltage for drain source voltages greater than $3 \cdot v_T$. Consequently, I_{M3} and I_{M4} are exponential functions of $(V_{dd} - V_{ramp})$ and V_{pd} , respectively. By stacking devices M3 and M4, the values of I_{M3} and I_{M4} may be compared directly. When $(V_{dd} - V_{ramp})$ is less than V_{pd} , the value of I_{M4} is greater than the value of I_{M3} , and the output of the comparator is pulled low. When $(V_{dd} - V_{ramp})$ is greater than V_{pd} , the value of I_{M3} is greater than the value of I_{M4} , and the output of the comparator is pulled high.

$$I_{M3} = I_{o,M3} \cdot e^{\left(\frac{V_{dd} - V_{ramp} - V_{th,M3}}{m_{M3} \cdot v_T}\right)} \cdot \left(1 - e^{-\frac{V_{dd} - V_{cmp}}{v_T}}\right) \approx I_{o,M3} \cdot e^{\left(\frac{V_{dd} - V_{ramp} - V_{th,M3}}{m_{M3} \cdot v_T}\right)} \propto e^{\frac{-V_{ramp}}{m_{M3} \cdot v_T}} \quad \text{Equation 1}$$

$$I_{M4} = I_{o,M4} \cdot e^{\left(\frac{V_{pd} - V_{th,M4}}{m_{M4} \cdot v_T}\right)} \cdot \left(1 - e^{-\frac{V_{cmp}}{v_T}}\right) \approx I_{o,M4} \cdot e^{\left(\frac{V_{pd} - V_{th,M4}}{m_{M4} \cdot v_T}\right)} \propto e^{\frac{V_{pd}}{m_{M4} \cdot v_T}} \quad \text{Equation 2}$$

The voltage transfer characteristic of the 2T comparator is plotted in Figure 7 at $V_{dd}=0.5V$ and is compared to that of a conventional five transistor (5T) comparator based on a differential-

pair structure. The 2T structure shows excellent gain relative to the 5T comparator due to the exponential dependence of currents I_{M3} and I_{M4} on $(V_{dd}-V_{ramp})$ and V_{pd} . Though the reduced area of the 2T structure is attractive, it has two clear drawbacks as compared to the 5T structure: increased variability and increased short-circuit currents.

Since the 2T structure compares the current through an NFET device to that of a PFET device, it is vulnerable to global mismatch between PFET and NFET devices (e.g., V_{th} variations induced by global doping shifts) as well as random mismatch (e.g., V_{th} variations induced by random dopant fluctuations). In contrast, the conventional 5T structure compares the current through two NFET devices and is vulnerable only to random variations. To quantify this observation, we run Monte Carlo simulations accounting for both global (correlated) and local (random) mismatch at $V_{dd}=0.5V$ with the comparator input voltage (i.e., the photodiode voltage, V_{pd}) held at 0.25V. All comparator devices are sized with $W=0.3\mu m$ and $L=0.3\mu m$ to capture the effects of random dopant fluctuations in an area-constrained system. The simulations reveal that the switching point of the 2T comparator has a standard deviation of 37 mV which is 24% larger than the variation observed on the 5T comparator. This variation, which maps to fixed-pattern noise in the image sensor, is an acceptable penalty for a 60% area reduction in the comparator.

In addition to increased variability, the 2T comparator sinks large short-circuit currents when both input voltages are near $V_{dd}/2$. This short-circuit current is minimized using the current limiters shown in Figure 6 (M7, M9), which are shared by all pixels in a column. As shown in Figure 7, the current limiters shift the comparator switching point and reduce output swing, but a high gain characteristic is maintained. The current limiters also increase switching point variation from a standard deviation of 37 mV to 43 mV. In addition to the current limiting devices, feedback from the bitline completely eliminates short-circuit current using device M8 once the bitline has switched.

E. Physical Implementation

The proposed image sensor has been fabricated in a $0.13\mu m$ bulk logic technology in an area of $1.1mm^2$ (die photo shown in Figure 8). In the target technology, $V_{th,lin}\sim 400mV$. Each $5\times 5\mu m$ pixel contains a $7.9\mu m^2$ n-diffusion/p-substrate photodiode with both polyimide and silicide layers removed.

The critical timing path that determines the frame-rate of the PWM architecture consists of the delay of the in-pixel comparator, the in-pixel read-buffer driving the bitline, and the pulse-width counter. In this work, gates along the critical delay path are sized to ensure 30 fps operation for all functional voltages. In particular, non-minimum gate lengths are used in the in-pixel comparator and in-pixel read-buffer to increase drive strength (due to reverse short channel effects [12]). The use of larger gate sizes has the added benefit of reducing V_{th} variations induced by random dopant fluctuations (which are inversely related to $\sqrt{W \cdot L}$). In applications with more stringent frame-rate requirements, gate sizing and supply voltage scaling could both be used to achieve higher frame-rates for an energy penalty.

IV. Test-Chip Measurements

In this section, we present test-chip measurements. We begin with basic image sensor characterization and then study the energy benefits of low voltage operation. Finally, we conclude with a study of noise, one of the primary consequences of low voltage operation.

A. Basic Characterization

To characterize the image sensor test-chip, collimated light from a green LED was filtered by a diffusing lens and projected onto the image sensor. During testing, on-chip control signals (including ramp and clock signals) were bypassed in favor of off-chip signals to permit fine-grained tuning, and delta-reset sampling was not performed. The image sensor was found to be functional from $V_{dd}=0.45\text{V}$ to $V_{dd}=0.7\text{V}$. Figure 9 shows that the measured response for the image sensor at $V_{dd}=0.5\text{V}$ (averaged over all pixel locations and 100 frames) is monotonic and linear. The pixel values in Figure 9 are normalized to the RMS pixel noise under dark conditions (i.e., the minimum resolvable pixel value). Basic functionality of the image sensor is further verified in the test image of U.S. currency in Figure 10. The image captured by the image sensor test-chip (Figure 10b) depicts each of the major features in the original image (Figure 10a, sampled at 128x128 resolution). Both spatial noise and temporal noise contribute to the noise evident in the test image (e.g., the erroneous white pixels in the image). Despite this noise, the image quality is sufficient for simple image processing in energy-constrained systems. The noise characteristics of the image sensor test-chip will be discussed further in Section IVC.

B. Energy Measurements

We focus in this section on the energy benefits of ultra-low voltage operation. As in the previous section, clock and ramp signals were generated off-chip to permit fine-grained tuning. However, on-chip ramp and clock generators were functional and were run in parallel to capture the power overhead of signal generation. The power overheads of clock and ramp distribution were also included in the numbers presented. Additionally, test infrastructure limitations constrain the frame-rate in subsequent measurements to a maximum of 8.5 fps.

As shown in Figure 11, the energy consumed per frame at 8.5 frames per second (fps) reduces by a factor of 180 between $V_{dd}=0.7\text{V}$ and 0.45V . This reduction is more dramatic than the quadratic trend (switching energy is proportional to V_{dd}^2) expected due to voltage scaling. Simulations indicate that the current limiters highlighted in Figure 6 become less effective at higher voltages, so much of this energy improvement is a result of reduced short-circuit current. At the minimum operating voltage of 0.45V , the energy consumption is only 6.6nJ/frame . At the target voltage of $V_{dd}=0.5\text{V}$, the energy consumption is 140nJ/frame , which is $<10\%$ of that reported in [15][16] and $<30\%$ of that reported in [17] (which does not include the power overhead of the decimation filter). A comparison to prior work is provided in Table 1.

While the energy/frame metric is important for battery-powered applications, power is often a more important metric in applications using energy scavenging. Figure 12 compares the power and energy dependence on frame rate at $V_{dd}=0.5\text{V}$. Power is minimized at low frame rates (700nW at 0.5fps), but energy is minimized at high frame rates (140nJ/frame at 8.5fps). The dependence of energy and power on frame rate is easily explained using Figure 13, which shows the contributions of leakage power and switching power to total power at different frame rates. For low frame rates, leakage power (i.e., the power consumed by leaking photodiodes) consumes more than 90% of the total power and drives up the energy/frame metric. Further improvements to power consumption at low frame rates will require a closer look at the management of photodiode leakage. For high frame rates, the photodiode leakage is amortized across multiple frames, and the switching energy becomes comparable to the leakage energy. Consequently, the energy/frame metric reduces dramatically.

C. Noise and Variability Measurements

It was shown in Section II that noise is an important concern in low voltage image sensors. Though the study of Section II was focused on the conventional 3T APS structure, much of the same intuition applies to the PWM structure proposed in this work, which uses subthreshold-biased devices. The effects of process variation are obvious in Figure 14(a), which shows FPN and PRNU as functions of V_{dd} . As expected, both FPN and PRNU increase at low voltage and climb dramatically at $V_{dd}=0.45\text{V}$. FPN can typically be reduced using correlated double sampling or delta-reset sampling. However, measurements indicate that delta-reset sampling actually increases image noise due to temporal noise during analog-to-digital conversion process. Figure 14(b) shows temporal noise (the RMS noise for each pixel averaged across all pixels) as a function of V_{dd} . Interestingly, RMS noise increases significantly above 0.7V .

In combination with FPN and PRNU (both spatial variations), temporal noise leads to increased noise. When coupled with reduced signal levels at low voltage, this increased noise leads to reduced SNR, as shown in Figure 15. Without temporal noise, the SNR reduces gradually from 0.7V and eventually drops off dramatically at 0.45V . Figure 15 also shows how noise worsens at 0.7V and above when temporal variations are included.

As discussed in Section II, the exponential dependence of current on supply voltage and threshold voltage makes low voltage image sensors susceptible to noise induced by process variations and voltage fluctuations. The results of this sub-section confirm this observation. Though this noise may be tolerable for many power-constrained designs, it can be managed using a range of techniques in designs that can tolerate area and power penalties. For example, selectively upsizing transistors in the pixel (e.g., the 2T comparator) can help to reduce local threshold voltage mismatch induced by random dopant fluctuations [18]. Though area intensive, replacement of the 2T comparator with a conventional 5T comparator could further reduce variations since the 5T comparator is less susceptible to global threshold voltage mismatch between NFET and PFET devices. Additionally, careful physical design to isolate sensitive nodes (such as the 2T comparator output) from aggressors (such as the clock signal and adjacent bitlines) can help to minimize switching noise, which has an exponential effect on current at low voltage.

V. Conclusion

In this work, we studied the use of aggressive voltage scaling in ultra-low power CMOS image sensors. We first explored the implications of ultra-low voltage operation on a conventional 3T APS structure and showed that low voltage CMOS image sensors face three important problems: reduced voltage swing, increased sensitivity to process variations, and reduced I_{on}/I_{off} . Together, these three problems result in a reduced SNR at low voltage. We used the latter portion of the paper to explore low voltage operation within the context of a 128x128 image sensor array with PWM read-out. We demonstrated the proposed array in a 0.13 μ m test-chip. Test-chip measurements showed operation as low as $V_{dd}=0.45V$, and measurements at $V_{dd}=0.5V$ showed unprecedented power consumption. We also showed that this low power operation came at the cost of increased noise. The energy advantage of low voltage image sensing is clear; future work must focus on improving noise characteristics at these low voltages.

VI. References

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Figure 1: Simulation model for a single column with 3T APS pixel structure

Figure 2: Output range for a simple bitline model at different supply voltages

Figure 3: SNR as a function of V_{dd} under process variation

Figure 4: (a) Column architecture and (b) timing waveforms for a PWM imager

Figure 5: Test-chip architecture

Figure 6: Pixel architecture

Figure 7: Static voltage transfer characteristics of 5T and 2T comparators

Figure 8: Die photo

Figure 9: Measured responsivity at $V_{dd}=0.5V$

Figure 10: (a) Original image at 128x128 resolution (b) Image captured by image sensor test chip

Figure 11: Measured energy/frame as a function of V_{dd} at 8.5 fps

Figure 12: Measured power and energy as functions of frame rate at $V_{dd}=0.5V$

Figure 13: Measured relative contributions of leakage energy and switching energy at $V_{dd}=0.5V$

Figure 14: (a) Measured FPN and PRNU as functions of V_{dd} (b) Measured temporal noise as a function of V_{dd}

Figure 15: Measured SNR as a function of V_{dd}

Table 1: Comparison with previous work

| Image Sensor | Voltage (V) | Frame Rate (fps) | Energy/Frame (nJ/frame) | Comments |
|---------------------|--------------------|-------------------------|--------------------------------|---|
| [15] | 1.35 | 9.6 | 5800 | Rescaled for 128x128 array, includes power for whole chip |
| [16] | 1.2 | 20 | 1550 | Rescaled for 128x128 array, includes power for whole chip |
| [17] | 3.3 | 30 | 480 | Does not include power of decimation filter |
| This work | 0.5 | 8.5 | 140 | Includes power for whole chip except scan buffer |