Near-Field Communication using Phase-Locking and Pulse Signaling for Millimeter-Scale Systems

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Abstract- An inductive coupling based proximity communication system is proposed for data readout of remote powered sensor systems with ultra small form factor in ~mm^3 range for implantable applications. The passive transponder is powered with a 1×1mm on-chip inductor, which also enables readout signaling using pulse signaling. The required resonance frequency for pulse signaling is obtained using a transponder PLL that locks to the incoming frequency transmitted by the reader system. Communication with a passive 1mm^2 sensor node implemented in 0.13μm technology is demonstrated.

I. INTRODUCTION AND SYSTEM OVERVIEW

Passive Radio Frequency Identification (RFID) is widely used in various areas including personal identification and public transportation. Backscattering is a commonly used method to simultaneously harvest power from the reader while transmitting data back from the transponder [1, 2]. Typically, external coils of 2-8 centimeters are used to couple magnetic waves in near field. However, for a growing number of applications, such as implantable medical devices, form factor is highly limited, requiring systems with much reduced inductor size. For example, telemetry-based prototypes for intraocular pressure (IOP) sensing specify an implant size of 3mm on the side or less [3]. Without a special fabrication process, such integrated inductors usually suffer from poor Q factors, which reduces the voltage difference seen by the reader under load modulation and hence degrades the sensitivity of the signal.

In this paper, we present an inductive coupling based proximity communication using an integrated inductor with outer dimension of 1×1mm for implantable applications with ultra-small form factors, such as IOP sensing. Recently, it has been demonstrated that a remote powering system can efficiently deliver power to a receiver coil as small as 2x2mm with near GHz frequency [4]. However, mm-sized coils make the data link from the transponder to the reader extremely challenging using conventional backscattering methods. To effectively strengthen the signal strength from the transponder, a time-multiplexed, pulse signaling based data readout scheme is therefore proposed.

Such an approach faces two challenges: First, the highly constrained form factor makes it necessary to use a single inductor for both remote power transmission as well as uplink communication from the transponder using pulse signaling. Since pulse signaling cannot occur simultaneously with power transmission to the same inductor, we use a time multiplexing approach where the reader introduces a short time gap in the continuous power signal during which the transponder transmits pulses back to the reader. Since the pulse signaling occurs during the gap in the power transmission, energy for the pulse signaling is stored on integrated capacitors and special steps are taken to reduce the power consumption during pulse signaling.
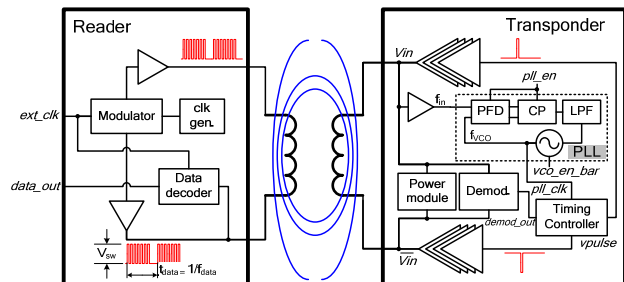

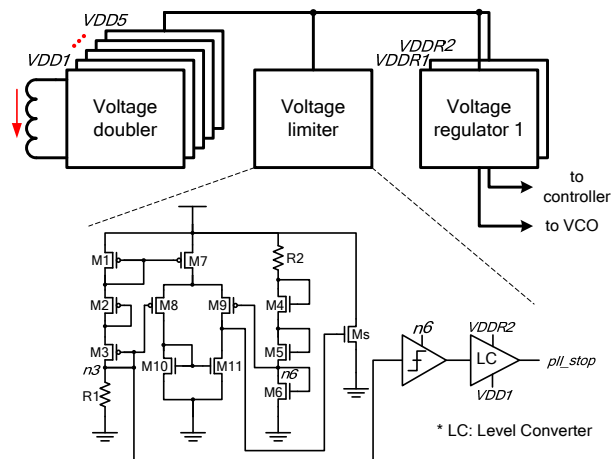Figure 1: Block diagram of the system.

Figure 2: Power harvesting module of the transponder.

The second challenge is that the pulse signaling must be tuned to the resonance frequency of the inductor coil to maximize transmission efficiency. While this matching can be performed by the transponder chip itself, such as in [4], such tuning can be complex and power hungry and hence is ill suited for integration on the transponder chip (particularly in implantable applications where large power transmission requirements may lead to unacceptable tissue heating). However, since the inductor for pulse signaling is also used for power transmission, it is already activated at its resonance frequency by the read during power transmission. Hence, we implement a PLL on the transponder chip that locks to the incoming resonance frequency transmitted by the reader system during power transmission. This simplifies the transponder design and moves the burden of matching the resonance frequency to the reader system. The block diagram of the system is shown in Fig. 1.

During power transmission, the PLL is in a closed-loop mode and replicates the incoming AC frequency. After locking, the PLL is then placed in open loop mode, during which
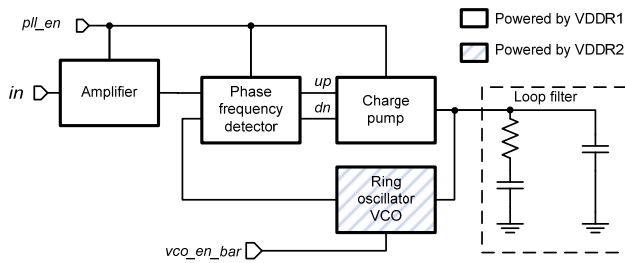
Figure 3: Block diagram of the PLL with power gating capability.

the loop filter holds the bias voltage that is then used to drive the VCO during pulse signaling when a notch in the power transmission envelope is detected. The PLL components other than the VCO are turned off during pulse signaling to reduce power, while still properly exciting the reader with the bias voltage stored in the filter.

III. BUILDING BLOCKS

A. Transponder chip

Since the transponder operates in passive mode during communication, it relies on the power harvesting module shown in Fig. 2 to provide operational power. The voltage doublers are used for AC to DC conversion. To prevent over-stressing of devices, the last stage of rectified voltage VDD5 is constrained to be below 2V by a voltage limiter that was presented in [7]. The voltage limiter also signals the controller (*pll_stop*) when VDD5 is below 1.2V. The purpose of *pll_stop* is to prevent the PLL from consuming all the power that is needed for pulse signaling. Two linear voltage regulators are implemented to supply DC voltages for the transponder. The sensitive VCO requires a dedicated voltage regulator to suppress supply noise from the digital circuits. The voltage regulator is designed at a minimum operating voltage of 770mV to allow the PLL to run at a target resonant frequency of 200MHz (including design margin).

The block diagram of the PLL is shown in Fig. 3. A type II PLL is used to ensure phase locking with unknown initial phase of the VCO. A power gating technique is adapted to eliminate PLL switching power consumption when it is not used. Therefore, assuming that the harvested energy can be stored on capacitors when PLL is power gated, the transponder does not need to maintain peak power of PLL (~20μW) during operation. True single phase clock (TSPC) flip-flops are used to implement the phase frequency detector for high speed operation. The loop filter is designed with 20MHz loop bandwidth by trading-off between stability and tracking speed. The total area of the integrated second-order loop filter is 180μm² in 0.13μm technology.

The operation of the transponder is presented in Fig. 4, showing the power harvesting mode, PLL locking mode, and pulse signaling mode. The operating cycles are synchronized with the system clock of the reader and can be demodulated with the aforementioned notch in the power waveform. When
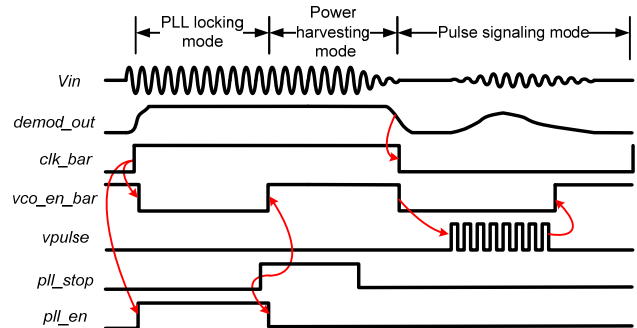

Figure 4: Timing diagram of the operating modes of the transponder.
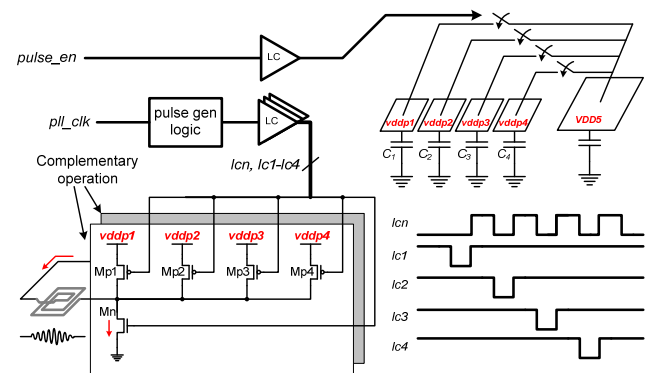

Figure 5: Pulse signaling scheme for the transponder.

the transponder coil starts to oscillate, it enables PLL locking mode by the demodulator output *demod_out*. After a certain cycles, it will finally replicate the frequency/phase of the incoming reference clock V_{in} to the VCO output. The energy range which is dictated by the total power consumption is dominated by the PLL in this case. To extend the energy range, the harvested power is allowed to be lower than the PLL power consumption. This implies that the harvested charge is depleted by the PLL when it is active and the active period should be limited. The PLL will be forced to turn off when the supply voltage seen by the voltage limiter drops below 1.2V and *pll_stop* goes high. However, it is also possible that in close distances the reader is able to provide sufficient power to the PLL continuously. An internal counter is needed to limit the number of cycles to less than 128 so that it can enter the next operating mode. Afterwards, the transponder enters power harvesting mode and starts to restore the supply voltage. In this mode, since the PLL is turned off completely, the main source of power consumption is coming from the bias current of the voltage limiter and voltage regulators, which is less than 2μW combined.

The end of the power harvesting mode is signaled by the attenuation of *Vin*. In response, signal *clk_bar* falls and the VCO is activated by *vco_en_bar*. The data is encoded using on-off keying (OOK) such that no pulse represents a "0" and a
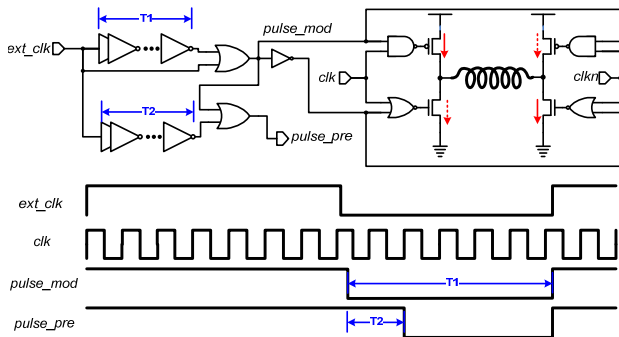
Figure 6: Pulse generation of the reader transmitter.

series of pulses represents a "1". Multiple pulses are used to properly establish the resonant amplitude. Since the same communication channel is used for both power transmission from the reader and data transmission from the transponder, the pulses sent by the transponder may excite the inductor to a degree, causing the envelope detector to falsely recognize the end of the current cycle. Therefore, the controller masks out the *demod_out* signal when *vco_en_bar* is low to prevent double clocking in one cycle.

Fig. 5 shows the pulse signaling scheme when a "1" is sent. During the power harvesting mode, charge is stored on separate capacitors C_1-C_4. In the pulse signaling mode C_1-C_4 are disconnected from the power harvesting module. The controller generates signals *lcn* for the pull-down network and *lc1-lc4* for the pull-up network from the VCO output signal *pll_clk*. Charge stored on C_1-C_4 is translated into AC current that enters the inductor through the MOS switches M_p and M_n.

B. Reader chip

The reader is designed to operate in both power transmitting and data receiving mode with a single coil. Fig. 6 shows the schematics of the pulse generation module that is used to excite AC currents into the transponder coil. When driving at resonant frequency of the output coil and the load capacitors, the output drivers are only used to replenish currents into the coil due to the parasitic loss. The data clock frequency is defined by *ext_clk* and modulated by the carrier frequency of on-chip generated *clk* signal. Two configurable delay lines are used to define the period when the reader stop send power (T1) and the period when the reader is allowed to detect incoming signals (T1-T2). T2 needs to be carefully selected because small value leads to falsely detecting the residual from the damping oscillating LC tank. On the other hand, large T2 means that pulse signaling should happen later after the falling edge of *ext_clk* in order to capture the occurrence of data switching. It extends the non-powering period of the transponder and results to more frequency shift of pulse signaling due to the leakage of loop filter in the PLL. While receiving data from the transponder, the oscillator on the reader is turned off in pulse signaling mode to reduce supply noise. After the incoming signals are AC coupled and properly
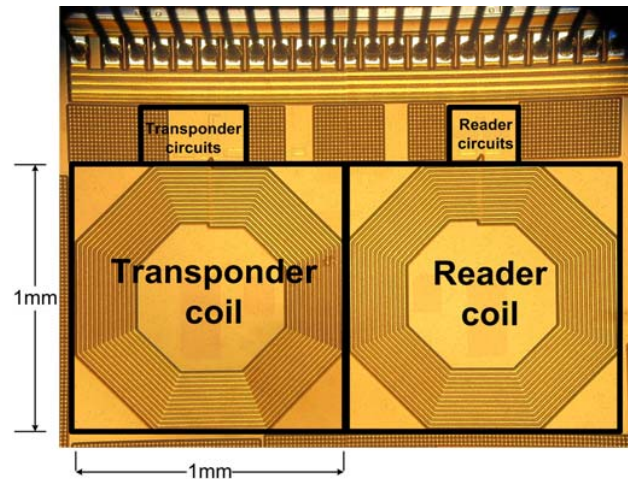

Figure 7: Die photo of the test chip fabricated in 0.13μm CMOS technology.
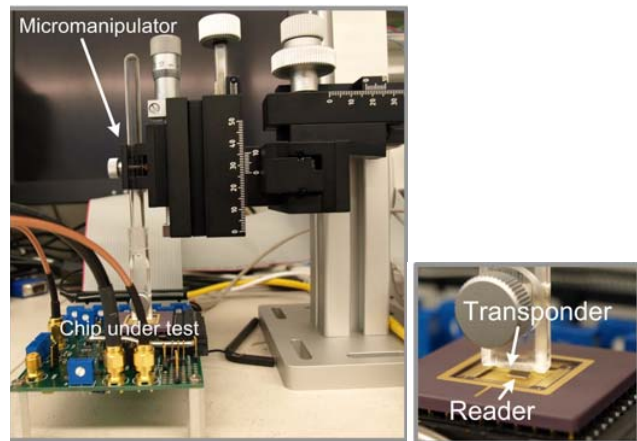

Figure 8: Test setup with the test board and the transponder chip attached to a micromanipulator

biased, the received pulses are amplified to full rail by a differential amplifier. Finally, the output data is decoded by a D flip-flop.

IV. TEST CHIP AND MEASUREMENTS

The test chip is fabricated in 0.13μm CMOS process. The active area of the transponder and the reader is 0.084mm^2 and 0.04mm^2, respectively. The die photo of the test chip is shown in Fig. 7 which shows that most area is taken by the coils.

The measurement setup is shown in Fig. 8. In our experiments, the reader chip is fabricated with an integrated inductor that is identical to that of the transponder for proof of concept and to guarantee matching resonance frequency. In a production system, a discrete coil could be used for the reader. This would allow upsizing of the reader inductor to achieve the same coupling coefficient at an extended distance and also maximize the Q factor. The position of the transponder chip is
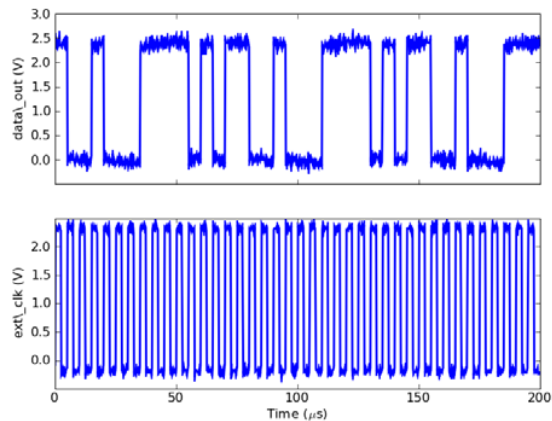
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Figure 9: Measured waveforms.

Figure 10: Measured communication distance (d_{max}) as a function of data rate (f_{data}) and switching amplitude (V_{sw}).

Figure 11: The tolerable horizontal misalignment for a given vertical distance that results in successful communication.

adjusted by a micromanipulator. The micromanipulator provides adjustment steps of 0.1mm in x-axis and y-axis, and 0.01mm resolution in z-axis that dictates the distance between the coils. Measured waveforms of the clock and decoded data transmitted from a 4-bit LFSR on the transponder are shown in Fig. 9.

A contour plot of maximum communication distance (d_{max}) is shown in Fig. 10. The switching amplitude (V_{sw}) of the reader determines the AC current that enters the inductor. At a given data rate (f_{data}), d_{max} monotonically increases with V_{sw}. While the reader power consumption is 16mW, it achieves 1.1mm range (1.1X the coil dimension) with $V_{sw} = 3V$ and $f_{data} = 50kHz$. For comparison, [4] demonstrates 15mm power transmission (no data link) with a 20x20mm transmission antenna and 2x2mm receiver antenna, which is comparable to our achieved communication distance when normalized for coil area. At higher data rates, d_{max} decreases because the harvested energy is also reduced. On the other hand, reducing data rate is not always advantageous since the frequency of pulse signaling relies on the ability of the filter in the PLL to hold the bias voltage. Due to ~20pA of leakage of the bias voltage when the charge pump is off, the frequency deviates from the resonant frequency as the time between refresh increases, resulting in signals with degrading amplitude. Fig. 11 shows the range of the method under horizontal misalignment. At $V_{sw} = 3V$, every 0.1mm of misalignment translates to a loss of ~0.1mm in communication distance. At $V_{sw} = 2.3V$ the impact of misalignment is halved.

V. CONCLUSION

In this work, we present a pulse signaling based method for data readout from inductive coupled coils in short range. The use of time-multiplexing pulse signaling allows the optimization of quality factor for both the reader and the transponder while resonating at the same frequency. It also relaxes the constraint on the receiver's sensitivity by eliminating the dominant noise source during data receiving. A PLL is implemented on the t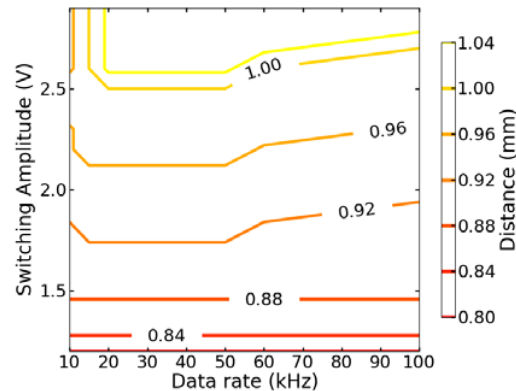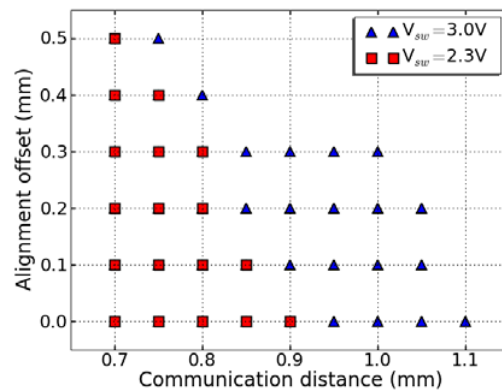ransponder chip to acquire the resonant frequency while harvesting power from the reader. The system is demonstrated with fully integrated chips that were fabricated in 0.13um CMOS technology.

REREFENCES

[1] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7-µW minimum RF input power", *IEEE J. Solid-State Circuits*, pp. 1602–1608, Oct. 2003.

[2] J-P. Curty et al., "Remotely powered addressable UHF RFID integrated system", *IEEE J. Solid-State Circuits*, pp. 2193–2202, Nov. 2005.

[3] K. Katuri, S. Asrani and M.K. Ramasubramanian, "Intraocular Pressure Monitoring Sensors", *IEEE Sensors J.*, pp. 12-19, Jan. 2008.

[4] S. O'Driscoll, A. Poon, T. Meng, "A mm-Sized Implantable Power Receiver with Adaptive Link Compensation", in *IEEE ISSCC Dig. Tech. Papers*, pp. 294-295, Feb, 2009.

[5] R. Xu, Y. Jin and C. Nguyen, "Power-efficient switching-based CMOS UWB transmitters for UWB communications and Radar systems", *IEEE Trans. Microw. Theory*, pp. 3271-3277, 2006.

[6] N. Miura, et al, "A 0.14pJ/b Inductive-Coupling Inter-Chip Data Transceiver with Digitally-Controlled Precise Pulse Shaping", in *IEEE ISSCC Dig. Tech. Papers*, pp. 358-608, 2007.

[7] Y-S. Lin, D. Sylvester and D. Blaauw, "Sensor Data Retrieval Using Alignment Independent Capacitive Signaling", in *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 66-67, 2008.

T-25-4

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