Interconnect Performance Corners considering Crosstalk Noise

Ravikishore Gandikota, David Blaauw and Dennis Sylvester
EECS, University of Michigan
{*gravkis, blaauw, dennis*}*@eecs.umich.edu*

***Abstract*— Process induced variations in the interconnect capacitance and resistance have resulted in significant uncertainly in the interconnect delay. In this work, we propose a new method to compute the interconnect corner considering coupling-noise due to simultaneous switching of aggressors. In prior approaches, the interconnect corners were computed under the assumption that the aggressor nets are not switching and no coupling-noise is injected on the victim net. In this paper, we first show that the interconnect corners obtained under such assumptions could in reality be much different from the true interconnect corner and could therefore result in optimistic delay analysis, particularly for fast-path analysis performed to check hold time violations. We also show that in some cases, the interconnect corner may not lie at an extreme point of the process variation range. In this work, we use the Elmore delay metric to efficiently search for the correct interconnect corner of the victim stage considering delay noise. We then show experimental results to verify the effectiveness of our proposed approach and demonstrate that the traditional approaches of computing the interconnect corners could lead to errors of up to 60% on a net by net basis.**

I. Introduction

Aggressive scaling of device dimensions into the nanometer regime has led to a considerable reduction in gate delays. However, due to less aggressive interconnect scaling, wire delays have not reduced in proportion to gate delays. Hence, wire delays and especially the global interconnect delays, now contribute significantly to the total circuit delay. Also, with process-technology scaling, the spacing between adjacent interconnect wires keeps shrinking which leads to an increase in the amount of parasitic coupling capacitance between the wires. A net under analysis is referred to as the *victim* and all neighboring nets which are capacitively coupled are termed as *aggressors*. The transition on the victim can be affected by the simultaneous switching of the aggressor nets due to the transfer of charges through the coupling capacitances. This change in the victim stage delay due to the simultaneous switching of aggressors is referred to as *delay noise*. For high performance VLSI designs, delay noise contributes to a significant portion of the total circuit delay and must be accurately modeled while performing the signoff timing verification [1], [2].

Imprecise control of photolithography equipment leads to a significant variability [3] in the geometry and the material properties of interconnects and devices. For example, deviations in the implant dose can significantly affect the threshold voltage and the electrical parameters of a device [4], [5]. Similarly, the vertical and lateral dimensions of the interconnect wires are affected by the variability in the metal deposition process and the dishing effects during metal etching. Furthermore, the variability in the manufacturing process is expected to exacerbate as the feature sizes continue to shrink in future technology nodes. In the past, the variability in devices was the dominant source of variation in the circuit delay. However, with the ever increasing contribution of interconnect delay, it has now become necessary to accurately model the variability in the interconnects while performing the timing verification of designs.

The variation in the interconnect resistance and capacitances are correlated since they are dependent upon the interconnect physical dimensions. For example, wire resistance is maximized for small-narrow wires and wire capacitance is maximized for thick-wide wires. Therefore, assuming the worst-case values for both the wire resistance and the wire capacitance is pessimistic since both cannot be maximized (or minimized for hold-time analysis) in the same interconnect process corner [6]. Therefore, an accurate analysis must account for the correlations between the wire resistance and capacitance. In [7], [8], it was shown that best/worst case delay does not always occur at the extremes of the interconnect dimensions. The interconnect corners was instead computed by using a simulation based approach which searched for the optimal interconnect parameters within their range of variations. In [9], the interconnect corners were computed considering the variability in both the interconnect dimensions and the gate drive strength. In [10], [11] statistical analysis of the interconnect delay was performed using model order reduction techniques.

The variations in the interconnect coupling capacitance C_c and the interconnect ground capacitance C_g are strongly correlated and an increase in the interconnect dimensions leads to an increase in the magnitude of both C_c and C_g. The victim stage delay always increases with an increase in the victim ground capacitance. However, when coupling-noise is injected onto the victim, the victim stage delay can actually *decrease* with an *increase* in the interconnect coupling capacitance. This scenario occurs when the victim-aggressor nets are switching in the same direction and the interconnects have substantial capacitive coupling. Hence, an increase in the coupling capacitance leads to an increase in the magnitude of the delay noise which in turn results in a lower victim stage delay. Therefore, for such cases, the best-case interconnect corner having the minimum victim stage delay coincides with maximum coupling capacitances.

However, prior approaches [7], [8] compute the interconnect corners under the assumption that the aggressor nets are

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not switching and that there is no coupling-noise injected on the victim net. Hence, the interconnect corners reported by them could in reality be much different from the *true* interconnect corner. Therefore, previous approaches which do not distinguish between the interconnect coupling and the interconnect ground capacitance can result in optimistic analysis. In this work, we propose to compute the *true* interconnect corner for the victim by accounting for the effects of coupling-noise due to simultaneous switching of aggressors. We use the Elmore delay metric to efficiently search for the correct interconnect corner of the victim stage considering delay noise. We then show experimental results to verify the effectiveness of our proposed approach and demonstrate that the traditional approaches of computing the interconnect corners could lead to errors of up to 60% on a net by net basis.

The remainder of the paper is organized as follows: In Section II, we analyze the problem of finding the best/worst case interconnect performance corners considering the impact of coupling noise in greater detail. In Section III, we present an approach to compute the interconnect corners by also considering the effects of delay noise. In Section IV, we show experimental results which confirm the effectiveness of our approach and in Section, V we conclude the paper.

II. Problem Analysis

In this section we analyze the problem of computing the best/worst case victim stage delay considering process variations in both the devices and the interconnects. Figure 1 shows the cross section of the interconnect layers, where W and T represent the lateral width and the vertical thickness of an interconnect. The spacing between adjacent interconnects on the same layer is given by S and the inter-layer dielectric (ILD) thickness is given by H. Due to the variations in oxide deposition and the chemical mechanical planarization (CMP) process, the ILD thickness H can vary substantially (e.g. $[H_{min}, H_{max}]$) within a die due to layout pattern dependencies

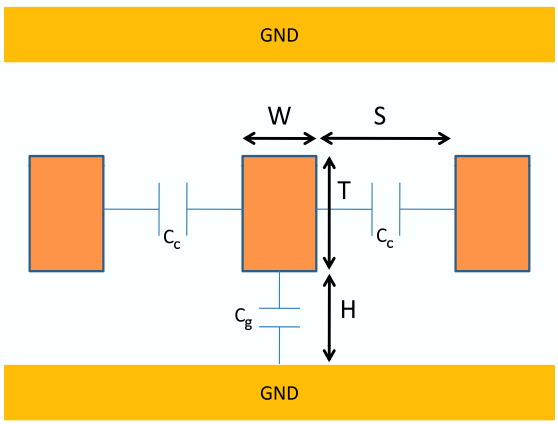

Fig. 1. Cross Section of Interconnect Metal Layers

[3]. Also, the variability of the photolithography equipment and dishing/erosion effects can cause significant variations in the width and thickness of the interconnect (viz. $W \in [W_{min}, W_{max}]$ and $T \in [T_{min}, T_{max}]$). Note that the variations in the interconnect parameters can be assumed to be mutually uncorrelated since they are caused by the different steps within the manufacturing process. The exception being the variations in W and S which are assumed to be perfectly negatively correlated since an increase in the interconnect width would lead to an equivalent decrease in the lateral spacing.

The interconnect *performance* corner (with no coupling-noise) can be obtained by performing exhaustive simulations at different interconnect *process* corners. Traditionally, the interconnect delay is assumed to be dominated by either the wire resistance or the wire capacitance. Therefore, in order to reduce the search space, worst-case process corners are often heuristically chosen such that they maximize either the interconnect capacitance or the interconnect resistance. Note that the wire resistance is maximized for thinner/smaller wires (W_{min}, T_{min}) and conversely wire capacitance is maximized for thicker/taller wires ($W_{max}, T_{max}, H_{min}$). Similarly the *best-case* performance corner (for hold-time analysis) is assumed to coincide with the interconnect corner having minimum wire resistance (W_{max}, T_{max}) or wire capacitance ($W_{min}, T_{min}, H_{max}$). However, the interconnect corners have to be combined with the Process-Voltages-Temperature (PVT) corners of a design. Hence, the traditional approach presented above essentially *doubles* the total number of corners that have to be analyzed for a design.

It was shown in [7] that the above heuristic accurately computes the worst-case interconnect performance corners. However, the best-case interconnect performance corner does not necessarily coincide with the minimum wire resistance/capacitance corners and the above heuristic could result in an optimistic analysis. Several simulation-based approaches have been proposed [7], [8], [9] to search for the best-case interconnect corner such that the stage delay is minimized. However, in all previous approaches the best-case corner is computed under the assumption that the aggressor nets are not switching. In other words, the victim stage delay is simulated by assuming that the floating coupling capacitances are grounded. With coupling capacitance accounting for more than 85% of the total wiring capacitance [12], one cannot ignore the delay noise on the victim net which occurs due to the simultaneous switching of the aggressor nets. Hence, the *true* best-case interconnect corner for the victim must incorporate the change in victim stage delay due to delay noise. The analysis is further complicated due to several reasons which are explained as follows.

A. Non-Monotonic Victim Stage Delay

The victim stage delay exhibits a non-monotonic relationship with the interconnect width W (see Figure 4). At very small interconnect widths, the victim interconnect has a significant amount of resistance. Therefore, in this region, the victim stage delay is dominated by the interconnect

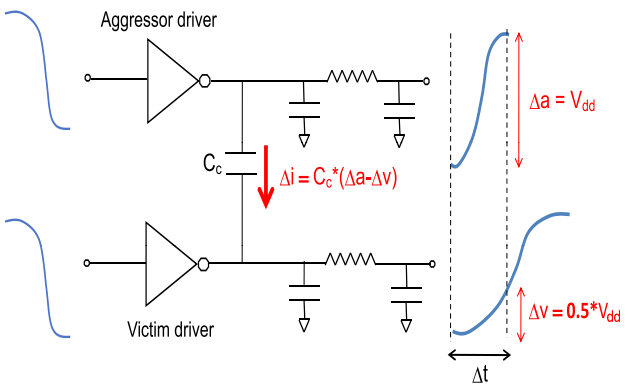

Fig. 2. Switching of aggressor-victim nets in the same direction

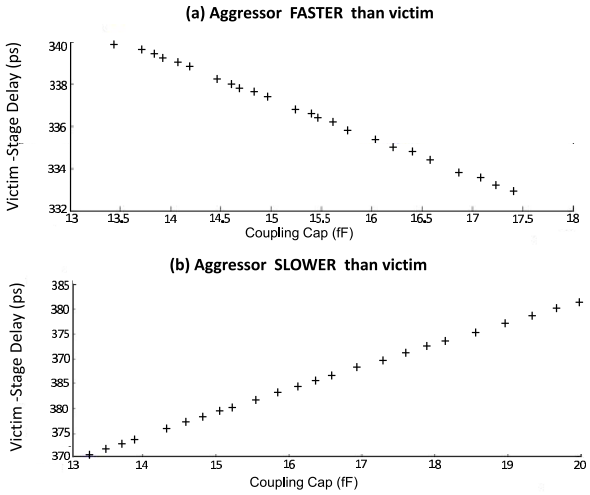

Fig. 3. Dependence of victim stage delay on coupling capacitance

resistance and is very sensitive to the variations in the interconnect resistance. Hence, a decrease in interconnect width W leads to an increase in the magnitude of interconnect resistance and consequently an increase in the victim stage delay. At larger interconnect widths, the interconnect has a significant amount of capacitance and the victim stage delay is dominated by the interconnect capacitance. A further increase in the interconnect width would lead to an increase in both the interconnect coupling and the ground capacitances. Therefore, at larger interconnect widths, the victim stage delay is directly proportional to W. The victim stage delay is minimized at an intermediate interconnect width ($W_{opt} = 0.037\mu m$ in Figure 4). A similar non-monotonic relationship can be observed when we obtain the victim stage delay as a function of the interconnect thickness T.

Process variations can lead to a variability in the interconnect dimensions (e.g. $[W_{min}, W_{max}]$). The victim stage delay is minimized at $W = W_{min}$, if the interconnect is capacitance dominated and the range of feasible variations i.e. $[W_{min}$, $W_{max}]$ lies to the right of W_{opt}. Similarly, for resistance dominated interconnects, the victim stage delay is minimized at $W = W_{max}$. However, there can be cases when W_{opt} lies inside the variation range $[W_{min}$, $W_{max}]$. For all such cases, it would be erroneous to assume that the best-case interconnect corner coincides with either W_{min} or W_{max}. Therefore, traditional approaches which maximize only the wire resistance or capacitance can miss the true interconnect corner.

B. Victim Stage Delay vs C_c

We now illustrate with an example the context-dependency of the victim stage delay with respect to the coupling capacitances. In Figure 2, we can see capacitively coupled aggressor-victim nets with falling transitions at the inputs of the drivers. In this example, the aggressor driver is lightly loaded relative to the victim and hence it has a relatively faster rising output transition when compared to the victim transition. Therefore, the aggressor transition is completed within the time interval Δt during which the victim transition rises only up to the $0.5V_{DD}$ voltage level. The charges transferred through the coupling capacitance C_c during the time interval Δt depends only on the magnitude of the coupling capacitance and the voltages at the extremes of the coupling capacitance. The total current flowing into the victim node (Q) through the coupling capacitance C_c can mathematically be expressed as,

$$Q(\Delta t) = \int_0^{\Delta t} i_{C_c} \cdot dt = C_c * (\Delta a - \Delta v) \quad (1)$$

where Δa and Δv represent the change in the aggressor-victim output voltages within the time interval Δt respectively. Hence, if the aggressor output transition rises faster than the victim (i.e. $\Delta a > \Delta v$), then it leads to a positive injection of current into the victim node. This injection of current into the victim node results in a speedup of the victim transition when compared to a scenario where we have a quiet (non-switching) aggressor. It follows from Equation 1 that the magnitude of the charge Q injected through the coupling capacitance is directly proportional to the magnitude of coupling capacitance. Hence, an increase in the coupling capacitance will lead to a further speedup of the victim transition due to an increase in the injected charge Q.

The above relationship is verified in Figure 3 where we plot the victim stage delay as a function of the coupling capacitance C_c. The simulations were performed using the HSPICE simulator with detailed parasitics extracted in the $65nm$ technology node. The coupling capacitance was varied by changing the lateral spacing between the aggressor and victim nets. As discussed earlier, we find that the victim stage delay *decreases* with an increase in coupling capacitance C_c (in Figure 3a) provided the aggressor transition is faster than the victim. A similar experiment was performed by changing the relative loadings of the aggressor-victim drivers such that the victim transition is now faster than the aggressor transition (i.e. $\Delta v > \Delta a$). In this case, there is a net outflow of current from the victim node to the aggressor node through the coupling capacitance. An increase in the coupling ca-

pacitance would lead to an increase in the magnitude of the total coupling current and finally result in a further slowdown of the victim transition. Hence, we observe that the victim stage delay *increases* with an increase in the magnitude of the coupling capacitance (in Figure 3b) given that the aggressor transition is slower than the victim.

C. Correlations between the C_c and C_g

We know that the interconnect coupling capacitance C_c and the interconnect ground capacitance C_g are strongly correlated since they depend on the interconnect physical dimensions. An increase in the size (W, T) of an interconnect leads to an increase in the magnitude of both C_c and C_g. When the aggressor nets are not switching and there is no coupling-noise, the victim stage delay always increases with an increase in total wire capacitance ($C_g + C_c$). However, as shown earlier, with coupling-noise the victim stage delay can either increase or decrease with an increase in the coupling capacitance (C_c). Therefore, it is difficult to predict apriori, whether an increase in the total wire capacitance ($C_g + C_c$) would lead to an increase in the victim stage delay when there is coupling-noise.

In previous approaches, the best-case interconnect corner is obtained by using the total wire capacitance ($C_g + C_c$) and assuming no switching of aggressors. With coupling capacitance sometimes accounting for more than 85% of the total wiring capacitance [12], the interconnect corner computed using the above assumption could result in significant errors.

III. Proposed Approach

In the previous section we saw that the victim stage delay can either increase or decrease with an increase in the interconnect coupling capacitance. Hence, even for a capacitance dominated interconnect, the best-case performance corner may not coincide with the minimum interconnect capacitance corner (i.e. smallest sized wires). A *bruteforce* approach to compute the best-case interconnect corner would be to sweep all the interconnect parameters (W, S, T, H) within their range of variations (e.g. $W \in [W_{min}, W_{max}]$) and select the corner which results in the minimum stage delay. It can however be noted that the interconnect capacitance is inversely proportional to the ILD thickness H and the interconnect resistance is independent of H. Consequently, the interconnect delay is always minimized at H_{max} [8]. We also know that the variations in W and S are perfectly negatively correlated. Therefore, the bruteforce approach to locate the best-case interconnect corner would require a two-dimensional sweep in the parameters W and T. However, the total number of simulations required in a bruteforce approach can be prohibitively expensive.

In this section, we present an approach to find the best-case interconnect corner by using the Elmore delay metric [13]. The Elmore delay of an RC tree provides a dominant pole approximation of the interconnect delay and can be computed very efficiently as follows,

$$Elmore\ Delay = \sum_{i=0:N} \left(R_i \sum_{k=i:N} C_k \right), \tag{2}$$

where N refers to the number of nodes in the RC tree. With the root node of the RC tree is connected to an equivalent driver output resistance R_0, the Elmore delay provides a first-order approximation of the actual stage delay.

It must be noted that Elmore delay is only defined for an RC tree where all the node capacitances have a terminal connected to the ground. In order to compute the Elmore delay of the victim stage, the coupling capacitance of the victim must be decoupled from the aggressor node. Therefore, we must find an equivalent Miller capacitance which models the change in the aggressor voltage (see Figure 5). If the aggressor-victim switch in the same direction, the effective Miller coupling capacitance can be written as,

$$C_c^{eff} = C_c \left(1 - \frac{\Delta a}{\Delta v} \right) \tag{3}$$

where Δa and Δv are the changes in the voltages across the coupling capacitances at the victim and the aggressor nodes. In [14], [15] techniques were proposed to accurately compute the Miller coupling capacitance C_c^{eff} by iteratively updating the victim-aggressor waveforms and refining the values of Δa and Δv. The C_c^{eff} can also be computed very efficiently by approximating the victim-aggressor waveforms with ramps and using the respective slew rates in Equation 3. Once the coupling capacitance is decoupled from the aggressor node, the Elmore delay of the victim can be computed using the Equation 2.

While the Elmore delay may not always be very accurate, its usefulness lies in the fact that it can be computed efficiently and that it accurately captures the relationship between the actual stage delay and the interconnect parameters. In order to validate the above claim, we plot in Figure 4 the victim stage delay as a function of the victim interconnect width W. The simulations were performed for the circuit shown in Figure 2 in the 65nm

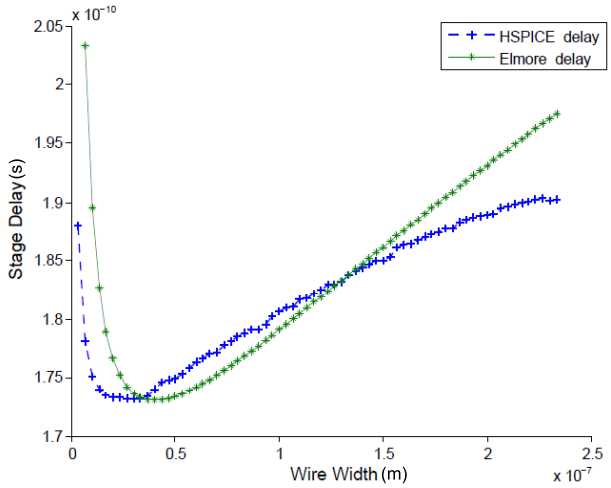

Fig. 4. Elmore delay vs HSPICE delay as a function of wire width W

technology node with the following interconnect parameters, $T = 0.35\mu m$, $S = 0.25\mu m$, $H = 0.2\mu m$ and $L = 150\mu m$. The interconnect resistance/capacitances (per unit length) were obtained as functions of the interconnect parameters [16] using the following equations,

$$R = \frac{\rho}{W \cdot T}$$

$$\frac{C_g}{\varepsilon_{ox}} = 1.171 \left(\frac{S}{S+1.51H}\right)^{0.7642} \cdot \left(\frac{T}{T+4.532H}\right)^{0.1204} + \frac{W}{H} + 2.217 \left(\frac{S}{S+0.702H}\right)^{3.193}$$

$$\frac{C_c}{\varepsilon_{ox}} = 1.158 \left(\frac{W}{W+1.874S}\right)^{0.1612} \cdot \left(\frac{H}{H+.9801S}\right)^{1.179} + 1.144 \frac{T}{S} \left(\frac{H}{H+2.059S}\right)^{0.0944} + 0.7428 \left(\frac{W}{W+1.592S}\right)^{1.144}$$

$$\rho = 2.2\ \mu\Omega - cm \quad , \quad \varepsilon_{ox} = 3.9 * 8.85 * 10^{-14} F/cm. \tag{4}$$

In Figure 4, it can be noted that the victim stage delay exhibits a *convex* relationship with the interconnect width W. In this experiment, the victim stage delay was minimized at an intermediate width of $W_{opt} = 0.037\mu m$. We also plot in Figure 4 the Elmore delay of the victim as a function of interconnect width W. It can be seen that the Elmore delay nicely captures the fidelity of the actual stage delay with respect to W. In the above experiment, the Elmore delay was minimized at $W = 0.4\mu m$. Since the Elmore delay tracks the actual stage delay very well and can be computed very efficiently, we use it instead in order to compute the best-case interconnect corner.

A bruteforce approach would require a 2-D sweep with the parameters W and T within their range of variations (e.g. $W \in [W_{min}, W_{max}]$) and the computation of the Elmore delay at every point. However, one can leverage the convex nature of the relationship between the stage delay and the interconnect width W and easily evaluate whether the interconnect delay is minimized at the boundaries W_{min} or W_{max}. We first compute the sensitivity of the Elmore delay with respect to width W at the boundaries W_{min} and W_{max}. If both the sensitivities are positive, it implies that the range of feasible interconnect widths [W_{min} , W_{max}] lies to the right of the minimum delay width W_{opt}. For such cases, the feasible interconnect width at which the stage delay is minimized would be at $W = W_{min}$. Similarly, if the sensitivities of the Elmore delay at the width boundaries are negative, then it implies that the range of feasible interconnect widths lie to the left of W_{opt}. Hence, for such cases, the stage delay is minimized at $W = W_{max}$. For cases where the sensitivities at the boundaries differ in sign, it can be inferred that W_{opt} lies within the range [W_{min} , W_{max}]. A gradient based approach (such as Newton-Raphson) could be used to search for W_{opt}. A similar approach could be used to compute the optimal interconnect thickness T_{opt}. Since the interconnect corners are evaluated using the Elmore delay, the overall algorithm to find the best-case interconnect corner is runtime efficient. In the results section, we will now show the accuracy of the interconnect corner computed using the above approach.

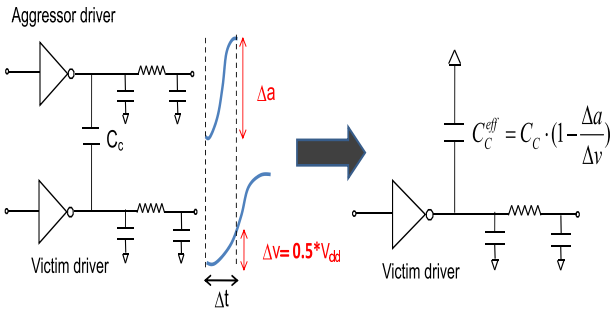

Fig. 5. Victim stage analysis with Miller coupling capacitance

IV. Results

In this section, we will show experimental results that verify the accuracy and effectiveness of our proposed approach for computing the best-case interconnect corner. We first show that significant error can be introduced when the best-case corner is computed under the assumption that the aggressor nets are not switching. Experimental results confirm the fact that if the coupling-noise is not accounted for, then one could potentially miss the true interconnect corner leading to optimistic delay analysis.

The experiments were performed in the $65nm$ technology node using the fully coupled victim-aggressor circuit topology shown in the Figure 2. In the above circuit, the victim-aggressor interconnect wires had the following dimensions $W = 0.14\mu m$, $H = 0.2\mu m$ and $T = 0.35\mu m$ as suggested in [17]. An intra-die variability of 30% was assumed for the interconnect parameters W and T. Multiple instances of the aggressor-victim coupled circuit were created by changing the parameters of the drivers and the interconnects. A total of 32 different circuits were instantiated with permutations among the following parameter values: the victim input slew rate $(10ps, 200ps)$, the victim-aggressor driver strength $(2X, 12X)$ with respect to the minimum-sized drivers, the interconnect length $(50\mu m, 200\mu m)$ and the aggressor-victim interconnect spacing S $(0.14\mu m, 0.45\mu m)$.

In order to confirm the importance of considering coupling-noise in our analysis, we find the best-case interconnect corners under the following two scenarios (1) the aggressor net is not switching, and (2) the aggressor net is switching in the same direction as the victim net. In both cases, the best-case interconnect corner was obtained by exhaustively sweeping the parameters W and T with a discretization step size of $1nm$. At each step, the corresponding variation in the interconnect capacitances/resistances was obtained by using the Equation 4 and the victim stage delay was obtained using the HSPICE circuit simulator. In case (1) the input of the aggressor driver is assumed to be grounded.

In case (2) the aggressor transition was enumerated with a discretization step size of $2ps$ and the optimal aggressor-alignment was computed such that it resulted in the minimum victim stage delay.

It is apparent that the interconnect corner obtained in case (2) is the true (golden) interconnect corner since it results in the minimum victim stage delay with coupling-noise. In comparison, the interconnect corner obtained in case (1) results in the minimum victim stage delay when there is *no* coupling-noise. Hence, if the interconnect corners obtained in both cases differ appreciably, the latter could lead to an optimistic stage delay when analyzed with coupling-noise due to a switching aggressor. In Figure 6, we compare using a bar plot, the victim stage delays obtained with coupling-noise at both the interconnect corners for each of the 32 circuits.

It can be observed that the victim stage delay reported in case (1) has large errors for several of the circuits. When these circuits were further analyzed, it was seen that the interconnect corner obtained for case (1) coincided with the minimum sized wires having the smallest wire capacitance. In contrast, the golden corner obtained in case (2) coincide with the tallest wires such that the coupling capacitance is maximized. Hence, for these circuits, it can be inferred that coupling-noise significantly contributes to the victim stage delay and maximizing coupling capacitance results in the minimum victim stage delay. A histogram of the percentage error in victim stage delay with respect to the golden victim stage delay for each circuit is also shown in Figure 6. We see that an error of up to 60% is observed in the victim stage delay when coupling-noise is not accounted for in the computation of the best-case interconnect corner.

A third set of interconnect corners were constructed for each circuit by instead using the Elmore delay as a proxy for the victim stage delay. A two-dimensional bruteforce sweep was performed in the W and T parameter space and the Elmore delay was computed at each step assuming a switching aggressor. Finally the interconnect corner which resulted in the smallest Elmore delay was reported as the best-case interconnect corner. In Figure 7, it can be seen that the interconnect corner reported above matches closely with the golden corner obtained earlier. The maximum error in the victims stage delay was less than 3% across all circuits. Therefore, Elmore delay indeed captures the fidelity of the actual stage delay with respect to the interconnect parameters and can be used to accurately compute the best-case interconnect corner.

A. MCNC benchmark circuits

It can be noted that the hold-time violations are typically caused by fast paths between pipeline stages with single or no logic gates. We saw earlier that the interconnect corner computed by assuming no coupling-noise could lead to errors of up to 60% in the stage delays when there is a significant amount of coupling capacitance. In comparison, the MCNC benchmark circuits are all combinatorial circuits and all the fast paths reported in Table I have a circuit depth ranging between $2-8$ stages. Therefore, in most cases they are not representative of the fast-paths that cause hold-time violations in a design. However, for the sake of completeness, we show experimental results to verify the effectiveness of our proposed approach on MCNC benchmark circuits. These benchmark circuits were synthesized in 130nm technology and then placed-and-routed by using a commercial APR tool. A commercial parasitic extraction tool was used to extract the distributed interconnect RC values. A coupling-noise analysis engine was implemented in C++ programming language and the circuit delay was computed using industrial timing libraries.

In Table I, we list the fast-path delays for each of the MCNC circuits obtained at different interconnect corners. A $3\sigma/\mu$ intra-die variability of 30% was assumed for the interconnect parameters W and T. In Column 2, we report the fast-path delays at the nominal interconnect corner by assuming that all aggressors coupled to the path are not switching. In Column 3, we update the fast-path delays

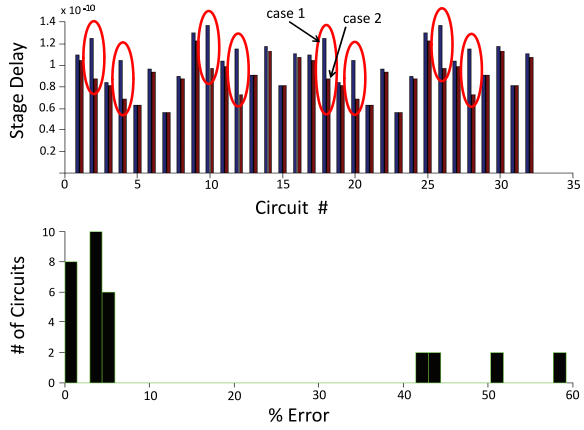

Fig. 6. Interconnect corner with no coupling-noise vs golden corner

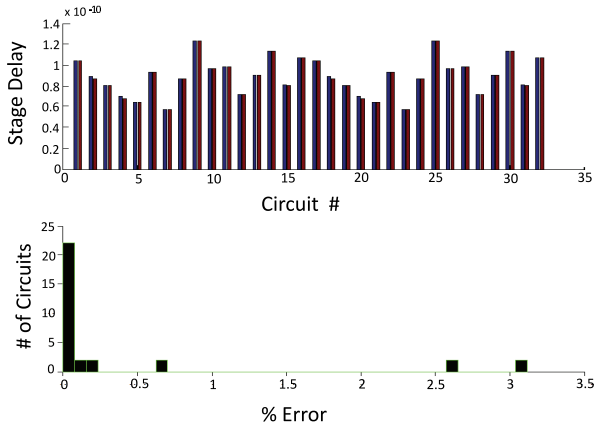

Fig. 7. Interconnect corner using Elmore delay vs golden corner

TABLE I

FAST-PATH DELAYS FOR MCNC BENCHMARK CIRCUITS

ckt	Nominal Delay(ps)	Delay with Xtalk(Nominal)	Delay with Xtalk(Min Cap)	Delay with Xtalk(Proposed Corner)	%Error in Delay-Noise
i1	60.7	49.7	48.9	47.8	9.32
i2	83.4	73.7	72.2	70.5	15.17
i3	42.97	37.1	36.3	35.5	11.99
i4	49.3	40.5	40.3	40.3	0
i5	42.8	39.4	38.2	38.2	0
i6	64.2	49.4	48.2	46.7	9.37
i7	61.5	48.1	46.8	45.4	9.52
i8	137.5	117.7	117.0	115.4	7.80
i9	180.1	167.2	166.7	166.7	0
i10	289.8	285.4	282.6	282.6	0

at the nominal interconnect corner by accounting for the speedups due to coupling-noise. Next, we construct an interconnect corner with minimum total wire capacitances by using the smallest sized interconnects (W_{min}, T_{min}). Since the local interconnects have negligible wire resistances, they are capacitance dominated. Therefore, the smallest sized wires with the least wire capacitance would lead to minimum path delays provided there is no coupling noise. In Column 4, we report the fast-path delays with coupling-noise computed at the minimum capacitance corner. Using the proposed Elmore delay based approach, we then find the *true* best-case interconnect corner for each victim net on the fast paths. In Column 5, we report the fast-path delays obtained at the interconnect corner constructed above. One can observe that the best-case interconnect corner does not always coincide with the minimum capacitance corners. Therefore, the path delays reported in Column 5 are always lesser than that obtained at the minimum capacitance corner. In the final column, we report the percentage error in the total delay noise of the paths obtained at the minimum capacitance corner. For a few circuits (e.g. $i10$), the minimum interconnect capacitance corner results in the minimum path delay. However, for other circuits (e.g. $i2$) the minimum capacitance corner leads to an error of up to 15% in the path delay noise.

V. CONCLUSIONS

In this work, we proposed a new method to compute the best-case interconnect corner considering coupling-noise due to simultaneous switching of aggressors. In prior approaches, the best-case interconnect corners were computed under the assumption that the aggressor nets are not switching and no coupling-noise is injected on the victim net. We first showed that the interconnect corners obtained under such assumptions could result in optimistic delay analysis. We used the Elmore delay metric to efficiently search for the best-case interconnect corner of the victim stage considering delay noise. Experimental results verified the effectiveness of our proposed approach and demonstrated that the traditional approaches of computing the interconnect corners could lead to errors of up to 60% on a net by net basis.

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