# *Circuit Design Advances to Enable Ubiquitous Sensing Environments*

Mingoo Seok, Scott Hanson, Michael Wieckowski, Gregory K. Chen, Yu-Shiang Lin, David Blaauw, Dennis Sylvester
University of Michigan, Ann Arbor, MI, U.S.A
dennis@eecs.umich.edu

**Abstract - This paper describes critical circuit building blocks for emerging sensing applications, particularly those where volume, and therefore power consumption constraints are orders of magnitude below current state of the art. Developments in ultra-low power microprocessors and memories are described, along with sub-nW timekeeping circuits, pW voltage references, and efficient DC-DC voltage conversion circuits at sub-µA current loads. Taken together, these circuit design advances point to a vision of true mm$^3$ low-cost sensing nodes with hybrid power sources, i.e., scavenged and micro-battery, providing long lifetime and reliable operation.**

## I. INTRODUCTION

Cubic millimeter systems promise to deliver enormous value to a wide range of wireless sensor applications. For example, general environmental sensor systems benefit from the lower costs associated with a small volume. Also, miniaturization of implantable sensing systems such as intra-ocular pressure sensors [1][2] enables surgeons to use less invasive procedures.

Although the size of circuit components can be reduced due to advances in semiconductor technology, the required battery size for a target lifetime is the major bottleneck to achieving the small volume. Given a 1mm$^2$ zinc/silver battery with a capacity of 100uAh/cm$^2$ and output voltage of 1.55V [2], system power consumption should be limited to 177pW to guarantee one year of battery life. This power source limitation provides motivation for a system that consumes minimal power.

In this work, we describe our most recent progress in designing circuit components of a 1mm$^3$ sensing system. We start with our efforts to reduce the energy consumption of an Ultra Low Power (ULP) microprocessor and Static Random Access Memory (SRAM) [3]. We particularly focus on standby mode, where the dominant portion of total energy is consumed, due to the small duty cycle of the sensing applications. We then discuss three analog building blocks. First, a watchdog timer using a program-and-hold technique is described that consumes 100-150pW [4]. Such a low power timer is needed to replace crystal oscillators, which consume a considerable amount of power and volume. Second, a 2.2pW ULP voltage reference, called a 2T voltage reference, is discussed [5]. It uses only two transistors biased at subthreshold regimes, improving power efficiency over traditional voltage references by ~4 orders of magnitude. Finally, we describe a DC-DC converter that provides a reliable supply voltage to systems [6]. It is challenging to design a high efficiency DC-DC converter for sub-µA load current since even modest circuit overheads significantly degrade power efficiency. A hybrid topology, consisting of a Switched Capacitor Network (SCN) and a linear regulator, is used along with multivibrator delay elements for clock generations. The 2T voltage reference is employed in the DC-DC converter. After discussing progress in circuit design elements, we conclude the paper by discussing remaining challenges and potential solutions.

## II. ULP PROCESSOR AND MEMORY DESIGN

Dramatic energy reduction can be achieved in digital logic by reducing supply voltage ($V_{dd}$), due to the quadratic dependence of switching energy on $V_{dd}$. It has long been known that CMOS circuits continue to function with $V_{dd}$ well below the threshold voltage ($V_{th}$), therefore aggressive voltage scaling into the subthreshold regime ($V_{dd}<V_{th}$) is possible with careful design practices [7][8]. To initially explore low voltage operation, we fabricated an 8-bit microprocessor with 1.5kb instruction memory and 1kb data memory in a 0.13µm process, which consumes 3.5pJ/inst at subthreshold $V_{dd}$ [9].

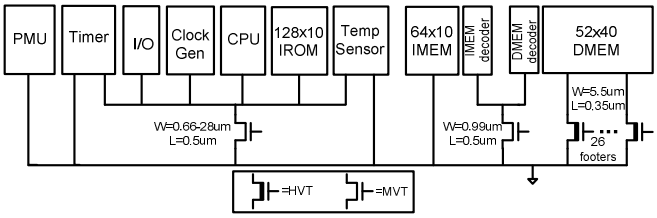


**Figure 1. Power gating domains in the Phoenix Processor.**

While the active energy is greatly reduced by $V_{dd}$ scaling, standby power was overlooked in early ultra-low power designs, which renders them sub-optimal in total energy consumption in common sensing applications with very low duty cycles. We therefore designed the Phoenix Processor to consume extremely low power in both active and standby modes by following comprehensive standby strategies across the design hierarchy [3]. In this section, we discuss two such approaches.

One of the critical pieces of our standby strategy is a unique approach to Power Gating Switches (PGS). As shown in Figure 1, several modules such as CPU, IROM, clock generator, and IO block can be completely turned off during standby mode to minimize power consumption. Typically, a wide power gating switch (~10% of total NFET width) is used to minimize the performance penalty due to the voltage drop across the switch. However, we chose a very small power gating switch of 0.66µm, or only 0.01% of total NFET width, since minimizing standby power is a more important design goal here than performance. The small power gating switch incurs active energy overhead in two ways. First, the voltage drop across the minimal PGS (maximum of ~100mV) degrades circuit performance and thus increases the leakage portion of active energy. Second, the PGS itself consumes power through the voltage drop across the switch. To compensate for the active energy penalty, we co-optimize the supply voltage with the power gating switch width [10].

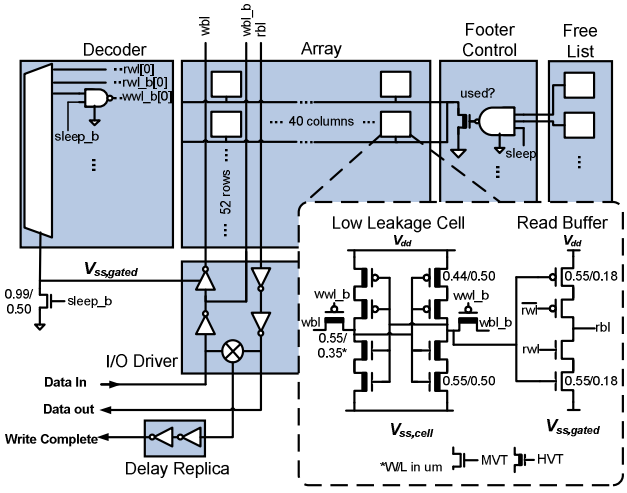


**Figure 2. Low leakage bitcell and DMEM architecture.**

While the CPU and other non-retentive modules can be power gated, SRAM modules such as Instruction Memory (IMEM) and Data Memory (DMEM) cannot be gated due to their data retention requirements. Therefore, we design a low leakage custom SRAM module. It uses the custom bitcell shown in Figure 2. The cross-coupled inverters and access transistors use high-$V_{th}$ devices. Stack forcing and gate length biasing are also used to further reduce leakage and improve subthreshold swing. To enable robust read operation, the cell includes a medium-$V_{th}$ read buffer [11], while asynchronous write operations are considered due to the relative infrequency of write operations. To further reduce standby power, the DMEM uses a leakage reduction scheme based on a free-list. The free-list, managed by the CPU, contains information about whether a particular row in DMEM is used or not. The DMEM has 26 PGS's that are selectively turned off during standby mode based on the contents of the free-list, reducing standby power. Also, decoders, read/write buffers, and other peripherals are power gated during standby time.

Measurements show that the Phoenix Processor consumes 297nW in active mode and 29.6pW in standby mode at $V_{dd}$=0.5V. The extremely low power consumption makes it an attractive candidate for ubiquitous sensing systems.

## III. ULP Watchdog Timer Design

The previous section shows that we can design ULP microprocessors and memories that consume on the order of 10s of pW in standby mode. We must also be able to design sub-modules such as watchdog timers, temperature sensors, and power regulators at comparable power levels to approach a $mm^3$ sensing node.

Watchdog timers play a critical role in such sensing systems that periodically awaken to perform specified tasks. In some cases it can also be essential for tight synchronization among physically adjacent sensing nodes during communication. Therefore, robust and low power timers are a key challenge in this application space.

We now describe a 150pW timer using a program-and-hold technique [4]. This low power consumption is achieved by sampling a bias voltage from a temperature insensitive current source and then shutting off the source after sampling the voltage across a track and hold circuit. This voltage is converted to a frequency by an oscillate stage that draws much less current than the initial bias voltage generating stage. 2-4min periodic programming is necessary to update the bias voltage to track changes in ambient temperature. This charge holding technique reduces the active power by a factor of 200. The temperature insensitive current source is implemented by self-biasing of a resistor.

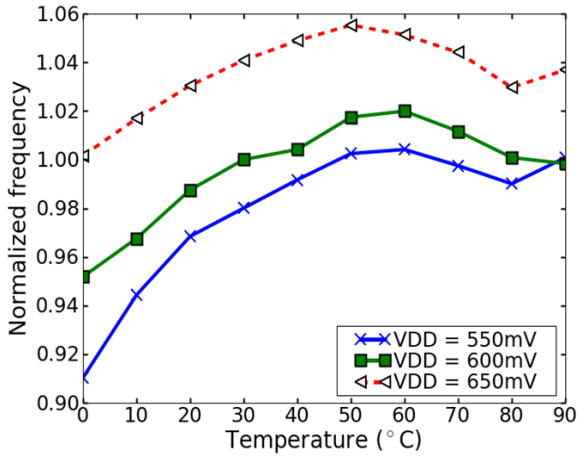


**Figure 3. Frequency of the ULP timer over temperature.**

A test chip was designed in 0.13µm CMOS and the proposed timer was measured to have a nominal period of 0.09s at 600mV. Temperature and voltage sensitivities are shown in Figure 3. When programming the timer every 2 minutes, the frequency deviation at worst-case temperatures is 5%. A frequency deviation of 2% is measured when reducing $V_{dd}$ from 600mV to 550mV. Supply noise is a minor concern for this application domain since very few logic blocks switch during the active mode of the timer (which is the standby mode of the overall system). The total area of the design is 0.019$mm^2$.

## IV. ULP VOLTAGE REFERENCE

The full sensing system often requires several reference voltages that are temperature and supply voltage insensitive. For instance, the ULP timer in Section III needs 3 reference voltages to bias analog circuitry. Additionally, a DC-DC converter such as a linear regulator requires further reference voltages. Therefore, designing an ULP voltage reference is critical to many building blocks for maintaining low power budgets.

Several low power voltage references have been proposed. In particular, [12] proposed a voltage reference that consumes <40nW at Vdd=0.9V. However this still dominates the total power consumption for the sensing systems under discussion, in particular if multiple voltage reference are needed.

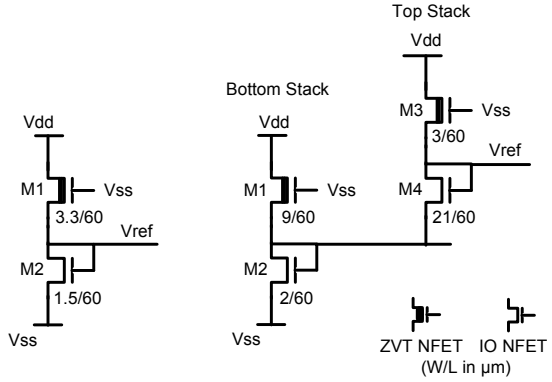


**Figure 4. 2T (left) and 4T (right) voltage references.**

Figure 4 shows a 2T voltage reference that has virtually no power overhead but still provides good temperature and voltage insensitivity [5]. The design consists of only two transistors. The ZVT device (M1) is identical to a normal MOSFET with a near-zero $V_{th}$. It can be replaced with a low $V_{th}$ device for technologies lacking a ZVT device. Figure 4 also shows a 4T voltage reference that cascades two 2T voltage references to generate a higher output voltage.

**Table 1. Measurement results of 2T voltage reference.**

| | 2T | [12] |
|---|---|---|
| Process | 0.13µm CMOS | 0.35µm CMOS |
| $V_{dd,min}$ | 0.5V | 0.9V |
| $V_{out}$ | 175.5mV | 670mV |
| TC | 19.4ppm/°C<br>3.4µV/°C | 10ppm/°C<br>6.7µV/°C |
| LS | 0.033%/V | 0.27%/V |
| PSRR | -70/-67dB<br>(100/100kHz) | -47dB/-38<br>(100/100k) |
| Power | 4.43pA×0.5V | 40nA×0.9V |
| Size | 1350(9785)µm$^2$ | 45000µm$^2$ |

The prototype circuits are fabricated in a 0.13µm CMOS process. The 2T voltage reference, functional down to $V_{dd}$ of 0.5V, achieves 2.2pW power consumption and small footprint with excellent Temperature Coefficient (TC), Line Sensitivity (LS), and Power Supply Rejection Ratio (PSRR). Detailed measurement results are summarized in Table 1. Additionally, the proposed design is compared to another state of the art reference [12], showing several orders of magnitude reduction in power and size with comparable or better temperature and voltage characteristics. Due to its small power and area, many 2T references can be incorporated into ULP sensing system with minimal overhead.

## V. ULP DC-DC CONVERTER

The microprocessors, memories, and timers in the previous sections assume constant supply voltages, which in practice must be supplied by DC-DC converters connected to batteries and/or energy scavenging units. The DC-DC converter must be fully integrated and highly power-efficient due to the small current draw of the sensing system (often sub-µA). Large voltage conversion steps are another challenge. When considering size and integration, Lithium-based thin-film batteries are particularly attractive. However, the relatively high output voltages of their chemistries, typically above 3V [13][14], pose a challenge to efficiently convert down to the target supply voltage of ~0.5V.

To date, little work has focused on this emerging design space. The closest design for comparison requires two input voltages of 1.2V and 1.8V and provides a variable 300mV to 1.1V output with 74% power efficiency (2.6X ideal linear regulator) at 5µW loading [15]. The proposed converter targets one order of magnitude lower power loading, supports 2X higher input voltage, and realizes 56% power efficiency (4.6X ideal linear regulator) in a self-contained system that requires no off-chip components.

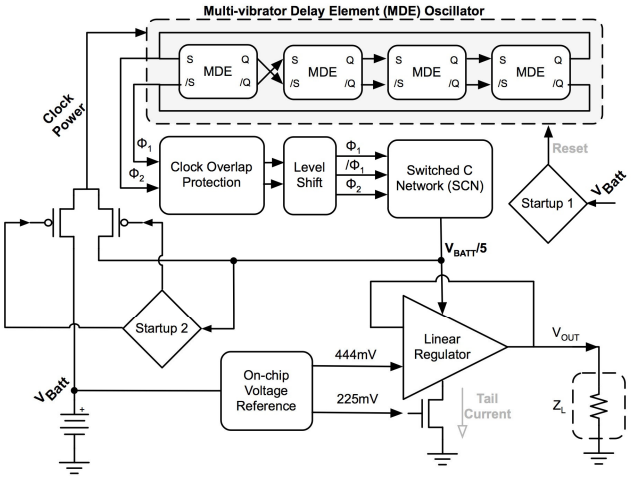


**Figure 5. Sub-µA DC-DC converter schematic.**

The converter uses a hybrid approach consisting of a 5:1 Fibonacci switched capacitor network (SCN) in series with a Low Dropout (LDO) linear regulator, as shown in Figure 5. The clock for the SCN is efficiently generated using a ring of multivibrator delay elements (MDE), which produce full swing outputs at a well-tuned frequency while consuming one order of magnitude lower power than inverter-based configurations. Two variants of the 2T voltage reference in the Section IV are used in the linear regulator.

The DC-DC converter was manufactured in a 0.13µm CMOS process in an area of 0.262 mm$^2$. All test chips were verified to successfully run from a 3.6V lithium coin cell

battery. Efficiency measurements are shown in Figure 6 as a function of load current, and a peak efficiency of 56% was measured with a load of 285nA at 444 mV. Sufficient load and line regulation for subthreshold processing was verified. The peak load regulation is 0.13%/nA at 2.5V and peak line regulation is 0.05%/mV at 3.3V.

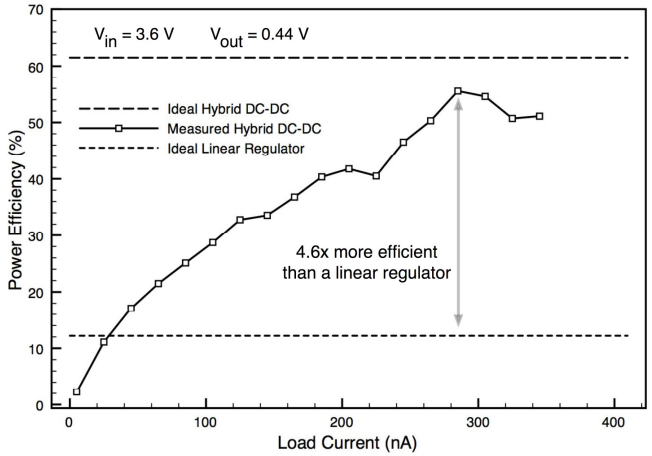


**Figure 6. Power efficiency of the DC-DC converter.**

## VI. FUTURE DIRECTIONS

The circuit techniques and design examples in the previous sections highlight the exciting progress made toward $mm^3$ ubiquitous sensing systems. However, challenges still remain. In this section, we suggest several avenues for future explorations in meeting these challenges.

Low voltage operation often amplifies the impact of temperature and process variations on performance, due to the exponential sensitivities of subthreshold drain currents. Therefore, temperature and process-insensitive designs become an interesting topic of study. They may employ adaptive body bias [16] or adaptive DC-DC converters [17]. Architectural approaches to variability are also vital. These may include a proliferation of traditional schemes such as error correction [18] and redundancy, although the power costs of added hardware need to be weighed carefully against the improvements in robustness achieved.

Options for power sources must be reexamined. Thin film Lithium batteries were considered when designing the DC-DC converter of Section V. However, other options such as solar power, ambient vibration, temperature gradients, or other scavenging techniques [19] can be considered. Also hybrid approaches using both batteries and energy scavenging can be an optimal solution for a specific set of applications.

The DC-DC converter needs to be enhanced by adding standby mode support, since the current draw of the sensing system in standby mode is several orders of magnitude smaller than in active mode. Intelligently slowing down the SCN clock and/or disabling linear regulators would be feasible options.

Perhaps most pressing is the need for ULP wireless communication schemes. The design of ULP communication blocks is highly application-specific. There may be cases where proximity communication schemes [20][21] are suitable and others where more traditional radios are used, but with new architectures to adhere to strict power budgets [22]. Ultra-wideband radio design is also becoming increasingly attractive since low energy consumption can be achieved at low data rates [23].

## REFERENCES


[1] U. Schnakenberg et al, "Initial investigations on systems for measuring intraocular pressure," *Sensors and Actuators* 85, No. 1-3, pp. 287-291, 2000.

[2] Y.-S. Lin et al, "Low-Voltage Circuit Design for Widespread Sensing Applications," *Int. Symp. on Circuits and Systems*, pp. 2558-2561, 2008.

[3] M. Seok et al, "The Phoenix Processor: A 30pW Platform for Sensor Applications," *Symp. on VLSI Circuits*, pp. 188-189, 2008.

[4] Y.-S. Lin et al, "A 150pW Program-and-Hold Timer for Ultra-low-Power Sensor Platforms," *Int. Solid-State Circuits Conf.*, pp. 326-327, 2009

[5] M. Seok et al, "A 0.5V 2.2pW 2-Transistor Voltage Reference," *Custom Integrated Circuits Conf.*, pp.577-580, 2009

[6] M. Wieckowski et al, "A Hybrid DC-DC Converter for Sub-Microwatt Sub-1V Implantable Applications," *Symp. on VLSI Circuits*, pp.166-167, 2009

[7] A. Wang et al, "A 180mV FFT processor using subthreshold circuit techniques," *Int. Solid-State Circuits Conf.*, pp. 292-293, 2004.

[8] N. Verma et al, "A 65nm 8T Sub-Vt SRAM Employing Sense-Amplifier Redundancy," *Int. Solid-State Circuits Conf.*, pp. 328-329, 2007.

[9] S. Hanson et al., "Performance and Variability Optimization Strategies in a Sub-200mV, 3.5pJ/inst, 11nW Subthreshold Processor," *Symp. on VLSI Circuits*, pp. 252-253, 2007.

[10] M. Seok et al, "Analysis and Optimization of Sleep Modes in Subthreshold Circuit Design," *Design Automation Conf.*, pp.694-699, 2007

[11] L. Chang et al., "Stable SRAM cell design for the 32nm node and beyond," *Symp. on VLSI Technology*, 128-129, 2005.

[12] G.D. Vita et al., "A Sub-1-V, 10ppm/oC, Nanopower Voltage Reference Generator," *IEEE Journal of Solid-State Circuits*, pp.1536-1542, 2007

[13] J.B. Bates et al., "Thin Film Rechargeable Lithium Batteries for Implantable Devices," *ASAIO Journal*, vol. 43(5), p. M647, Sept. 1997

[14] B. Bates et al., "Thin-film lithium and lithium-ion batteries," *Solid State Ionics*, Vol. 135, pp. 33, 2000.

[15] Y. Ramadass et al., "Voltage Scalable Switched Capacitor DC-DC Converter for Ultra-Low-Power On-Chip Applciations," *Power Electronics Specialists Conf.*, pp. 2353-2359, 2007

[16] S.V. Kumar et al, "Mathematically-Assisted Adaptive Body Bias (ABB) for Temperature Compensation in Gigascale LSI Systems," *Asia-South Pacific Design Automation Conf.*, pp. 559-564, 2006.

[17] G. D.Vita. et al, "A Voltage Regulator for Subthreshold Logic with Low Sensitivity to Temperature and Process Variations," *Int. Solid-State Circuits Conf.*, pp.530-531, 2007

[18] D. Blaauw, et al, "Razor II: In situ Error Detection and Correction for PVT and SER tolerance," *Int. Solid-State Circuits Conf.*, pp.400-401, 2008

[19] J.A. Paradiso, et al, "Energy scavenging for mobile and wireless electronics," *Pervasive Computing*, pp. 18-27, 2005.

[20] R.J. Drost, et al, "Proximity communication," *IEEE Journal of Solid-State Circuits*, pp. 1529-1535, 2004.

[21] N. Miura, et al, "Analysis and design of inductive coupling and transceiver circuit for inductive inter-chip wireless superconnect," *IEEE Journal of Solid-State Circuits*, pp. 829-837, 2005.

[22] J. Chen, et al, "A Fully Integrated Auto-Calibrated Super-Regenerative Receiver," *Int. Solid-State Circuits Conf.*, 2006.

[23] F. Lee, et al, "A 2.5nJ/b 0.65V 3-to-5GHz Subbanded UWB Receiver in 90nm CMOS," *Int. Solid-State Circuits Conf.*, pp. 116-117, 2007.