

# Driver Modeling and Alignment for Worst-Case Delay Noise

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**Abstract**—In this paper, we present a new approach to model the impact of cross-coupling noise on interconnect delay. We introduce a new linear driver model that accurately models the noise pulse induced on a switching signal net due to cross-coupling capacitance. The proposed model effectively captures the nonlinear behavior of the victim-driver gate during its transition and has an average error below 8% whereas the traditional approach using a Thevenin model incurs an average error of 48%. The proposed linear driver model enables the use of linear superposition which allows the analysis of large interconnects and an efficient determination of the worst-case transition times of the aggressor nets. We proposed a new approach to determine the worst-case alignment of the aggressor net transitions with respect to the victim net transition, emphasizing the need to maximize not merely the delay of the interconnect alone but the combined delay of the interconnect and receiver gate. We show that in the presence of multiple aggressor nets, the worst case delay may occur when their noise peaks are not aligned, although the error incurred from aligning all peaks is small in practice. We then show that the worst-case alignment time of the combined noise pulse from all aggressors with respect to the victim transition is a nonlinear function of the receiver gate output loading, the victim transition time, and the noise pulsewidth and height. To efficiently compute the worst-case alignment time, we propose a new representation of the alignment such that it closely fits a linear function of the input variables. The worst-case alignment time is then computed for a gate using a precharacterization approach, requiring only eight sample points while maintaining a small error. The proposed methods were implemented in an industrial noise analysis tool called ClariNet. Results on industrial designs, including a large PPCmicroprocessor design, are presented to demonstrate the effectiveness of our approach.

**Index Terms**—Cross-coupled noise analysis, delay computation, delay noise, signal integrity, timing verification.

## I. INTRODUCTION AND PREVIOUS WORK

**D**UE to process scaling, cross-coupling capacitance has become a dominant portion of the total parasitic interconnect capacitance. As previously observed [1], [2], the interconnect delay of such nets is strongly dependent on whether their neighboring nets are simultaneously switching or not. The net under consideration is referred to as the *victim* net, and the neighboring nets that capacitively coupled to it are referred to as *aggressor* nets. A victim net with its associated aggressor nets is referred to as a *noise cluster*. If the victim net is stable when the aggressor nets switch, a noise pulse is induced on the victim net that can propagate through the gates in the circuit and potentially change the state of a latch, causing a functional failure. This type of

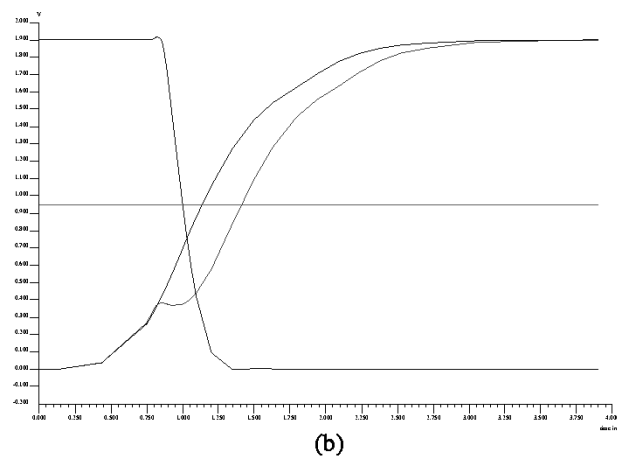
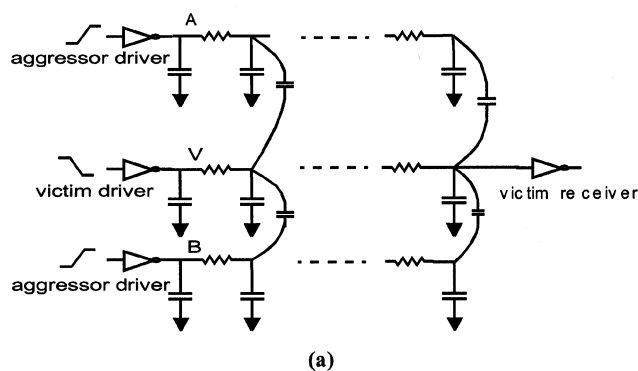


Fig. 1. Coupled interconnect and victim transition wave forms with and without injected noise.

noise is referred to as *functional* noise and has been extensively studied [3]–[6]. If the victim net itself is also switching when the aggressor nets switch, the delay of the victim net can either increase or decrease depending on the aggressor and victim switching directions. This is referred to as *delay noise* and is the focus of this paper.

Fig. 1(a) shows an example of a victim net with two coupled aggressor nets. The victim transition with and without injected noise is shown in Fig. 1(b). In this example, the aggressor nets switch in the opposite direction of the victim net transition, thereby increasing the victim interconnect delay. In order to determine the amount of added delay, we need to solve two problems: 1) Find an efficient approach to simulate the noise cluster composed of the nonlinear drivers with the linear interconnect elements. This is complicated by the fact that the linear interconnect can be quite large, often consisting of tens of thousands of elements. 2) Determine the worst-case alignment between the victim and aggressor transitions such that the impact

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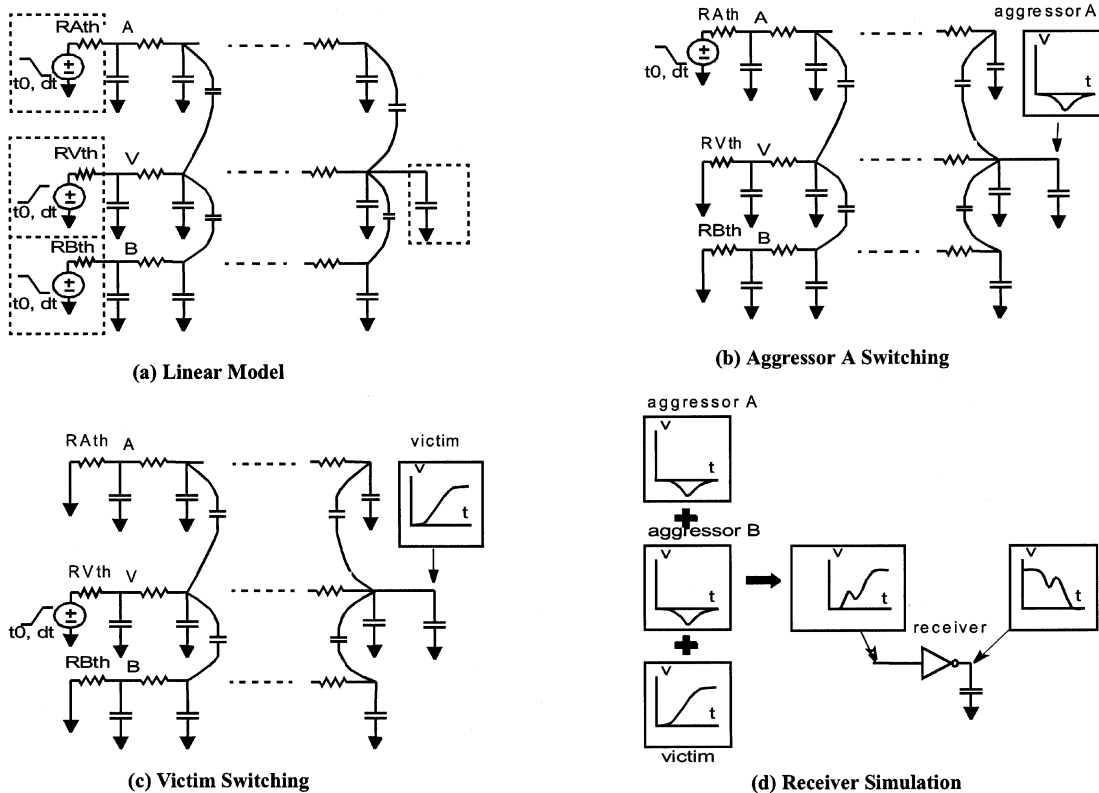


Fig. 2. Interconnect analysis using linear simulation and superposition.

on the victim delay is maximized. In this paper, we investigate both of these issues and proposed efficient solutions for each.

A common approach has been to simply replace the coupling capacitors with *equivalent grounded capacitors*. If the victim and aggressor nets are switching in the opposite directions, the equivalent grounded capacitance is set to twice the coupling capacitance and if the nets are switching in the same direction, the equivalent grounded capacitance is set to zero. However, it has been shown that this approach is not conservative, meaning that it may significantly underestimate the impact of noise on delay [20], [22]. Extensions to this approach have been proposed that increase its accuracy [20], however, the analysis remains approximate and is primarily applicable to the early stages of performance analysis. Recently, a number of models have been proposed to analyze the noise injected from an aggressor net on a victim net using either a closed form solution or simplified circuit analysis techniques [7]–[13], [32]. These methods are useful in early noise analysis and have been applied in noise avoidance approaches [14]–[19]. However, they do not provide the required accuracy needed for performing detailed timing analysis in a high-performance design. Also, they do not consider the nonlinear behavior of the driver and receiver gates in their models.

A straightforward approach for accurate analysis of delay noise is to simulate the nonlinear driver gates and the linear interconnect with a nonlinear simulator, such as SPICE. To increase the efficiency of the analysis, a multiport reduced order model of the interconnect can be used. However, since each victim can have a large number of aggressor drivers, this approach remains slow despite the use of reduced order modeling. Moreover, determining the worst-case alignment between the

aggressor and the victim transitions would require a search with an expensive nonlinear simulation in each iteration. Therefore, such a nonlinear simulation approach is not practical for large processor designs where hundreds of thousands of nets need to be analyzed.

To address the analysis of large designs, linear models of the driver and receiver gates need to be constructed to allow the use of efficient linear simulation and superposition. The driver gate is traditionally modeled with a Thevenin model consisting of a Thevenin resistance  $R_{th}$  and a linear voltage ramp characterized by its start point  $t_0$  and transition time  $d_t$  [23]. The receiver gate loading is modeled with a grounded capacitor. Fig. 2(a) shows the linear model for the circuit in Fig. 1(a). Using superposition, each of the driver gates is simulated in turn, while other Thevenin voltage sources are shorted. Fig. 2(b) shows the simulation model when a transition on aggressor driver A is simulated. A similar model is used to simulate a transition on aggressor driver B. Fig. 2(c) shows the simulation model used to simulate the victim driver transition. The voltage waveforms observed at the receiver input from all simulations are then added together using superposition to obtain the noisy waveform as shown in Fig. 2(d). Using linear driver and receiver models has the advantage that a reduced-order model of the linear network is created once with methods such as PRIMA [21], and is then reused in all different driver simulations. Also, the use of linear superposition allows the noise waveform induced by each aggressor to be shifted to search for the worst-case alignment without requiring re-simulation of the network. The linear model for a victim or aggressor driver is computed using a single nonlinear simulation of the individual driver gate. These linear driver models can be precomputed and stored in precharacter-

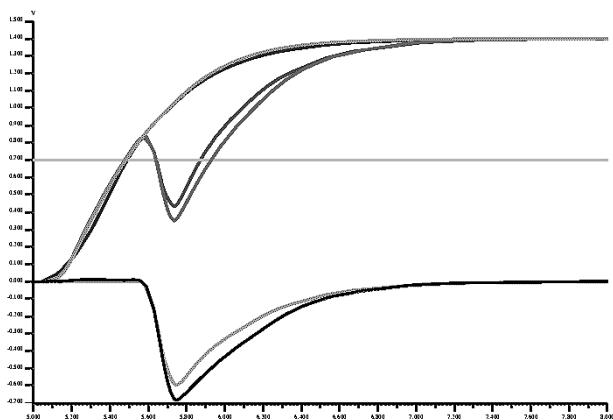


Fig. 3. Simulation results using Thevenin model.

ized tables, after which they are efficiently accessed during the analysis of large designs.

The three parameters that characterize the Thevenin model,  $t_0$ ,  $d_t$ , and  $R_{th}$ , are a function of the effective load of the driver gate which reflects the fact that the driver is actually a nonlinear device. The effective loading of the interconnect is calculated using so-called *C-effective* iterations [23], [24] and captures the resistive shielding of the interconnect. For a particular effective load, the Thevenin model parameters are optimized to obtain a good correspondence with the nonlinear driver simulation at the 10%, 50%, and 90% transition times. In Fig. 3, a victim transition using a nonlinear driver and its corresponding linear Thevenin model are compared when the aggressor nets are not switching [Fig. 2(c)]. The simulation shows that for such a noiseless transition, the linear Thevenin model matches the behavior of the nonlinear driver very well. When an aggressor transition is simulated [Fig. 2(b)], the victim and other aggressor drivers are modeled with their Thevenin voltage source grounded, i.e., their Thevenin resistances are connected to ground. These grounded resistances, or *holding* resistances, represent the ability of these drivers to hold their signal lines steady while the simulated aggressor gate injects noise through the coupling capacitances. However, the Thevenin resistance has been calculated to model the aggregate resistance of the driver over an entire transition of a gate whereas the noise from the simulated aggressor is injected for only a short period of time during the victim is transition. Since the small signal conductance of the driver gate varies dramatically during the transition, an accurate holding resistance is a function of the duration of the injected noise and its alignment relative to the victim transition. It is thus clear that the standard Thevenin resistance is not a good approximation to model the grounded drivers in the superposition flow for coupled interconnects. Fig. 3 shows that the noise pulse computed using the Thevenin resistance for a victim driver significantly underestimates the actual noise injected on the victim net.

One approach proposed for modeling coupled interconnects involves a modified C-effective calculation [26] that accounts for the additional charge that a switching driver gate sees when other gate drivers are switching simultaneously. In this approach, the Thevenin model parameters are updated using a modified effective loading capacitance that accounts for

the additional charge injected due to the switching aggressor nets. However, this approach does not address the deviation of the Thevenin resistance from the actual conductance of the nonlinear victim driver during the short period that the aggressors switch, which is the issue addressed in this paper. Therefore, this modified C-effective calculation can be used in conjunction with our proposed approach.

We propose a new approach which models the victim driver gate with a modified resistance when its voltage source is shorted in the superposition flow [Fig. 2(b)], referred to as the “*transient holding resistance*” –  $R_{tr}$ . The transient holding resistance is a function of the noise width, height, and alignment relative to the victim transition. It is computed using one additional nonlinear simulation of the victim driver and can be precharacterized and stored in a table similar to that for the Thevenin model. Since the transient holding resistance is a function of the noise width and height, we iterate on the computed noise pulse and its associate transient holding resistance until convergence. In practice, only one or two iterations are required. We show that the proposed transient holding resistance significantly increases the accuracy of the delay noise analysis, having an average error of 7% compared with 48% for the standard Thevenin resistance.

The second issue addressed in this paper is how to align the transition of the aggressor nets relative to the transition of the victim net. The aggressor nets must be aligned within the constraints of the switching timing windows that are calculated during timing analysis [1], [27]–[30]. One difficulty is that the timing windows are a function of the added delay due to cross coupling noise, and this added delay is in turn a function of the aggressor timing windows. In [27], [28], it was shown that iteratively calculating the timing windows and the added noise delay will converge. In practice, this requires only a few iterations. Also, the logic constraints in the circuit must be taken into account when considering which aggressor nets can switch simultaneously with the victim net [6], [5], [31].

The task that we examine in this paper is to determine the switching time that produces the worst case victim delay within the constraints of specified timing windows and logic constraints. We approach this problem in two steps: First, we determine the worst alignment of the aggressors nets relative to each other. This will produce a composite noise pulse which is the superposition of all aggressor induced noise pulses. Second, we determine the worst-case alignment of the composite noise pulse with respect to the victim transition time. In the past, the objective has been to maximize interconnect delay, which is measured from the 50% crossing time of the victim driver output to the 50% crossing time of the victim receiver gate *input*. In [26] it was shown that under reasonable assumptions, this delay is maximized by aligning all aggressor noise pulses such that their peaks occur at the same time. The peak of this composite noise pulse is then aligned at the point where the noiseless victim transition reaches  $V_{dd}/2 + V_n$  for a rising transition, where  $V_n$  is the height of the composite noise pulse, as shown in Fig. 4 [25].

In timing analysis, however, the true objective is not to maximize the interconnect delay, but the combined delay of the interconnect and the receiver gate, measured from 50% crossing time of the victim driver output to the 50% crossing time of the

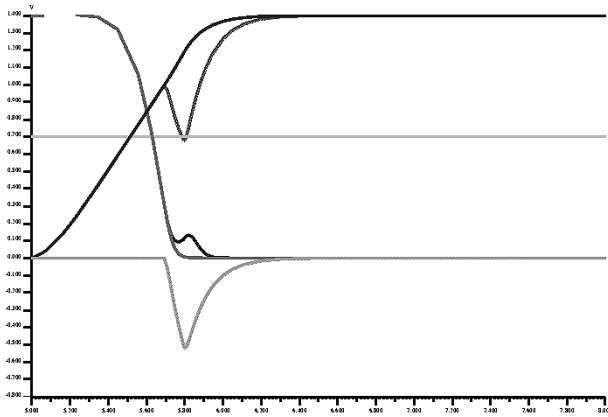


Fig. 4. Spice simulation of worst case alignment at receiver input.

victim receiver gate *output*. In Fig. 4, a SPICE simulation shows that aligning the composite noise pulse for the worst interconnect delay may result in an alignment that does not increase the combined interconnect and receiver delay at all. This occurs when the alignment for maximizing the interconnect delay places the aggressor transition too late and the receiver gate has already completed its transition. In this situation the noise pulse at the receiver input is quite large and a correct alignment of the aggressor would have significantly increased the delay at the receiver output. Note also that in this example, the noise pulse at the receiver output is less than 100 mV and does not constitute a functional noise failure.

It is therefore clear that aligning the aggressor transition based solely on maximizing the interconnect delay, as has been considered to this date, is not valid and that the effect of the alignment on the receiver output transition must be considered. When the receiver delay is included in the aggressor alignment objective, the worst-case aggressor alignment becomes a function of the receiver gate type, size,  $P/N$  ratio, and output load. Furthermore, the receiver gate is highly nonlinear, making efficient closed form solutions difficult. In this paper, we first examine the worst-case alignment of the aggressor transitions with respect to each other. We show that the worst case alignment does not always occur when all aggressor noise pulses have coincident peaks. In these cases, however, the receiver delay is relatively insensitive to the exact alignment of the aggressor peaks, and we show that using aligned noise peaks introduces only a very small amount of error. Second, we examine the worst-case alignment of the composite noise pulse from all aggressor nets with respect to the victim transition. In general, the worst-case alignment is a nonlinear function of the noiseless transition time, the noise pulse height and width, and the receiver gate loading. Finding the worst-case alignment therefore involves a nonlinear optimization, which is expensive since it requires the simulation of the nonlinear receiver gate in each iteration. However, in this paper we represent the noise pulse alignment in such a way that the alignment closely fits a linear function of the input variables. This enables a precharacterization approach where fitted linear functions of the worst-case alignment are precomputed for a particular gate based on a few alignment conditions. We then compute the worst-case alignment for any instantiation of this gate during the analysis by directly evaluating these precomputed

linear function eliminating the need for expensive nonlinear optimization.

Finally, we should note that the linear driver models are a function of aggressor alignment and, conversely, the alignment is a function of the linear driver models. Hence, we iterate in the overall approach between the linear model calculation and the alignment calculation to reach convergence. The overhead in each iteration is relatively small because the linear model calculation involves only one nonlinear simulation of the victim driver circuit and the alignment calculation involves only evaluation of linear functions. In practice we find that only one or two iterations are needed. In this paper, we restrict our discussion to the case when the aggressor nets switch in the opposite direction of the victim net, increasing the interconnect delay. However, the proposed approach is also applicable to the case where the aggressor nets switch in the same direction as the victim net and the interconnect delay is decreased.

This paper is organized as follows. Section II presents the method for calculating the transient holding resistance needed to model the victim driver model when grounded in the superposition flow. Section III presents the methods for calculating aggressor alignment. Section IV presents the results of the proposed approach, and Section V presents our conclusions.

## II. VICTIM DRIVER MODEL

In the proposed superposition flow, the voltage source of the victim driver model is shorted when simulating the noise injected by an aggressor driver as shown in Fig. 2(b). The victim driver is then represented only by the Thevenin resistance  $R_{th}$ . This model introduces a significant error as it does not represent the gate conductance during the time of the noise injection. We propose a more accurate model by replacing the standard Thevenin resistance  $R_{th}$  with a *transient holding resistance*  $R_{tr}$ . We determine this transient holding resistance such that it produces a matching noise waveform with noise injected on the nonlinear victim driver. Our approach is outlined as follows. First, we obtain an estimate of the aggressor noise on the victim net by performing a linear simulation using the standard Thevenin resistance for the victim driver as in the original approach, shown in Fig. 2(b). We then construct a lumped interconnect model using the standard C-effective calculation [23], [24] or the modified C-effective calculation proposed in [26]. Based on this lumped, effective interconnect model and the noise voltage waveform, we calculate the associated noise current that is injected into the victim driver output. We then simulate the nonlinear victim driver with the lumped interconnect model, both with and without this computed noise current. Since the victim driver is switching when the noise current is injected, we cannot directly observe the noise voltage on the victim line but can only construct it from the difference of the driver responses with and without injected noise. Thus, we subtract the two driver output waveforms to obtain the noise waveform at the nonlinear driver output. We then calculate a transient holding resistance that yields a noise pulse with an area matching the area of the noise pulse from the nonlinear simulation. We now compute a more accurate noise voltage waveform at the driver output by repeating the first step with the newly calculated transient holding resistance  $R_{tr}$ . If necessary, we can then iterate on

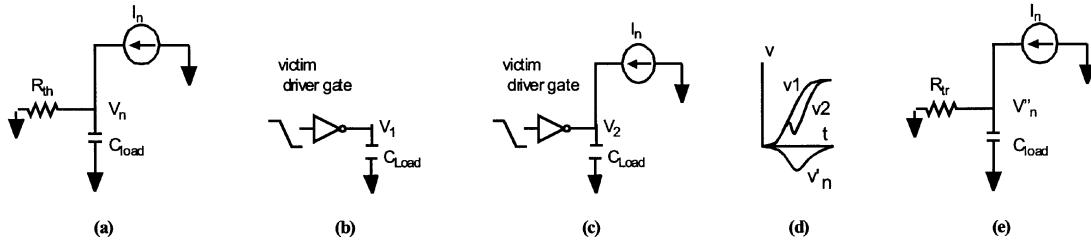


Fig. 5. Transient holding resistance ( $R_{tr}$ ) calculation.

the proposed approach to reach convergence. Each of the steps in the proposed approach is explained in more detail:

- 1) Using Thevenin models for the victim and aggressor drivers, we simulate one aggressor driver at a time while grounding the victim and all other aggressor models [Fig. 2(b)]. In each simulation we record the voltage waveform at the victim driver output and then calculate the total noise voltage  $V_n$  as the sum of all voltage waveforms.
- 2) Using the simplified model shown in Fig. 5(a), we calculate the current waveform  $I_n(t)$  injected into the driver gate as follows:  $I_n = V_n/R_{th} + C_{load} \cdot (\partial V_n)/(\partial t)$ , where  $R_{th}$  is the victim driver Thevenin resistance, and  $C_{load}$  is the effective load capacitance as calculated with C-effective iterations.
- 3) We perform a nonlinear simulation of the victim driver gate with  $C_{load}$  at the output to obtain a noiseless transition  $V_1$  as shown in Fig. 5(b). We repeat this simulation with the added current source  $I_n$  obtained from Step 2 connected at the gate output, and obtain the “noisy” voltage waveform  $V_2$ , as shown in Fig. 5(c).
- 4) We calculate the noise voltage response of the nonlinear driver,  $V'_n$ , by subtracting the two nonlinear simulation results:  $V'_n = V_1 - V_2$ , as shown in Fig. 5(d).
- 5) Finally, we construct the equivalent linear model with transient holding resistance  $R_{tr}$  shown in Fig. 5(e). We determine the value of  $R_{tr}$  such that the area under the resulting noise voltage waveform  $V''_n$  matches the area under  $V'_n$ . The value of  $R_{tr}$  is calculated as follows:

$$I_n = \frac{V''_n}{R_{tr}} + C_{load} \cdot \frac{(\partial V''_n)}{(\partial t)}.$$

Taking the integral of this equation we get the following:

$$\int I_n dt = \frac{1}{R_{tr}} \int V''_n dt + C_{load} \cdot V''_n |_{t=0}^{t=t_{end}}.$$

Since  $V''_n$  is a noise waveform which will return to its original value at  $t_{end}$ ,  $V''_n(0) = V''_n(t_{end})$ , i.e.,  $V''_n |_{t=0}^{t=t_{end}} = 0$ . Also, to match the area of  $V'_n$  and  $V''_n$ , we replace  $\int V''_n dt$  with  $\int V'_n dt$ . Thus:

$$R_{tr} = \frac{\int V'_n dt}{\int I_n dt}$$

where  $\int I_n dt$  and  $\int V'_n dt$  are obtained from Step 2 and Step 4, respectively.

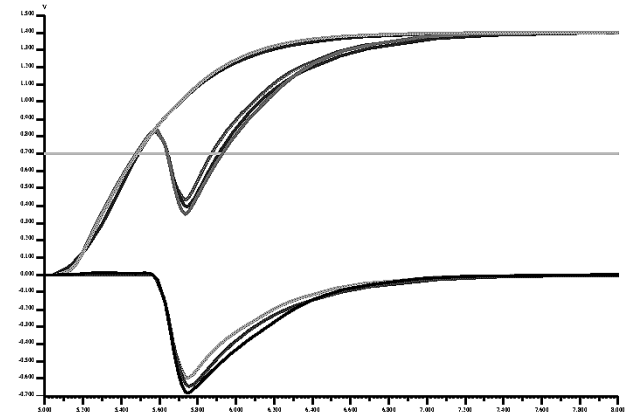


Fig. 6. Linear noise simulation using  $R_{tr}$ .

- 6) We calculate the noise waveform by performing a linear simulation using  $R_{tr}$  in place of the victim driver Thevenin resistance  $R_{th}$  in the circuit shown in Fig. 2(b).

As mentioned, the noise current  $I_n$  has changed after step 6 requiring a recalculation of  $R_{tr}$  and iteration on the proposed steps until  $R_{tr}$  converges. In practice, a single or at most two iterations are necessary. Similarly, when the alignment of the aggressor transition changes with respect to the victim transition, the nonlinear noise waveform  $V'_n$  will be affected, and  $R_{tr}$  must be recalculated. In Fig. 6, we show the simulation results when the proposed approach is applied on the circuit producing the waveforms shown in Fig. 3. The result shows that the voltage waveforms match closely the full nonlinear simulation results. In this case, the calculated transient holding resistance,  $R_{tr}$  is 1463 Ohms, whereas the original Thevenin resistance was 1203 Ohms.

Although up to this point we have focused on the holding resistance of the victim driver, a similar issue arise when we consider the aggressor driver when it has noise inject on it from the victim driver, as shown in Fig. 2(c). In this case, the noise pulse injected on the aggressor net by the victim will be underestimated due to the Thevenin resistance used for the aggressor driver. However, the voltage on the aggressor net is not of direct interest to our analysis and has only an indirect effect on the victim net. Also, in most cases of interest, the victim transition will be relatively slow compared to the aggressor transition, further reducing the impact of this effect. This explains why the noiseless victim transition using a standard Thevenin model shown in Fig. 3 is quite accurate. However, the proposed approach can also be extended to the shorted aggressor driver models to calculate their transient holding resistances if needed.

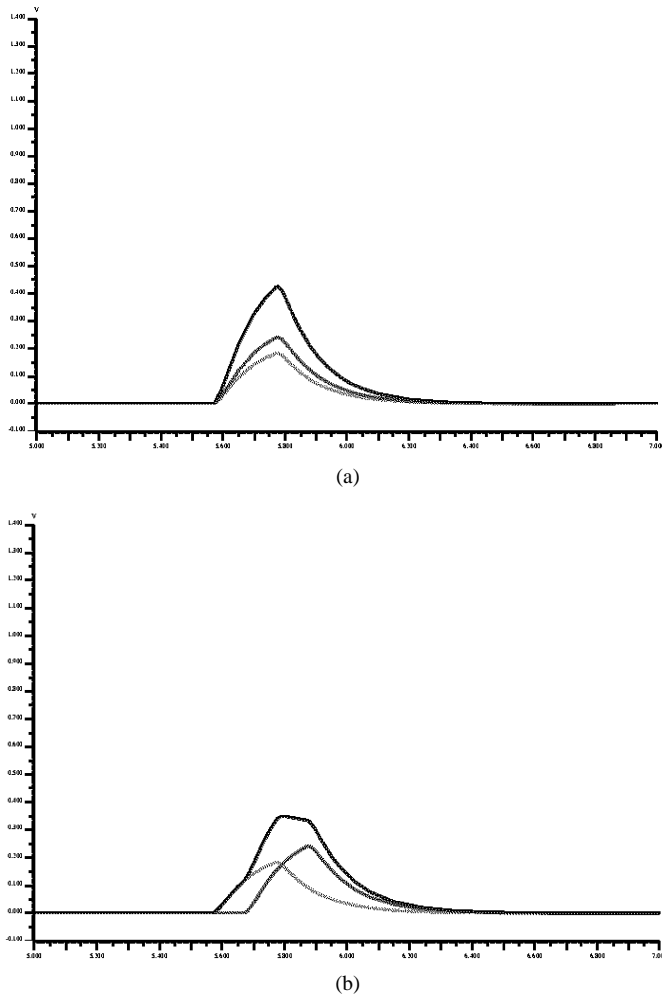


Fig. 7. Composite noise pulse shape with (a) aligned and (b) shifted aggressor noise pulser.

### III. AGGRESSOR ALIGNMENT FOR WORST-CASE DELAY

The interconnect and receiver delay are strongly dependent on how the noise waveforms are aligned with respect to the victim transition. If the noise pulse is aligned too early, the receiver gate has started to transition and its delay will not be affected. On the other hand, if the noise pulse is aligned too later, the receiver gate will already have completed its transition and again its delay will not be affected. Particularly when the receiver gate is lightly loaded and switches fast is the delay of the receiver gate very sensitive to the alignment of the aggressor transitions. We approach the alignment problem in two steps. First, we determine the alignment of the aggressor transitions with respect to each other, forming a composite noise waveform. Then, we align this composite noise waveform with respect to the victim transition. We discuss each of these two issues in more detail later.

#### A. Alignment Among Aggressors

Traditionally, the noise waveforms induced on the victim net are aligned such that their peaks coincide. Such an alignment will produce a composite noise pulse with a maximum pulse height and minimum noise pulsewidth as shown in Fig. 7(a). Conversely, shifting the alignment of the individual noise peaks

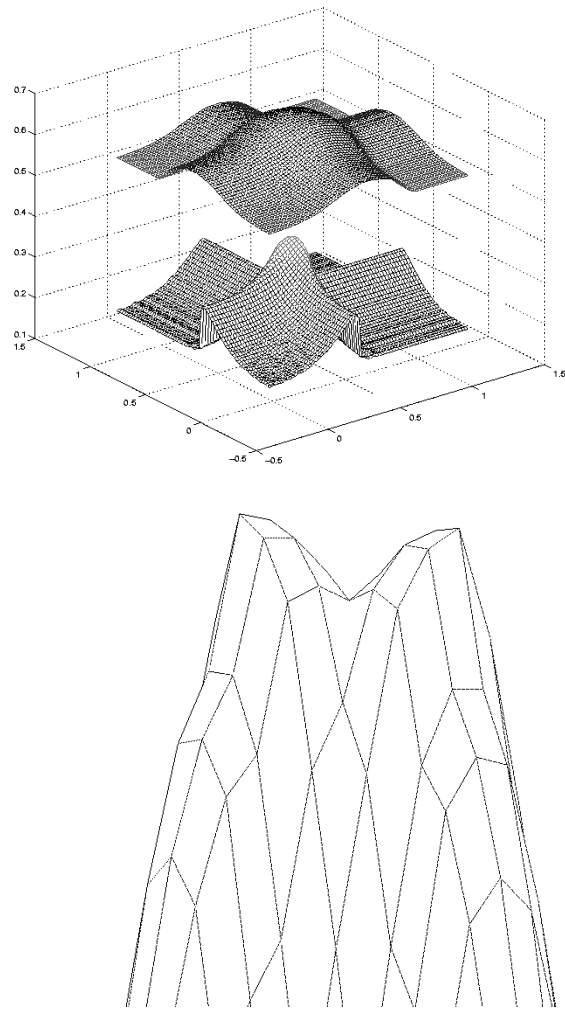


Fig. 8. Impact of the alignment of two aggressor nets on receiver delay.

will result in a wider and less high composite noise pulse as shown in Fig. 7(b). When considering only the interconnect delay, a composite noise waveform with aligned aggressor noise pulses will typically result in the maximum delay. However, as discussed earlier, considering only the interconnect delay is not meaningful, and the receiver delay must be included. Since the receiver gate acts as a low pass filter, a composite noise pulse with maximum height may not always result in the maximum response at the receiver output. Especially when the receiver gate has a large capacitive load, a composite noise pulse with a lower peak voltage and wider width can result in a more delayed response at the output.

Fig. 8 shows the combined interconnect and receiver delay of a circuit with two aggressor nets under varying alignments, simulated using SPICE. The bottom graph shows the result with a lightly loaded receiver driving a fanout of 1. In this case, the receiver gate is able to pass a high frequency noise pulse relatively well and the worst aggressor alignment occurs when the noise peaks of both aggressor nets coincide. The top graph shows the same receiver gate when it is heavily loaded with a fanout of 39. In this case, the receiver gate acts as an effective low pass filter and the worst aggressor alignment occurs when the noise peaks are not aligned and a wider and less high composite noise pulse

is presented to the receiver gate. This is evident from the two off-center spikes in the enlargement of the delay peak shown in Fig. 8.

Having to consider nonaligned aggressor peaks greatly expands the search space for the worst-case aggressor alignment and makes the problem significantly more complex. Fortunately, the cases where the worst-case delay occurs with nonaligned aggressor noise peaks also represent those cases where the delay is relatively insensitive to the noise alignment. The worst-case delay is produced by nonaligned aggressor noise peaks are when the victim transition is fast relative to the aggressor transition, or the receiver output load is large. In both these cases, the extra delay is relatively small and insensitive to the alignment. Therefore, we can align all aggressor peaks together without incurring a large error in the delay calculation. In Fig. 8, for example, the delay difference at the receiver output is only 2.7 ps between the worst-case alignment and the alignment with coincident peaks. In all our simulations, the error introduced by this approximation is less than 5%.

### B. Alignment With Respect to the Victim Transition

After the composite noise pulse is constructed, its alignment relative to the victim transition is determined. Calculating the worst-case alignment is complicated by the fact that the added delay is a nonlinear function of the alignment time. Also, the worst-case alignment time is a nonlinear function of the receiver gate size and output load, as well as the composite noise waveform height and width and the noiseless transition time at the receiver input. Finding the precise worst-case alignment requires a nonlinear optimization (such as the simplex method), and involves a large number of nonlinear simulations of the receiver gate. This is clearly too expensive to perform during timing analysis.

We therefore propose a pre-characterization approach where the worst-case noise alignment is calculated using precharacterized parameters. Since the number of variables that influence the worst-case alignment is large, the number of data points needed to build a simple linearly interpolated lookup table or a fitted spline would be unacceptably high. For instance, if for a particular gate the four dimensions (output load, noise pulsewidth/height, and victim edge rate) were sampled at 10 points each, a total of 10 000 sample points would be required. Each sample point requires a nonlinear optimization, which would be prohibitively expensive. Although the worst-case alignment time is a nonlinear function of the four variable, we found that it matches a linear function in each dimension with every little error if represented correctly as discussed later. Using this approach, we can represent the alignment using a fitted linear function of the input variables, requiring only eight precharacterization points, while maintaining an accuracy within 10% of the worst-case added delay. The dependence of the worst-case alignment on the four variables is discussed in more detail later.

*Receiver Output Load Capacitance:* To understand the behavior of delay noise with respect to the receiver gate output load, Fig. 9(a) shows the total delay (the combined interconnect and receiver delay) as a function of the composite noise pulse alignment for different receiver output load capacitance values. The simulation shows that for small receiver loads, the

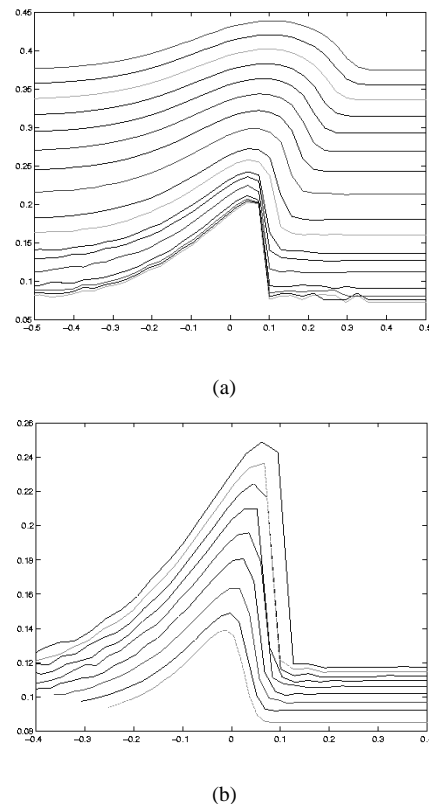


Fig. 9. Delay as a function of noise alignment.

alignment is very sensitive and even a small shift in alignment can produce a dramatic change in the delay. However, for large output loads, the delay is relatively insensitive to the alignment and a deviation in the worst-case alignment results in only a small error in the added delay. In our approach, we therefore use the worst-case alignment at minimum receiver output load for all loading conditions for the receiver gate. From Fig. 9(a), it is clear that this will introduce only a small error for the case where the receiver gate has a large capacitive load. In our model, the alignment is therefore independent of the receiver load.

*Victim Edge Rate:* The worst-case alignment exhibits a nonlinear relationship as a function of the edge rate, if the alignment is measured from the start of the victim driver input transition. However, when we measure the alignment with respect to the 50% crossing time of the victim transition, the relationship closely approximates a linear function. To illustrate this, Fig. 9(b) shows the total delay as a function of the composite noise pulse alignment for different victim transition times with the alignment measured relative to the 50%  $V_{dd}$  crossing time of the victim transition. Since the worst case alignment is nearly linear with respect to the victim transition time, we need to precharacterize a gate for only minimum and maximum victim transition time and can linearly interpolate for points in between. The alignment with respect to the victim transition time is expressed using the following simple model:  $t_n = t_{50} + a_1 + a_2 t_r$ , where  $t_n$  is the alignment time,  $t_{50}$  is the 50% crossing time of the noiseless victim transition,  $t_r$  is the transition time of the noiseless victim transition and  $a_0$  and  $a_1$  are fitted parameters. Note that  $t_{50}$  is nonlinear function of the transition time of the victim since it includes the driver delay. Therefore, to evaluate the alignment time  $t_n$  we first simulate the noiseless transition

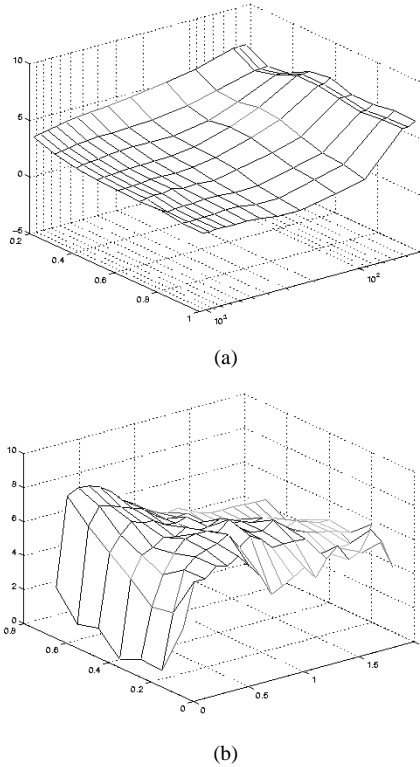


Fig. 10. Error plot for predicted worst-case alignment.

of the victim driver and then find the crossing time  $t_{50}$  through a method such as Newton-Raphson which can be performed very efficiently.

To determine the worst-case alignment for different victim slopes and receiver output loads, we require only two pre-characterization points, one at maximum victim transition time and one at minimum victim transition time. Both pre-characterizations are performed with minimum receiver output load. Fig. 10(a) shows the accuracy of this approach for all possible victim slopes and receiver loads for a typical gate. The added delay obtained using the predicted worst-case alignment is compared with the added delay using a worst-case alignment obtained through a nonlinear optimization. The receiver output load and the victim transition time are both varied over a large range. In all cases, the error in the added delay is less than 7%.

**Noise Height and Width:** The noise alignment time is a nonlinear function of the noise pulse height and width, complicating an efficient calculation of the worst-case alignment time. Therefore, we express the alignment in terms of the so-called alignment voltage instead of the alignment time. The alignment voltage is the voltage at the input of the receiver at the time point when the noise pulse reaches its peak (voltage  $V_a$  in Fig. 3). When considering the alignment in terms of its alignment voltage, we find that it exhibits a close to linear dependence on the noise pulsewidth and height. Fig. 11(a) and (b) shows the total delay as a function of the alignment voltage for varying noise pulse widths and heights, respectively. We model the alignment voltage with a linear function, fitted at four sample points at corresponding to the conditions of minimum and maximum pulsewidth and pulse height. We use the following model:  $v_a = b_0 + b_1 h_n + b_3 w_n + b_4 h_n w_n$ , where

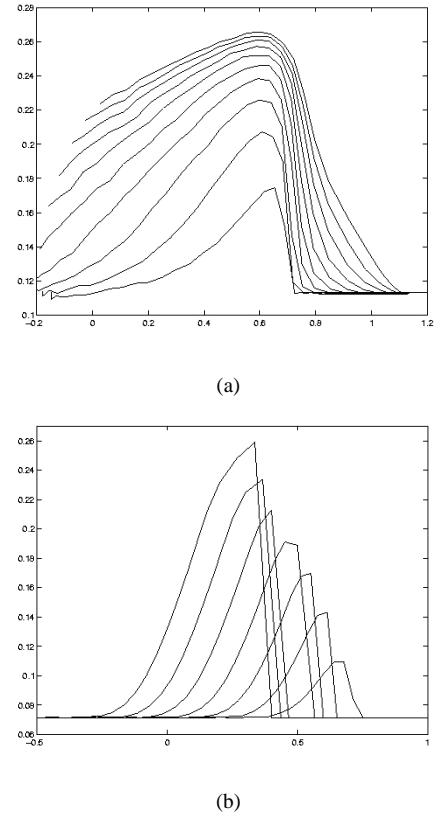


Fig. 11. Delay as a function of alignment voltage.

$v_a$  is the alignment voltage,  $h_n$  and  $w_n$  are the pulse height and width, and  $b_0$ ,  $b_1$ ,  $b_2$ , and  $b_3$  are fitted parameters.

Note that we can always calculate the alignment time from the alignment voltage and the noiseless victim transition waveform. The alignment time is a nonlinear function of the alignment voltage and finding the alignment time  $t_a$  translates into the problem of finding the time point at which the noiseless victim transition reaches voltage level  $v_n$ , where  $v_n$  is the sum of the alignment voltage  $v_a$  and the noise pulse height  $h_n$ ,  $v_n = v_a + h_n$ . We can again solve this nonlinear problem efficiently, using Newton-Raphson iterations, since the noiseless victim transition is a monotone increasing function and no nonlinear simulations are required in the search iterations. Fig. 10(b) shows the error in the calculated delay using the proposed approach for worst-case alignment calculation for a range of possible noise pulsewidths and heights. The added delay obtained with the worst-case alignment using the fitted linear function and the added delay obtained with a worst-case alignment using a nonlinear optimization are compared. The error in the added delay is less than 8% over a large range of noise pulsewidths and pulse height combinations.

Since for the noise pulsewidth and height we express the alignment in terms of voltage, while for the output load and victim transition time we express the alignment in terms of time, we resolve the worst-case alignment calculation in two steps. First, we compute the alignment voltage as a function of the pulsewidth and height at the minimum and maximum victim transition time. We then translate these two alignment voltages into alignment times, and compute the worst-case alignment time by linearly interpolating between them using



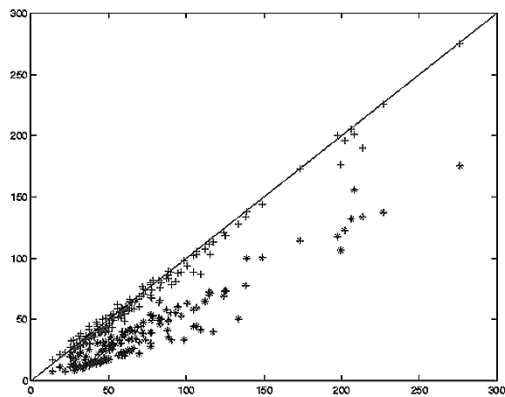


Fig. 12. Linear model results versus nonlinear simulation.

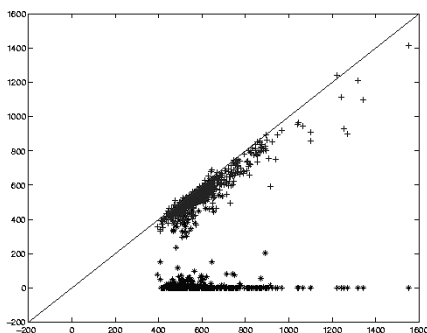


Fig. 13. Extra delay computed using exact and predicted worst-case alignment.

the victim transition time. The overall precharacterization process uses eight receiver gate conditions – 2 points in each of the pulsewidth, pulse height, and victim slope dimensions, all with the minimum receiver output load. Using 4 sample points at both minimum and maximum victim transition times we fit the parameters of the two linear functions expressing  $v_a$  as a function of  $h_n$  and  $w_n$ .

#### IV. RESULTS

The proposed algorithms were implemented in an industrial noise analysis tool called ClariNet, which has been used on a number of chip designs [6]. The proposed method was tested on a random logic block from a 500-MHz processor in 0.18  $\mu\text{m}$  technology. The circuit block was synthesized and placed and routed using commercial tools and the interconnect parasitics were extracted using a 2.5d extraction tool. We report the analysis results on the 300 nets with the highest noise as shown in Figs. 12 and 13. Fig. 12 shows the accuracy obtained with the proposed transient holding resistance calculation. The calculated delay using linear simulation with either the original Thevenin resistance or our proposed transient hold resistance are plotted on the  $Y$  axis, and are compared with the delay obtained using Spice simulation of the full nonlinear circuit, plotted on the  $X$  axis. A perfect match would correspond to points falling on the 45 degree line. The results show that the transient holding resistance has a significantly higher accuracy, with an average error of 7.41% compared to the Thevenin resistance, with an average error of 48.63%. The maximum error for the transient holding resistance model was 23 ps compared with 101 ps for the Thevenin model. Moreover, the Thevenin resis-

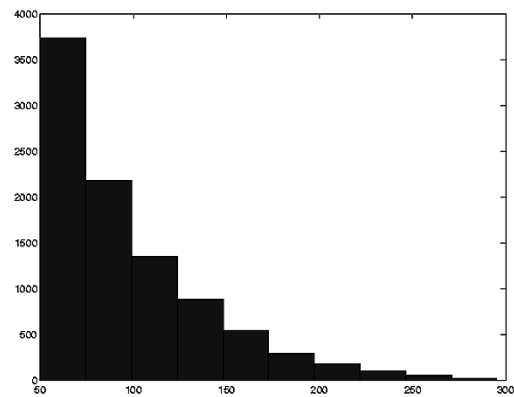


Fig. 14. Added delay distribution for a large PPC processor core.

tance incurs a higher error for nets with a larger delay and in all cases underestimates the delay, which is undesirable for noise analysis.

In Fig. 13, the extra delay using the predicted alignment with our proposed approach is plotted on the  $Y$  axis and is compared with the delay using an exhaustive search of the worst-case alignment, plotted on the  $X$  axis. We also show the delay obtained when using the alignment that maximizes the delay at the receiver input using the method presented in [25]. Comparing this approach with our proposed approach which maximizes the delay at the receiver gate output, shows that our proposed method has a significantly higher accuracy. It is clear from the many nets that have zero extra delay under the traditional alignment approach that alignment based on maximizing the delay at the receiver input places the noise pulse too late, such that the receiver output has already completed its transition and its delay is not affected by the noise. The average error for the traditional alignment approach is therefore 82%. On the other hand, the proposed approach shows good accuracy with an error of 9% on average over all nets.

Finally, we used our analysis approach on a 500 MHz PPC industrial processor core consisting of 200 000 top-level nets. The analysis time for all top level nets was 3 h on a Sparc Ultra-60 computer. For the 9364 nets with significant coupling noise, the distribution of the added delay is shown in Fig. 14. The results show that the 95% of all nets have an added delay of 50 ps or less. However, for 72 nets, the added delay is quite significant, exceeding 250 ps. These nets strongly impact the performance of the circuit, therefore underscoring the importance of delay noise analysis.

#### V. CONCLUSION

In this paper, we presented a new approach to accurately calculate the extra delay due to cross-coupled noise injection. We proposed a new linear model that accurately captures the nonlinear behavior of the victim driver gate when noise is injected from aggressor nets. Results show that this model significantly reduces the error in the calculated noise. The model is obtained through a simple simulation of the driver gate and can be precharacterized for gates prior to noise analysis. For determining the alignment of the aggressor noise pulses relative to the victim transition, we have demonstrated the need to include the victim receiver gate delay in the alignment objective

function. We have shown that while in some cases nonaligned aggressor noise peaks will result in the worst-case delay noise, aligned aggressor noise peaks can be used with a small error. To determine the alignment of the composite noise pulse relative to the victim transition, we proposed an alignment representation that allows us to compute the worst-case alignment with linear precharacterized functions in an accurate and efficient manner. Finally, results were shown on industrial circuits demonstrating that the proposed methods significantly increase the accuracy of the analysis.

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