Analyzing the Impact of Double Patterning Lithography on SRAM Variability in 45nm CMOS

Vivek Joshi, Michael Wieckowski, Gregory K. Chen, David Blaauw, Dennis Sylvester

University of Michigan, Ann Arbor, MI. email: {vivekj, wieckows, grgkchen, blaauw, dennis}@eecs.umich.edu

***Abstract* — This paper analyzes the impact of Double Patterning Lithography (DPL) on 6T SRAM variability. A test chip is implemented in a 45nm CMOS process that uses DPL. Measurements from 75 dies demonstrate a significant impact of DPL on SRAM failures. Extensive analysis demonstrates that DPL induced mismatch considerably increases functional failures in SRAM cells, and degrades yield. We also propose a DPL-aware sizing technique to mitigate yield losses.**

I. INTRODUCTION

Double patterning lithography (DPL) is widely considered the only optical lithography solution for the 32nm and several subsequent technology nodes [1], due to significant technical hurdles delaying the implementation of new lithography techniques such extreme ultraviolet (EUV) [2], immersion ArF (IArF) lithography [3], and e-beam lithography [4]. Pitch-split DPL decomposes and prints critical layout shapes in two exposures, and systematic offsets between the two masks leads to mismatch between adjacent devices [5]. Such variations in channel length negatively impact SRAM robustness by increasing functional failures. Figure 1 shows the layout and schematic of a typical six transistor (6T) SRAM cell, along with the stick diagram (polysilicon layer only) depicting how rows of SRAM cells are laid out. The access transistor PG1 is on a different polysilicon track than the pull-up/pull-down transistors (PU1/PD1), and in DPL they are printed on separate exposures, thereby leading to mismatch that impacts SRAM robustness. For example, if PG1 becomes stronger in comparison with PD1, the read stability of the SRAM cell is negatively impacted. Also, as shown in the figure, adjacent rows of SRAM cells are mirror images of each other, and hence if transistors on track A are stronger (smaller channel length) in Row 1, transistors on track B will be stronger in Row 2. Hence, for a given operation (read 1, write 1, etc.), alternate SRAM rows will show similar behavior, and adjacent rows will show opposite behavior.

Past work [6, 7] has analyzed the impact of lithographic variation on electric yield of SRAM, for single patterning lithography and cut-mask double patterning [8]. However, to the best of our knowledge, this is the first work to analyze the impact of pitch splitting double patterning (adjacent polysilicon tracks are printed in separate exposures [5]) on SRAM variability and robustness through silicon measurement. To observe the impact of DPL in hardware in 45nm CMOS, we examine the difference in write failures between even and odd rows at lowered supply voltage to accelerate failures. Student's t-tests [9] are performed on the data to ensure that the observed difference in behavior between even and odd rows is due to double patterning and not random threshold voltage (V_{th}) variation. Extensive simulations are also conducted to quantify the impact of double patterning on SRAM robustness and establish that DPL substantially degrades the electrical yield of SRAM. It is concluded that there is a need for DPL variation aware SRAM variability analysis and optimization. Finally, we propose a DPL-aware SRAM sizing method to mitigate yield loss. Section II presents simulation based analysis

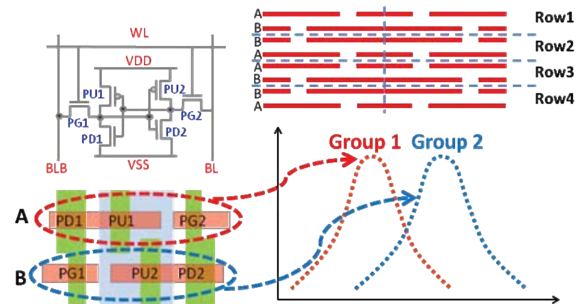

Figure 1: SRAM cell/row layout and DPL based variation.

of SRAM robustness, Section III presents the measurement results from the test chip, and DPL-aware sizing scheme is discussed in Section IV.

II. SIMULATION BASED ANALYSIS OF SRAM ROBUSTNESS UNDER DPL

Mismatch between the access transistor and pull-up/pull-down transistors leads to increased SRAM variability. This mismatch depends on the mean (μ) and standard deviation (σ) of the line-width distribution for the two separate masks used to print the polysilicon gates for these transistors (shown as Group 1 and Group 2 in Figure 1). Previous work has reported $3\sigma/\mu$ numbers as high as 16.5% for these line-width distributions [5]. A convenient method to analyze SRAM robustness is through corner-based failure analysis, where the failure is characterized in terms of the smallest multiple of sigma V_{th} at which the cell experiences functional failure, and this value is called read/write margin.[1] For our analysis, we assume that the two line-width populations due to the two DPL masks have the same mean (μ) and $3\sigma/\mu$ of 10%. This is an optimistic scenario as any difference in the means will further increase the mismatch, resulting in greater degradation in robustness due to DPL. Read margin is calculated for each length sample, and Figure 2 shows the distribution of the read margins under DPL and single exposure lithography (higher read margin means lower probability of failure, and higher robustness). Also plotted is a zoomed in view of the distribution tails, showing the μ-3σ points for single patterning ($P_{\mu\text{-}3\sigma,SP}$) and DPL ($P_{\mu\text{-}3\sigma,DP}$) read margin distributions. Mean of the read margin curve for DPL is $4.20\sigma_{VT0}$, with a standard deviation of 0.2 σ_{VT0}, while for single exposure lithography mean is $4.23\sigma_{VT0}$, and standard deviation is $0.1\sigma_{VT0}$. σ_{VT0} is the sigma V_{th} defined for the 45nm industrial technology used in this work. As expected, DPL increases the variability with the standard deviation increasing by 2×. For the μ-3σ point in the distribution, the probability of failure increases by ~3.3× due to DPL compared to single exposure lithography. Figure 3 shows how the mean (μ), standard deviation (σ), and μ-3σ points of the read margin distribution vary (normalized to σ_{VT0}), as the difference between the mean of the two line-width

[1] where each device is skewed in its worst direction to induce a particular failure mode, e.g., strong access devices lead to read failures.

978-1-4244-5760-1/10/$26.00 ©2010 IEEE

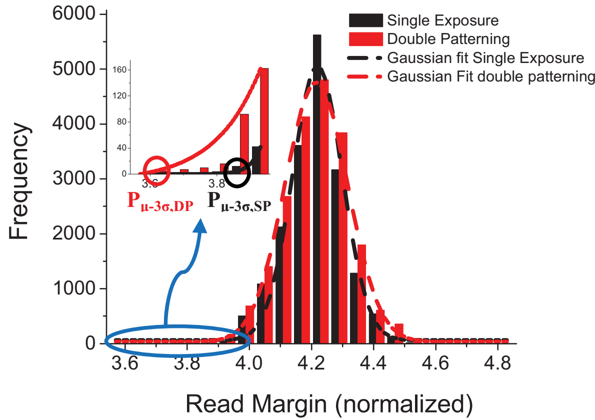

Figure 2: Read margin distributions and Gaussian fits for DPL and single exposure lithography.

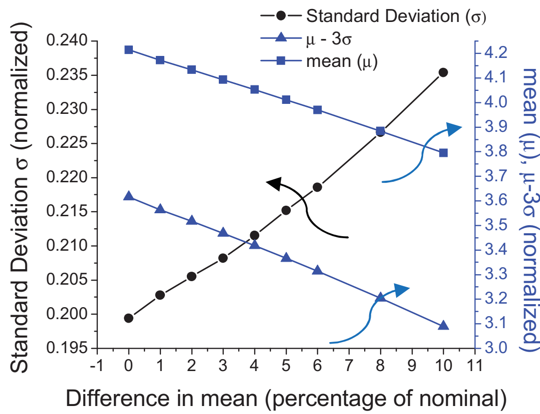

Figure 3: Read margin σ, μ, and μ-3σ as a function of difference in means of the line-width distribution curves for DPL.

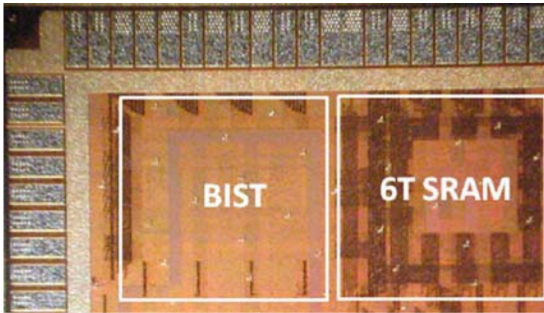

Figure 4: Die-shot of the 45nm test chip showing the SRAM array and built-in self-test (BIST) structure.

distribution curves is increased from 0, while maintaining the $3\sigma/\mu$ value at 10%. Introducing a difference in mean further increases the mismatch and results in an increase in variance and decrease in the μ-3σ point, thereby increasing the probability of failure and degrading the SRAM robustness. Similar results are observed for write failure, although the write operation itself is more robust with a mean write margin of 6.36 σ_{VT0}.

III. TEST CHIP MEASUREMENT RESULTS

We implemented a 45nm test chip with 32kb 6T SRAM arrays to observe the effect of double patterning on SRAM failure counts. Figure 4 shows the die shot of the chip with SRAM arrays and built-in self-test (BIST) structures. We measured 75 such chips to obtain data on read and write failures. In order to obtain statistically significant failure data from a 32kb memory, we lower the operating voltage to induce failures. For a given sample of transistor lengths, the mismatch has a different impact on read and write errors, and hence it is necessary to differentiate between them. Read errors are examined by writing to the memory at nominal V_{DD} (1.1V) and then reading out at a lower voltage. Similarly, capturing write errors involves writing the cells at a reduced voltage, followed by a read at full V_{DD}.

It is necessary to observe how the failures scale with voltage to determine the appropriate operating voltage for measurement. Figures 5 shows the increase in read and write errors as supply voltage is reduced in three test chips. The peripheral circuits are designed such that they are not failure critical at lower values of voltage, and the failures occur only in the SRAM cells. In the case of a read operation, the number of failures increases abruptly at voltages close to 0.36V, whereas in the case of write operation the number of errors becomes sufficient for statistical analysis at approximately 0.45V. Eventually, as the operating voltage approaches the threshold voltage, nearly all cells fail. The difference in behavior between read and write operations matches results from SPICE simulation of a nominally sized SRAM cell. Write operation is more stable at nominal V_{DD} (write margin is higher than read margin), however as V_{DD} is lowered it becomes less robust than read operation. Thus, more write failures will occur at lower V_{DD}, which means that significant write failures are observed before reaching the threshold voltage where nearly the full array abruptly fails. Based on these observations, we focus on write 0 and write 1 operations, and the V_{DD} used for measurement is 0.45V.

As shown in Figure 1, adjacent rows of SRAM cells are mirror images of each other. Hence, if gates on polysilicon track A (shown in Figure 1) are stronger (smaller channel length) than those on track B in one row of SRAM cells, gates on track B will be stronger in the adjacent rows. If in fact DPL has a major impact on SRAM stability, even rows should behave differently than odd rows for a given operation (write 1 or write 0). This difference should result in significantly different error counts for the two rows.

Figure 6 shows the error count distribution for write 1 operations across the 75 test chips, for even and odd rows, along with the Gaussian fit for the two distributions (total number of failures

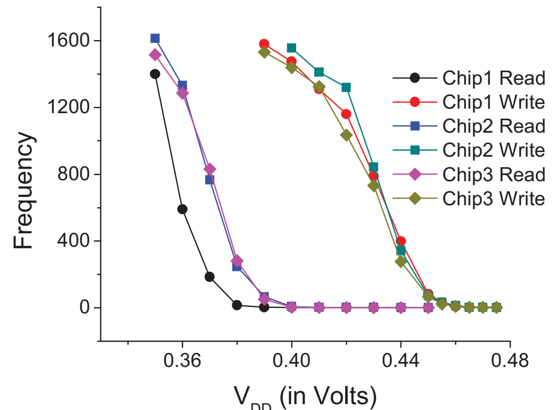

Figure 5: Number or read and write failures as a function of V_{DD}.

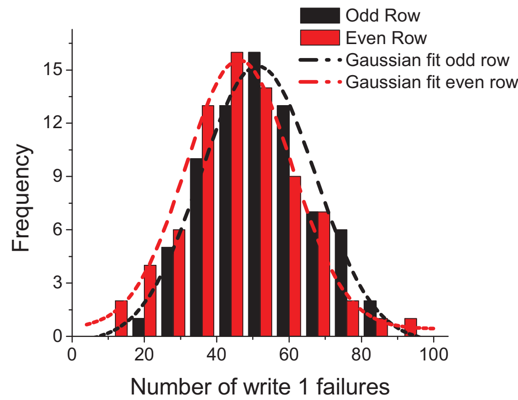

Figure 6: Write 1 failure count distribution for even and odd rows.

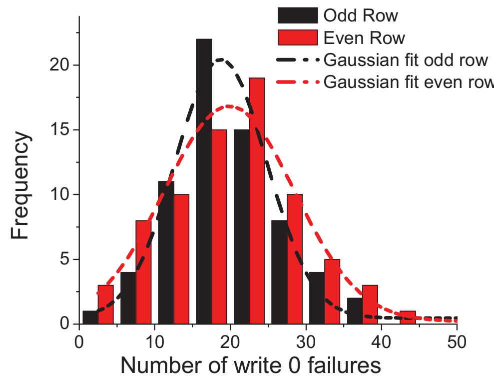

Figure 7: Write 0 failure count distribution for even and odd rows.

analyzed is ~7700). The distributions for even and odd rows are distinct, and the difference in mean for the two distributions is ~14.5%. Figure 7 shows the corresponding distributions for write 0 operation, and the difference in mean between even and odd rows is ~25% in this case (total number of failures analyzed is ~3400). To show through simulation that most of this difference in mean failure counts is caused by double patterning and not random V_{th} variation, we plot the number of write 0 errors as well as the percentage difference between the mean number of errors of even and odd rows as a function of V_{th} standard deviation for 75 length samples (to model 75 dies measured) under the assumption of single exposure lithography. Under a single exposure lithography assumption both even and odd rows use the same length sample, but include random V_{th} variation, and the V_{th} standard deviation is increased in steps. Figure 8 shows this plot; all the V_{th} standard deviation values are normalized to σ_{VT0} specified for the 45nm library. As V_{th} standard deviation increases, the number of errors and the difference in the number between even and odd rows both go up. As a result, the percentage difference in error remains almost constant at around~4.5%, which is significantly lower than the observed difference in the silicon measurements. Hence, random V_{th} variation is unlikely to have caused the high difference in mean observed between even and odd rows for the test chip measurements.

Next, we performed Student's t-test [6] on the two sets of data for write 0 and write 1 operations, to more conclusively reject the possibility that the observed difference in means is due to random

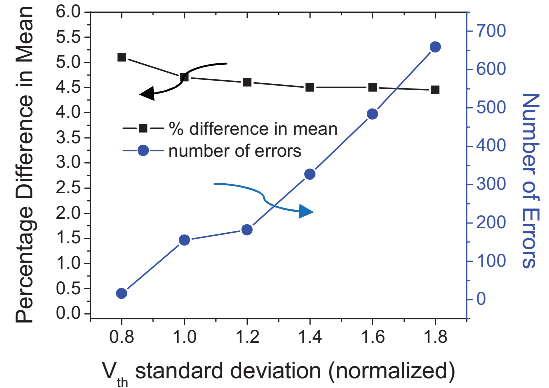

Figure 8: Difference in mean and number of errors for write 0 operation as a function of V_{th} standard deviation.

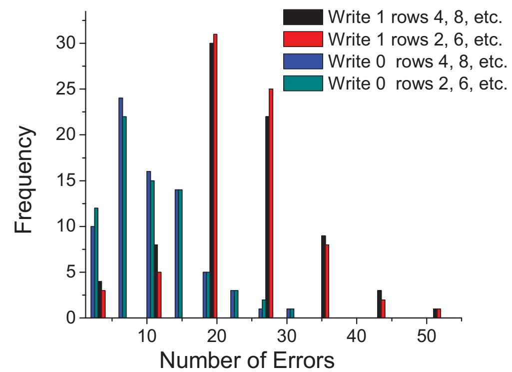

Figure 9: Write 0 and write 1 failures for two subsets of even rows.

variation rather than DPL. Student's t-test is a small-sample statistical hypothesis test, in which two sets of data are tested to determine if their mean difference is due to chance/ random variation, or if there is indeed a difference in the two sets of data. The data is said to follow the null hypothesis if there is no effective difference between the observed sample means for the two sets, and any measured difference is due only to chance/random variation. For write 1 operation, the probability of the result assuming the null hypothesis was found to be 0.025, and the corresponding probability for the write 0 operation was found to be 0.0033. Both these values suggest the improbability of the null hypothesis (probability < 0.05) and point to the conclusion that the differences in measured error count are due to double patterning lithography.

Another way to validate the t-test results is to compare the failure counts between subsets of even/odd rows. Since there is no added variability due to DPL, two subsets of even rows should show similar error counts for the 75 test chips within the bounds of random variation. We break the even rows into two subsets: subset 1 comprising of rows 2, 6, 10, etc., and subset 2 comprising of rows 4, 8 , 12, etc. Figure 9 shows the error count distribution for the two subsets, for write 1 and write 0 operations. As expected, the distributions are very similar for the two subsets, with the difference in mean failure count being ~3% for write 1, and ~1% for write 0 operation. On performing Student's t-test upon the two subsets, we obtain the probability of the result

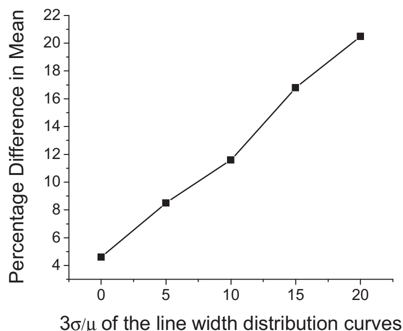

Figure 10: Write 1 difference in number of failures for even and odd rows as a function of 3σ/μ of line width distribution curves for DPL.

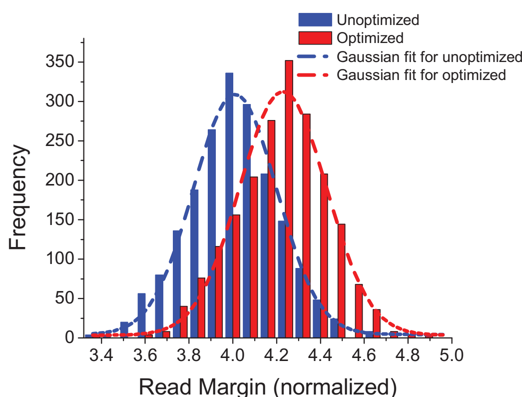

Figure 11: Read margin distributions and Gaussian fits for DPL-aware sizing optimized and unoptimized case.

assuming null hypothesis to be 0.91 for write 0 operation, and 0.62 for write 1 operation. Thus, t-tests can successfully determine that the two sets of data are subsets of same kind of row (even in this case). This experiment further validates the t-test results suggesting difference in behavior between even and odd rows is due to DPL.

In order to estimate the DPL line width distribution curves for the two separate exposure steps, we use simulation to find 3σ/μ value for the two curves that can generate such a difference between failure counts for even and odd rows. To simplify the problem, we assume that the two curves have same mean and standard deviation, and sweep the 3σ/μ values to generate difference in error counts between even and odd rows as a function of 3σ/μ for the line-width distribution. Figure 10 shows the resulting plot for write 1 operation. The plot gives a rough estimate of 3σ/μ for the two curves to be ~12.8%. Based on simulation results in Section II, such a difference can lead to appreciable degradation in SRAM robustness compared to the single exposure case.

IV. DPL-AWARE SRAM SIZING

From the chip-level measurements and simulation-based analysis, we can conclude that there is a need for DPL-aware analysis and optimization of SRAM. We suggest one such technique, DPL-aware SRAM sizing, where the SRAM cell is resized under double patterning assumptions. The sizing optimization is performed at nominal V_{DD} (1.1V), where write operation is much more stable than read (for nominally sized cell, write margin is $6.06\sigma_{VT0}$ and read margin is $4.03\sigma_{VT0}$). Hence, the sizing optimization tries to make the read operation more robust. This is done by iteratively sizing the SRAM cell, while using DPL-based analysis to guide each sizing step until a yield requirement is met. Only the widths of the pull up, pull down and access transistors are used as optimization variables, and the optimization is constrained by limits on maximum dynamic energy, read and write times (to avoid access failures). A sensitivity metric calculated based on double patterning assumptions is used to choose the optimization variable to change at every iteration step. We perform such a sizing optimization on a 45nm industrial SRAM cell, for the case when the two line-width distribution curves differ by 5% in mean and each distribution has 3σ/μ of 10%. Figure 11 shows the distribution of the read margins for the optimized and unoptimized case, along with their Gaussian fits, for a maximum allowed change in dynamic energy of 5%. DPL-aware sizing optimization makes the read operation much more robust by shifting the distribution to the right (higher values of read margin means lower probability of failure and more robustness). Proposed optimization shifts the μ-3σ point of the distribution by ~6.2% decreasing the failure probability by 2.17X. For the DPL-aware resizing, μ-3σ for the write margin distribution decreases to ~$5.27\sigma_{VT0}$ from its value of ~$5.43\sigma_{VT0}$ for the unoptimized case (~2.9% change). Even after the sizing optimization, write operation remains the more robust operation, but read robustness improves significantly.

V. CONCLUSION

The impact of pitch splitting double patterning lithography (DPL) on SRAM robustness is analyzed for the first time. A test chip was implemented in a 45nm CMOS technology using DPL. Statistical analysis of write failures measured in 75 dies verifies the significant effect of double patterning on SRAM failures. We also investigate a DPL-aware SRAM sizing technique that effectively mitigates DPL based yield loss.

Acknowledgements

The authors thank STMicroelectronics for chip fabrication and general support of this project.

References

[1] G. Capetti *et al.*, "Sub k1 = 0.25 Lithography with Double Patterning Technique for 45nm Technology Node Flash Memory Devices at 193nm," *Proc. SPIE Optical Microlithography*, vol. 6520, pp. 65202K-1 - 65202K-12.

[2] H. H. Solak *et al.*, "Sub-50 nm period patterns with EUV interference lithography, " *Microelectronic Engineering*, vol. 67-68 , Issue 1, pp. 56-62, 2003.

[3] R. H. French *et al.*, "High Index Immersion Lithography With Second Generation Immersion Fluids To Enable Numerical Apertures of 1.55 For Cost Effective 32 nm Half Pitches," *Proc. SPIE Optical Microlithography XX*, 6520, 2007.

[4] C. Vieu *et al.*, "Electron beam lithography: resolution limits and applications," *Applied Surface Science*, vol. 164, pp. 111-117, 2000.

[5] M. Dusa et al., "Pitch Doubling Through Dual-Patterning Lithography: Challenges in Integration and Litho Budgets," *Proc. SPIE Conference on Optical Microlithography*, 2007, pp. 65200G-1 - 65200G-10.

[6] S. Mukhopadhayay et. al, "Modeling of Failure Probability and Statistical Design of SRAM Array for Yield Enhancement in Nanoscaled CMOS," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Volume 24, Issue 12, pp. 1859-1880, December 2005.

[7] S. Verhaegen et. al, "Litho variations and their impact on the electrical yield of a 32nm node 6T SRAM cell," *Proc. SPIE*, vol. 6925, 69250R, 2008.

[8] C. Sarma et. al, "Double exposure double etch for dense SRAM: a designer's dream," *Proc. SPIE*, vol. 6924, pp. 692429-692429-9, 2008.

[9] R. R. Wilcox, "Introduction to robust estimation and hypothesis testing," *Elsevier academic press*, 2005, p. 155.