A 695 pW Standby Power Optical Wake-up Receiver for Wireless Sensor Nodes

Gyouho Kim, Yoonmyung Lee, Suyoung Bang, Inhee Lee, Yejoong Kim, Dennis Sylvester, David Blaauw
University of Michigan, Ann Arbor, MI 48109

Abstract — We propose an ultra-low power optical wake-up receiver with a novel front-end circuit and communication scheme suitable for miniature wireless sensor node applications. Named "FLOW" for *F*ree-space *L*ow-Power *O*ptical *W*ake-up, the receiver consumes 695pW in standby mode, which is ~6,000× lower than previously reported RF and ultrasound wake-up radios. In active mode, it consumes 140pJ/bit at 91bps. A pulse width modulated communication encoding scheme is used, and chip-ID masking enables selective batch-programming and synchronization of multiple sensor nodes.

I. Introduction

In recent years, wireless sensor networks (WSN) have been one of the main foci of low power circuit research, enabling a wide range of new application domains for semiconductor electronics. WSN nodes rely on limited energy stored in the battery, which becomes an increasingly difficult constraint as the nodes shrink in volume. To maximize sensor node lifetime, heavy duty-cycling is used under the premise that standby power is negligible compared to active power. Hence, minimizing standby power is critical, particularly when sensors find themselves in poor conditions for harvesting energy, such as indoor or night operation for solar cells.

One key component in a WSN node is a wake-up receiver that stays on at all times to enable external interrupt, synchronization, and reprogramming. Given the miniature size of sensors and their inaccessibility after being deployed, wired connections are impractical. RF solutions are conventionally used [1]-[2], exhibiting high throughput at the cost of high power consumption (>10s of μW). Recently, an ultrasound solution was proposed [3], but its 4.4μW standby power remains high compared to the nW power budgets in small sensor nodes such as those in [4]-[5]. This approach also requires a piezoelectric material to be bonded to the CMOS die, complicating system integration. Free-space optical solutions exist [6], but they are not integrated and consume hundreds of μW.

II. Proposed Solution

We propose *F*ree-space *L*ow-power *O*ptical *W*ake-up (FLOW), a fully integrated sub-nW optical wake-up receiver and communication scheme. The FLOW receiver consumes 695pW in standby mode and 12.7nW in active mode. The role of FLOW in a WSN is two-fold: 1) initial programming after sensor node system assembly, and 2) rescuing a sensor node after catastrophic failure by re-programming and re-synchronizing timers. The latter is required if 1) nodes become unsynchronized, effectively disabling timing-sensitive node-to-node RF communication, 2) the sensor node restarts from a power shutdown mode due to poor harvesting conditions, or 3) the CPU program encounters an unforeseen error and requires a hard reset. Hence, it is critical that the FLOW receiver remains on at all times and does not require a software stack, which is commonly needed in RF wake-up receivers.

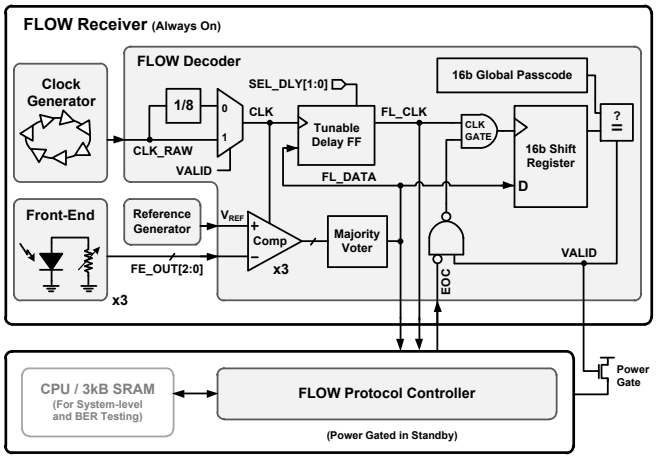

Figure 1. System block diagram of FLOW (Free Low-power Optical Wake-up). The FLOW receiver remains on at all times, consuming 695pW, while the protocol controller, CPU, and SRAM are power-gated in standby mode.

FLOW was integrated in a WSN node [4] where it can directly load a program into the memory, trigger control signals to wake up the CPU, set configuration bits, and turn on an RF radio block to initiate high-speed communication. With FLOW, multiple nodes can be addressed in parallel using a global 16-bit access code while a programmable chip-specific ID code allows communication to a specific subset of nodes.

III. Circuit Description

The FLOW receiver is comprised of a decoder, protocol controller, reference generator, clock generator, and three identical front-end circuits, whose outputs are majority-voted (Fig. 1). This redundancy in the front-end circuit improves robustness against false triggers and provides immunity against possible structural problems such as a dust particle blocking the path of light to the front-ends.

Each front-end circuit includes an n+/pw/nw parasitic diode as a PV cell and pull-down resistors in parallel with the diode (Fig. 2). One of the key challenges of an optical front-end is to

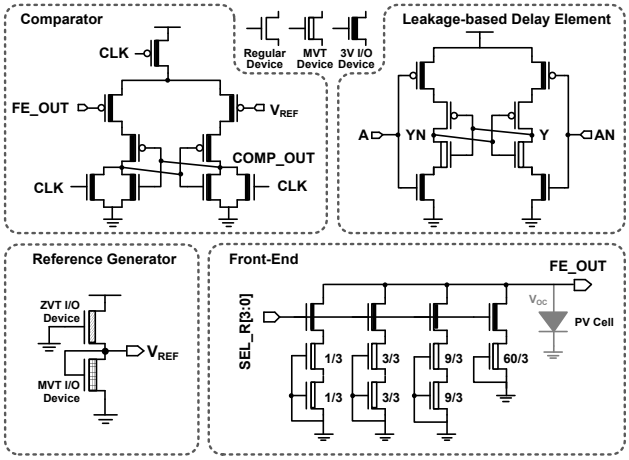

Figure 2. Circuit schematics of the comparator, leakage-based delay element used in clock generator, reference generator, and front-end with tunable off-state MOSFET resistors.

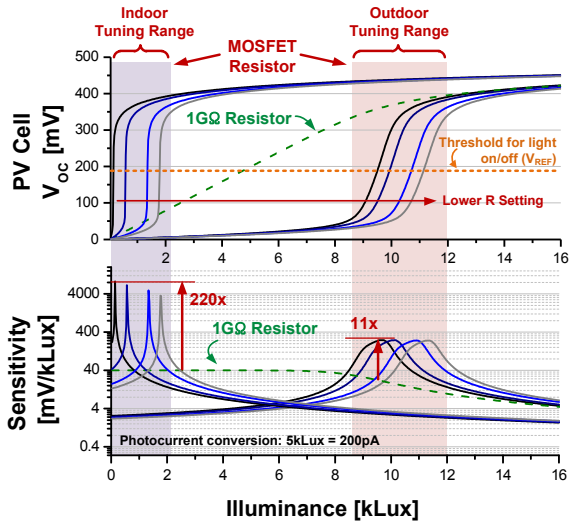

Figure 3. The non-linearity of off-state MOSFET resistance improves peak light sensitivity of the front-end output (PV cell's V_{OC}) by up to 220× compared to a linear resistor.

differentiate between high and low illumination levels in the presence of ambient light. The open circuit voltage (V_{OC}) of a PV cell's anode has a logarithmic dependence on illumination, hence a parallel pull-down resistor is required to control the V_{OC} response to illumination, as well as to speed up the falling transition of V_{OC}. As shown in Fig. 3, however, a linear resistor smoothes out the voltage response of V_{OC}, obscuring the definition of illumination levels. Since hundreds of MΩ is required to modulate a small PV cell current, a linear resistor implementation would also be impractical in terms of die area. Hence, we propose the use of an off-state MOSFETs, whose non-linear resistance characteristic improves the front-end's light detection sensitivity by up to 220× compared to a linear resistor, significantly improving ambient light immunity and signal integrity. With this approach, light level detection is achieved with a single reference and a comparator. The resistance can be easily tuned with SEL_R[3:0] depending on the operating conditions. Fig. 3 shows 8 out of 16 available resistor configurations, designed to cover both indoor and outdoor lighting conditions. Default resistor tuning bits are hard-coded so that FLOW can initially program under indoor conditions after the sensor node is fabricated and assembled. A 2-T low power reference circuit [7] generates a stable voltage of 190mV with σ of 4.8mV (1k Monte Carlo simulation result) to be used as a reference threshold for light level detection. A 2 kHz clock (CLK_RAW) is generated using a leakage-based oscillator [5] for reduced voltage sensitivity and low power.

Fig. 4 shows the pulse width modulated timing scheme of FLOW communication. Illumination pulse widths of t_{short} and t_{long} determine data bit values 0 and 1, respectively. The outputs of the three front-end circuits are digitized by the comparators and majority-voted to generate FL_DATA, which is delayed using a tunable delay flip-flop to create FL_CLK. FL_DATA is latched at the positive edge of FL_CLK. The delay of the tunable delay flip-flop is $t_{delay} = n \cdot t_{clk}$, where the parameter n is set by configuration bits

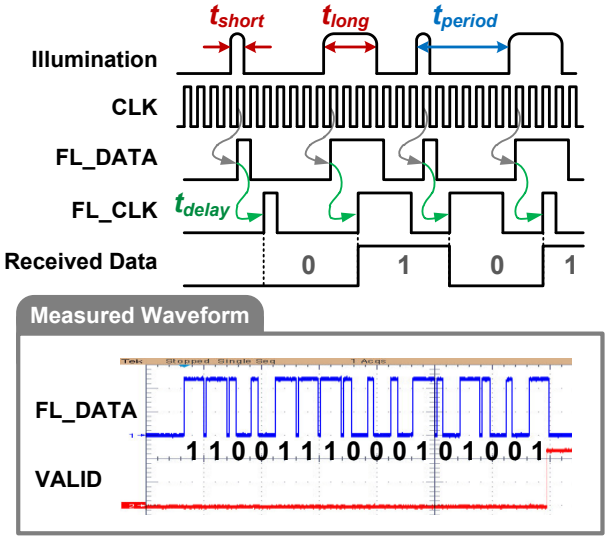

Figure 4. Timing diagram of FLOW's pulse-width modulated communication encoding scheme. The oscilloscope snapshot shows the VALID signal being triggered by the 16-bit global passcode.

SEL_DLY[1:0] to be between 7 and 29, with a default setting of 29. This delay serves as a safety margin to accommodate for batch programming. To achieve batch programming of multiple chips, process variation of CLK_RAW must be considered in determining a common data rate, $1/t_{period}$. Considering process variation in t_{clk}, the values of t_{short} and t_{long} have the following constraints:

$$2 \cdot t_{clk\_slow} < t_{short} < n \cdot t_{clk\_fast} \quad (1)$$

$$n \cdot t_{clk\_slow} < t_{long} < t_{period} \quad (2)$$

Hence the common data rate for FLOW batch transmission, $1/t_{period}$, is limited by the clock frequency of the slowest chip and delay parameter n, which can be lowered from its default value given less chip-to-chip variation.

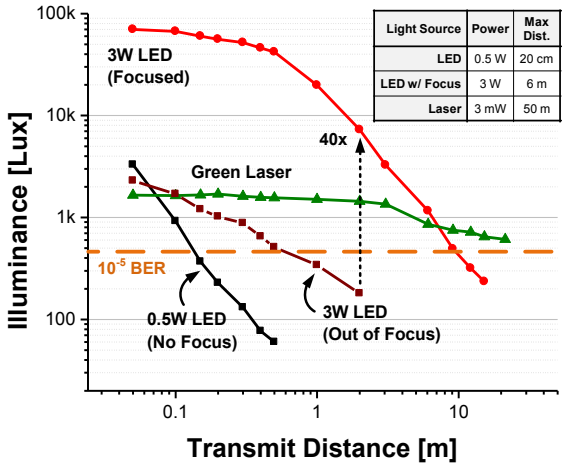

Figure 5. Illuminance measured at the receiver end versus light transmission distance for different classes of light sources. An off-the-shelf laser pointer can trigger FLOW from >50m.

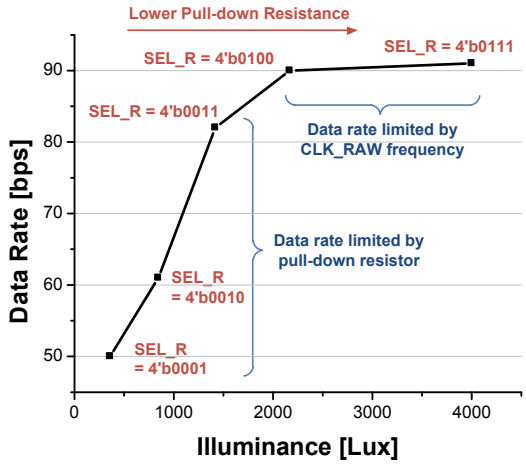

Figure 6. Data rate versus illuminance with optimal setting for resistor. High resistance is required for low light conditions, limiting data rate.

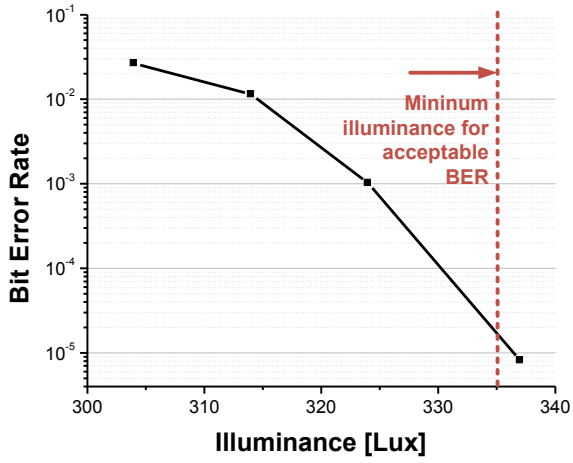

Figure 7. Bit error rate versus illuminance. Lowest measured BER is 8E-6. A relatively low illuminance of ~300 lux is required to achieve acceptable BER.

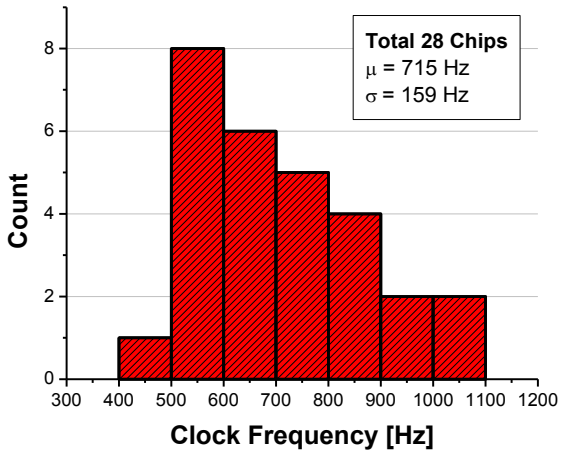

Figure 8. Measured clock frequency distribution of 28 chips. All 28 chips can be simultaneously programmed without prior tuning.

In standby mode, the FLOW receiver operates at 1/8th the nominal clock frequency to minimize standby power. The protocol controller is power-gated during this mode. To prevent false triggers from ambient light, a 16-bit predetermined code is used as a global passcode. Once the incoming stream of FL_DATA matches this 16-bit code, the VALID signal wakes up the protocol controller and increases the clock frequency by 8× to enable full speed data transfer. The protocol controller then receives and interprets the subsequent FL_CLK and FL_DATA, which follow a custom communication protocol. The controller first checks for a local chip ID that is used to address groups of chips or individual chips, enabling selective batch programming. It then processes a header containing transmission data length and parity bits to validate transmission. The header is followed by data, and once the FLOW transmission completes or FL_DATA is idle for more than 21 seconds, the protocol controller asserts the EOC (End-Of-Communication) signal, resetting the FLOW receiver into standby mode. The protocol controller has direct access to memory, and can send interrupt messages to the CPU to start executing code, effectively taking full command of the WSN node.

IV. Measurement Results

The proposed FLOW receiver was fabricated in 180nm CMOS technology and successfully tested. It was also integrated in a WSN node [4] with an ARM M0 CPU and 3kB SRAM, which were used for BER testing and sensor node system-level testing. Three different light sources were used for communicating with FLOW: a 0.5W 45lm LED without focus, a 3W 134lm LED with manual focus, and a 3mW green laser. Receiver performance depends on the illuminance received at the surface of the chip. As shown in Fig. 5, the power and optics of the light source strongly impacts the illuminance. With the laser, FLOW can be triggered from a distance of 50m, with longer range measurements limited by the testing environment. This demonstrates the advantage of optical communication as it enables long distance transmissions with simple, commonly available transmit

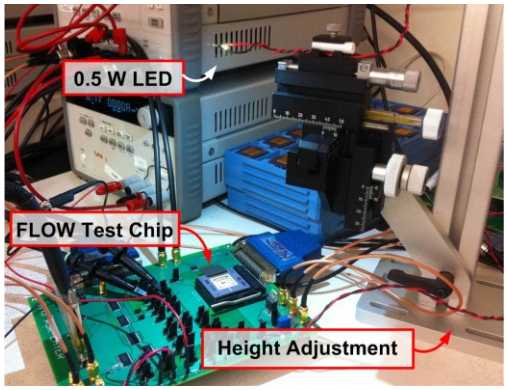

Figure 9. Test setup with 0.5W LED controlled by NI Labview. Ambient office light interference does not affect FLOW operation.

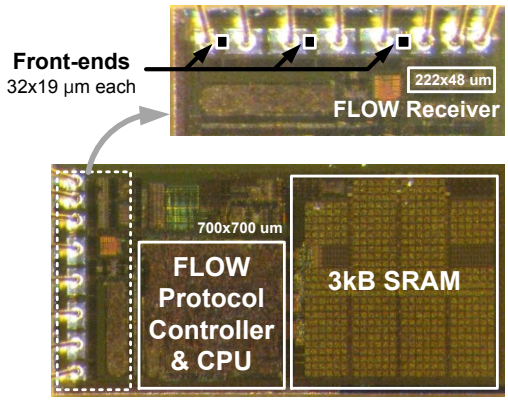

Figure 10. Die photo in 180nm CMOS. The three front-end circuits are placed between bonding pads for light exposure in a stacked system.

sources. With higher illuminance, the pull-down resistance setting can be reduced, resulting in faster pull-down of the diode voltage and increased data rate, with a maximum measured data rate of 91bps (Fig. 6). Data rate can be further increased by adding a faster clock generator while retaining low standby power by power-gating this fast clock in standby mode. The measured clock generator consumes 520pW, so if a clock is already available in the system, total FLOW power overhead would be only 175pW. Bit error rate also declines with higher illuminance; a minimum illuminance of 37lux was needed to obtain a BER of 8.1E-6 (Fig. 7).

To demonstrate batch programming, clock distribution among 28 chips was measured (Fig. 8). At the default delay parameter of n=29, all 28 chips can be simultaneously programmed with a common data rate of 14bps without prior tuning. Based on the measured CLK_RAW frequency σ of 159 Hz, the default delay setting can cover ±3σ clock variation, leading to 99.7% yield. Both batch programming and chip-ID masking was verified with multiple chips.

Fig. 9 shows the testing setup with a 0.5W LED controlled by NI Labview. WSN node system-level functionality was verified by transferring a 1kB program through FLOW without any prior tuning, followed by successful program

TABLE I
MEASURED PERFORMANCE SUMMARY AND COMPARISON

	[1]	[2]	[3]	[6]	This Work
Transmit Method	RF	RF	Ultrasound	Optical	Optical
Technology	65nm	90nm	65nm	No IC	180nm
Fully Integrated	Yes	No	No	No	Yes
Supply Voltage	1.2V	0.5V	0.6V	3.3V	1.2V
Standby Power	415µW	52µW	4.4µW	317µW	695pW
Max. Data Rate	500kbps	100kbps	250bps	2kbps	91bps
Energy/Bit	830pJ/b	520pJ/b	18nJ/b	159nJ/b	140pJ/b
Range	-	-	8.6m	15m	50m
BER	$<10^{-4}$	$<10^{-5}$	$<10^{-3}$	-	$<10^{-5}$

execution by the CPU. Fig. 10 shows the die photo of the test chip; the three front-ends are placed between bonding pads to demonstrate FLOW feasibility in a die-stacked system.

V. CONCLUSION

This paper proposed a novel ultra-low power optical wake-up receiver and communication scheme suitable for wireless sensor nodes. We have demonstrated stable operation with good transmission distance with 140pJ/bit operation and 695pW standby power. Table I summarizes the measurement results and compares to previously proposed RF and ultrasound wake-up receivers.

ACKNOWLEDGEMENTS

The authors thank NSF for funding and Prof. Prabal Dutta at the University of Michigan for valuable discussions.

REFERENCES

[1] S. Drago *et al.*, "A 2.4 GHz 830pJ/bit duty-cycled wake-up receiver with −82dBm sensitivity for crystal-less wireless sensor nodes," *IEEE International Solid-State Circuits Conference*, 2010.

[2] N. Pletcher *et al.*, "A 52µW Wake-Up Receiver With -72 dBm Sensitivity Using an Uncertain-IF Architecture," *IEEE Journal of Solid-State Circuits*, 2009.

[3] K. Yadav *et al.*, "A 4.4µW Wake-Up Receiver using Ultrasound Data Communications," *IEEE Symposium on VLSI Circuits*, 2011.

[4] Y. Lee *et al.*, "A Modular 1mm3 Die-Stacked Sensing Platform with Optical Communication and Multi-Modal Energy Harvesting," *IEEE International Solid-State Circuits Conference*, 2012.

[5] G. Chen *et al.*, "Millimeter-Scale Nearly Perpetual Sensor System with Stacked Battery and Solar Cells," *IEEE International Solid-State Circuits Conference*, 2010.

[6] J. Mathews *et al.*, "Low Power Wake-Up in Wireless Sensor Networks Using Free Space Optical Communications," *IEEE SENSORCOMM*, 2010.

[7] M. Seok *et al.*, "A 0.5V 2.2pW 2-Transistor Voltage Reference," *IEEE Custom Integrated Circuits Conference*, 2009.