# Reconfigurable Sleep Transistor for GIDL Reduction in Ultra-Low Standby Power Systems

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***Abstract*— Standby power reduction is critical to battery life and volume reduction in mm-scale sensor nodes. Power gating is extensively adopted to reduce leakage, but the inserted sleep transistors can suffer from other leakage mechanisms, namely GIDL, which become dominant at battery voltages of 3 V or higher. This paper introduces the concept of reconfigurable sleep transistors, in which two different topologies are used in active versus sleep mode. In active mode, transistors are stacked as in traditional power gating schemes. In sleep mode, sleep transistors are reconfigured to reduce GIDL current, in addition to subthreshold leakage. Measurements on a 180nm CMOS test chip shows 12.6× standby leakage reduction at $V_{DD}$=4.0 V and T=25°C. This improvement comes with acceptable area penalty due to additional small reconfiguration transistors and separate body contacts, and no impact on active mode operation.**

## I. Introduction

Miniaturized ($mm^3$) sensor nodes with indefinite operation have been recently demonstrated based on techniques that bring average system power down to 1-10 nW levels [3,4]. Such nodes are rarely active and spend most of their time in sleep mode, hence their average power is largely determined by the standby leakage [5].

Until now, a wide range of techniques have been proposed to reduce subthreshold leakage during sleep mode in ultra-low power systems [5], including aggressive voltage scaling [6], dynamic body biasing [9], and sleep transistors [7-10]. However, such techniques are not necessarily effective in suppressing other leakage contributions such as gate-induced drain leakage (GIDL) of sleep transistors, which dominates at battery voltages ($V_{DD}$) of 3V or higher. Such battery voltages are commonly observed in highly integrated mm-sized sensor nodes, as they typically rely on batteries with high energy density. For example, Cymbet printed batteries with $mm^2$ size have a typical operating voltage range of 3.6-4.0V [2].

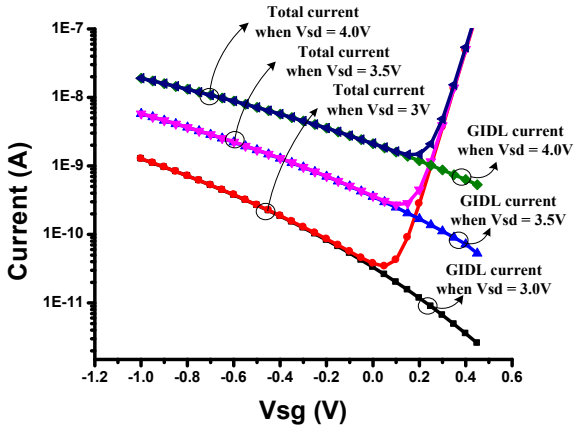


Figure 1. Simulated GIDL and overall leakage of p-MOSFET transistor ($W/L$=1012) versus $V_{SG}$.

The importance of GIDL at such voltages is shown in Fig. 1, which plots GIDL and overall leakage of a PMOS transistor versus $V_{SG}$ for $V_{DD}$ of 3, 3.5V, and 4V in 180nm CMOS (note that older technologies are often used in sensor nodes due to low leakage, and the sensor's relatively low performance requirements). Fig. 1 shows that GIDL becomes dominant in the overall leakage budget for higher $V_{SD}$, even at $V_{SG}$=0 V. Hence, new techniques to suppress GIDL in sleep transistors are needed to prolong battery lifetime in mm-size sensor nodes using ultra-compact batteries.

This paper introduces the concept of reconfigurable sleep transistors to suppress GIDL, in addition to subthreshold leakage. Various topologies based on this concept are proposed and compared to existing solutions through measurements of a 180nm test chip at various temperatures. Reconfigurable sleep transistors are demonstrated to enable 12.6× standby leakage reduction at $V_{DD}$=4.0 V and T=25 °C, at acceptable area overhead and no active mode performance penalty.

## II. Sleep Transistor Leakage and Proposed Reconfigurable Topology

### A. Sleep transistor leakage

We begin by considering the typical stacked sleep transistors as shown in Fig. 2b, which are preferred over the single sleep transistor in Fig. 2a for extremely low subthreshold leakage [7,10]. Transistors in Fig. 2 are conventionally sized to set the on-resistance in active mode (and hence the voltage drop) lower than a given specification. An example constraint would be that the virtual supply $VV_{DD}$ remains close to the supply voltage $V_{DD}$ (e.g., within 5-10%). In sleep mode, the sleep transistor conducts leakage current that is dominated by either GIDL or subthreshold leakage, depending on the value of $V_{DD}$. These leakage mechanisms differ significantly since the former increases with reverse body biasing and negative gate biasing (i.e., super cut-off), in contrast to the latter.

GIDL current of a p-MOSFET can be expressed according to the BSIM4 model [11] as

$$I_{GIDL} = AGIDL \cdot W_{eff} \cdot N_f \cdot \frac{V_{gd} - EGIDL}{3 \cdot T_{oxe}} \cdot \exp\left(-\frac{3 \cdot T_{oxe} \cdot BGIDL}{V_{gd} - EGIDL}\right) \cdot \frac{V_{bd}^3}{CGIDL + V_{bd}^3} \quad (1)$$

where $AGID$, $BGIDL$, $CGIDL$, and $EGIDL$ are technology-dependent GIDL coefficients, $V_{sd}$ and $V_{sge}$ are the source-drain and effective source-gate voltages, respectively, $T_{oxe}$ is the electrical gate equivalent oxide thickness, and $V_{bd}$ is the bulk-drain voltage. Here, (1) was obtained by substituting $V_{sd} - V_{sge} = V_{gd}$ into BSIM4 standard equations. From (1), GIDL current is reduced by minimizing voltages $V_{gd}$ and $V_{bd}$, while channel width $W_{eff}$ cannot be used as a knob for GIDL since it is sized according to active mode performance requirements as discussed above.

From the exponential dependency of GIDL on $V_{DD}$ (through $V_{gd}$ and $V_{bd}$) in (1), GIDL becomes negligible and subthreshold leakage dominates at low supply voltages. The stack configuration in Fig.

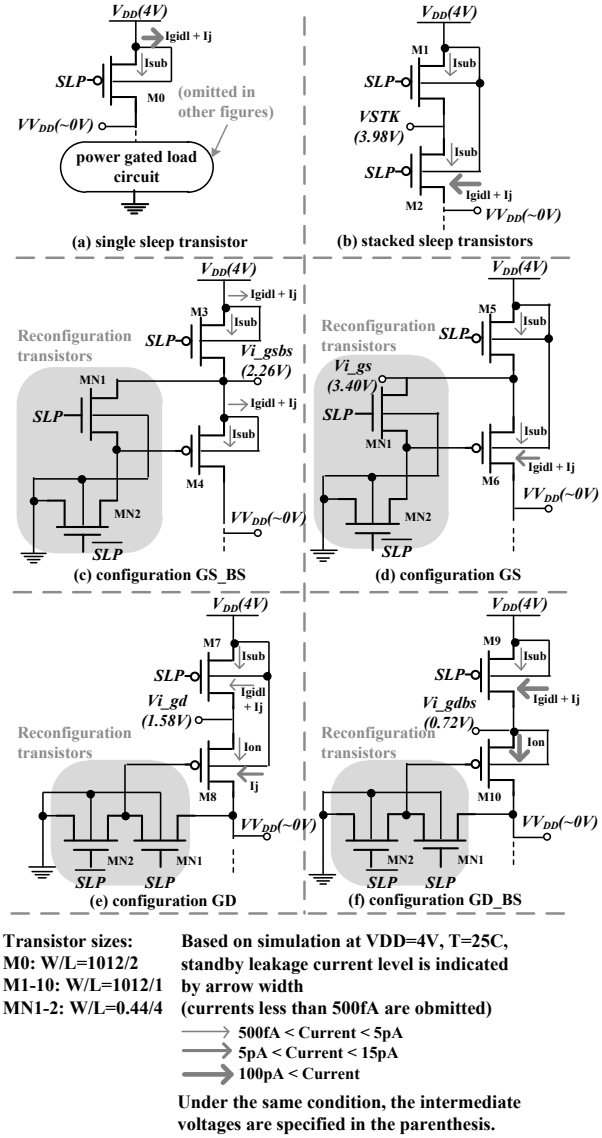


Figure 2. Six different sleep transistor configurations: configuration GS_BS is proposed for best GIDL reduction. Transistor sizes are indicated. Load is connected to drain of the bottom transistor in each configuration (M0, M2, M4, M6, M8, M10). GS stands for gate and source connected in sleep mode in the bottom transistor. GD stands for gate and drain connected in sleep mode. BS means body and source connected in sleep mode. BS means body and source of the bottom transistors are tied. Igidl, Ij, Isub and Ion refer to GIDL, junction leakage, subthreshold leakage and on-current, respectively.

2b is an effective way to reduce subthreshold leakage due to the stack effect in M1-M2, and is commonly used to reduce standby power in low voltage systems where subthreshold leakage dominates.

### *B. Proposed reconfigurable sleep transistors*

While the configuration of Fig. 2b achieves ultra-low subthreshold leakage, GIDL becomes a serious issue at larger supply voltages since both $V_{gd}$ and $V_{bd}$ in (1) tend to be high (i.e., close to $V_{DD}$). Specifically, the gate and body voltage of M2 are at $V_{DD}$ and its drain voltage is very close to ground, due to the large voltage drop across well-designed sleep transistors [10]. Ideally GIDL would be significantly reduced by setting the gate and/or body voltage of M2 such that $V_{gd}$ and $V_{bd}$ in (1) are minimized. The main idea of this paper is to minimize GIDL by reconfiguring the topology in Fig. 2b to set the voltages across transistor M2 as follows:

- In active mode (*SLP* is low), the gate voltages of M1 and M2 (i.e., the sleep signal) are equal to 0, so that active mode operation is the same as in Fig. 2b;
- In sleep mode (*SLP* is high), voltages $V_{gd}$ and $V_{bd}$ of off-transistors are reduced compared to Fig. 2b by setting their gate and/or body voltages lower than $V_{DD}$.

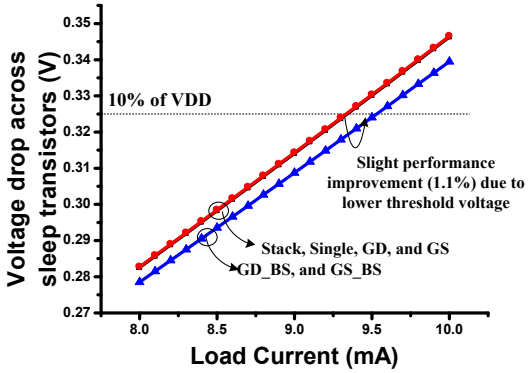


Figure 3. Simulated voltage drop across sleep transistors in active mode ($V_{DD}$=3.25 V, T=25 °C).

Such reconfiguration can be conceptually obtained by connecting the gate terminal of the bottom stacked transistor (M2 in Fig 2b) to ground only in active mode, while connecting it to an existing node with potential lower than $V_{DD}$ in sleep mode (e.g., the intermediate node between the two sleep transistors or $VV_{DD}$). This permits GIDL reduction without the need for generating an *ad hoc* voltage. To this aim, two reconfiguration transistors (MN1-MN2) are added in Figs. 2c-2f, which show four options found to be promising through preliminary simulations. The detailed operation of these topologies and their potential leakage advantages are detailed in Section III.

## III. Simulation & Measurement Results of Proposed Reconfigurable Sleep Transistor Topologies

The proposed sleep transistors in Figs. 2c-2f are sized to have the same on-resistance as the reference stacked sleep transistors in Fig. 2b. The area penalty of topologies in Figs. 2c-2f compared to Fig. 2b is due to the additional reconfiguration transistors MN1-MN2, as well as additional area for a separate body contact for M4 (M10) in Fig. 2c (Fig. 2f). The area penalty due to reconfiguration transistors is low since these transistors can be small (e.g., minimum size), considering that they do not affect the active mode on-resistance. The size of MN1-MN2 is constrained only by the required time to switch from/into sleep mode. The additional area of separate body contacts is also small compared to the large sleep transistors. Typical sleep transistor sizes for the above topologies are reported at the bottom of Fig. 2, where 10% virtual $V_{DD}$ degradation at $V_{DD}$=3.25 V and T=25°C was targeted, assuming a 9.3-mA load in active mode.

### *A. Active mode*

In active mode, configuration GD_BS (Fig. 2f) and GS_BS (Fig. 2c) were found to have the lowest virtual $V_{DD}$ voltage degradation among the considered sleep transistor configurations, although this

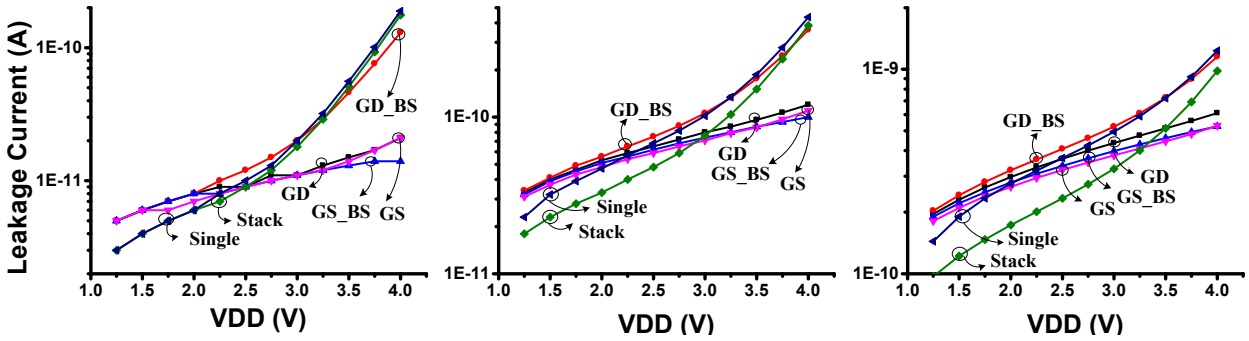


Figure 4. Measurement results of overall leakage for when sleep transistor is in sleep mode at 25°C (left), 50°C (center), and 75°C (right).

advantage was found to be limited (about 1%). This small advantage arises since the bottom transistor in configurations GD_BS and GS_BS (M4 and M10 in Figs. 2c and 2f, respectively) has its body connected to its source, thereby canceling body effect and reducing $|V_{TH,p}|$ compared to the other topologies. This is shown in Fig. 3, which plots the simulated voltage drop across the sleep transistors in active mode versus the current drawn by the power gated load (ranging from 8 to 10 mA) under the above conditions.

*B. Sleep mode*

All circuits in Fig. 2 were fabricated using thick-gate MOSFET in 180nm CMOS to comparatively evaluate the sleep mode leakage reduction over the traditional topologies in Figs. 2a-2b. The adopted sleep transistors sizes are shown in Fig. 2. The overall leakage current in each configuration was measured by sweeping the battery voltage $V_{BAT}$ from 1.25V to 4V, at 25, 50, and 75°C. Measured results are reported in Fig. 4.

Fig. 4 shows that the proposed configurations GS_BS, GS, and GD significantly reduce leakage for voltages higher than 2.75V at T=25°C, mainly due to the reduction of the dominant GIDL leakage component. In particular, GS_BS has the lowest leakage at $V_{DD}$>2.75 V, thanks to the symmetry of transistors M3-M4 in Fig. 2c, setting the intermediate voltage *Vi_gsbs* close to $V_{DD}/2$, which in turn reduces $V_{bd}$, $V_{gd}$ and GIDL in both M3 and M4 (see (1)). Fig. 5 shows the measured value of the intermediate voltage between the sleep transistors in the various configurations; it can be seen that GS_BS tracks $V_{DD}/2$ fairly well, leading to small $V_{gd}$ values.

Similarly, GS has lower GIDL than traditional stacked transistors since the intermediate voltage *Vi_gs* in Fig. 2d is lower than *VSTK* in Fig. 2b (as shown in Fig. 5, *VSTK* is very close to $V_{DD}$ because of reverse gate biasing of M2 in Fig. 2b). Since gate and source are short-circuited by MN1 in sleep mode, this results in a $V_{gd}$ reduction in M6 (see Fig. 2d), thereby reducing GIDL leakage from (1).

Analogously, GD has lower GIDL than traditional stacked transistors and GD_BS since gate and drain of M8 are short-circuited by MN1 in sleep mode. In GD and GD_BS, M8 and M10 are diode-connected and are still on in sleep mode, so GIDL from these devices is negligible and GIDL from only M7 and M9 are of interest. The intermediate voltage of GD (*Vi_gd* in Fig. 2e) is determined by negative feedback between GIDL current and body effect in M8. Lower *Vi_gd* increases M7 GIDL current in Fig. 2f, but reduces M8 on-current in Fig. 2f due to body effect. As a result *Vi_gd* is higher and closer to $V_{DD}/2$ than *Vi_gdbs*. On the other hand, GD_BS does not provide any GIDL reduction since intermediate voltage *Vi_gdbs* is close to 0 V (see Fig. 5) due to the zero body-source and gate-drain voltage of M10 in sleep mode. This increases

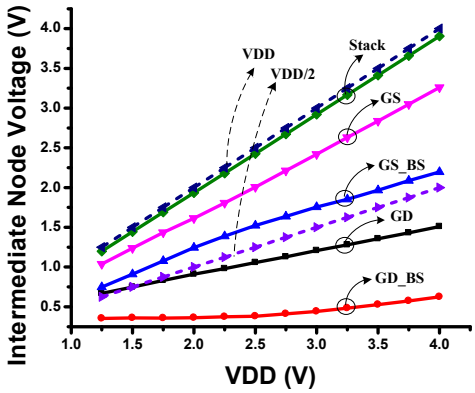


Figure 5. Measured intermediate voltages of proposed sleep transistor configurations and traditional stack sleep transistor in sleep mode T=25°C.

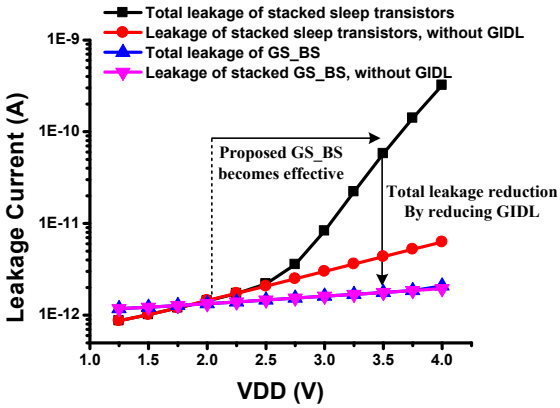


Figure 6. Simulated total and non-GIDL leakage vs. $V_{DD}$ in configuration GS_BS (Fig. 2c) and traditional stack (Fig. 2b) at 25°C.

$V_{gd}$ and $V_{bd}$ (and hence GIDL) for M9, compared to M1 in Fig. 2b. For these reasons, GD_BS provides no leakage reduction at either high or low $V_{DD}$, and its leakage profile resembles that of a single sleep transistor as *Vi_gdbs* is clamped to approximately the threshold voltage of M10.

The above considerations are summarized in Fig. 2, where the relative leakage current magnitude is qualitatively indicated by the arrow width, based on simulation results at $V_{DD}$=4V and T=25°C. Among the proposed topologies, GS_BS has the lowest GIDL and

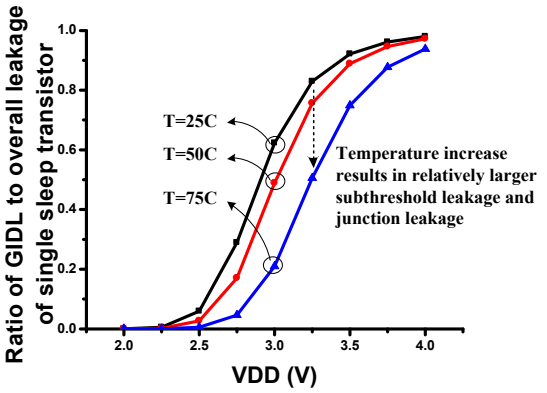


Figure 7. Simulated ratio of GIDL to overall leakage of a single sleep transistor (W/L=1012/2) in sleep mode vs. $V_{DD}$ at different temperatures

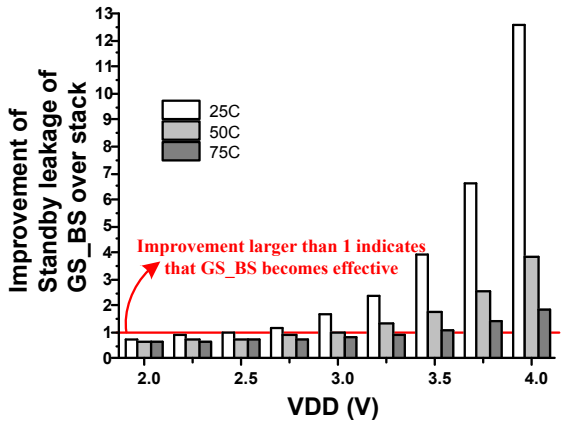


Figure 8. Standby leakage improvement ($I_{stack}/I_{GS\_BS}$) of proposed configuration GS_BS over stack.

TABLE I. STATISTICAL PROCESS AND MISMATCH VARIATION SIMULATION RESULTS OF TOTAL STANDBY LEAKAGE CURRENT (PA) AT DIFFERENT TEMPERATURES AND $V_{DD}$ =4V (500 RUNS FOR EACH):

| Temp. | Config. | single | stack | GS_BS | GS | GD | GD_BS |
|---|---|---|---|---|---|---|---|
| 25 C | Mean | 269.60 | 269.40 | **2.25** | 16.86 | 12.73 | 146.70 |
| | S.D. | 63.90 | 63.83 | **0.65** | 4.82 | 2.03 | 39.81 |
| 50 C | Mean | 359.50 | 358.60 | **9.60** | 28.95 | 22.82 | 235.50 |
| | S.D. | 80.82 | 80.69 | **3.89** | 8.96 | 5.58 | 60.45 |
| 75 C | Mean | 482.70 | 478.80 | **46.19** | 68.00 | 63.35 | 379.30 |
| | S.D. | 107.00 | 106.80 | **18.62** | 22.98 | 20.67 | 96.38 |

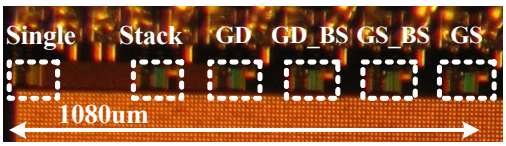


Figure 9. Die photo: Configuration single, stack, GD, GD_BS, GS_BS, GS from left.

overall leakage. Regarding GS, it has higher $V_{bd}$ in M6 (its body is tied to $V_{DD}$), which in turn leads to higher GIDL and junction leakage compared to GS_BS. GD exhibits higher junction leakage than GS_BS due to a higher $V_{bd}$ in M8 compared to M4.

As expected from qualitative considerations in Section II, the proposed reconfigurable sleep transistor GS_BS, GS, and GD offer a substantial leakage reduction at moderately high $V_{DD}$ through GIDL mitigation, whereas they provide no benefit at low voltages at which subthreshold leakage dominates. This is shown in Fig. 6, which depicts the simulation results of the total and non-GIDL leakage for configuration GS_BS and the traditional stacked version (Fig. 2b) at 25°C. Regarding the temperature dependence, higher temperatures exponentially increase subthreshold leakage, while weakly affecting GIDL leakage, as shown in Fig. 7. GIDL therefore becomes a smaller fraction of total leakage at higher temperatures, hence the GIDL reduction offered by configuration GS_BS has a smaller impact. In particular, our measurements show that configuration GS_BS has the lowest leakage for $V_{DD}$>2.5 V at T=25°C (representative of most applications in ultra-low power sensors since no self-heating does not occur), for $V_{DD}$>3 V at T=50°C (possible in very high ambient temperatures), and for $V_{DD}$>3.25~3.5 V at T=75°C. As shown in Fig. 8, configuration GS_BS can reduce leakage by 2.41× at $V_{DD}$=3.25 V and by 12.6× at $V_{DD}$=4 V (T=25°C), compared to stacked transistors.

To consider the impact of process and mismatch variation, statistical simulation results (Monte Carlo) at different temperatures (T=25/50/75 °C) and $V_{DD}$ =4V are summarized in Table I. The results show the consistent effectiveness of GS_BS even under process and mismatch variation. The die photo is shown in Fig. 9.

## IV. CONCLUSION

We have proposed novel reconfigurable sleep transistors to reduce GIDL current in battery-driven ultra-low power sensors. Experimental comparisons with traditional configurations in 180nm CMOS were made to evaluate the efficacy of the new techniques. The proposed configuration GS_BS reduces leakage by up to 12.6× at $V_{DD}$=4 V and room temperature. Such an advantage comes with acceptable area penalty and no degradation in active mode performance.

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