A 266nW Multi-Chopper Amplifier with 1.38 Noise Efficiency Factor for Neural Signal Recording

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Abstract

A low power high efficiency neural signal recording amplifier with a novel multi-chopper technique is proposed and implemented in 180nm CMOS. The input referred rms noise is 1.54μV (1-500Hz) with 266nA tail current. The result corresponds to a 1.38 noise efficiency factor, which is the best reported among current state-of-the-art amplifiers.

Introduction

Recently, the recording of human body electrical signals has attracted growing attention. Specifically, several low power high density recording devices have been proposed [1]-[3]. Although digital power consumption scales well with technology improvements, the noise requirements of these systems restrict front-end amplifier power improvements due to the fundamental noise efficiency factor (NEF) limits (fundamental limit = 1 with an ideal single BJT amplifier). As a result the analog front-end power limits the number of channels in neural recording arrays, effectively holding back major advances in brain machine interfaces.

The fundamental power consumption limit of the analog front-end amplifier arises from the white noise of the input transistors. The amplifier NEF is given by:

$$NEF = V_{rms}\sqrt{\frac{2 \times I_{total}}{\pi \times V_T \times 4kT \times Bandwidth}}$$

State-of-art neural recording systems typically employ high accuracy amplifiers with a differential topology and high (> 100dB) power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR). In this case the typical NEF value is 3 [4] while amplifiers with relaxed PSRR and CMRR specifications (> 80dB) exhibit NEFs of ~1.5 [3].

In a traditional front-end amplifier, the current must be sufficiently large to achieve the target noise level. In setting the current to this level, amplifier bandwidth increases beyond the requirement of neural recording, translating to wasted power consumption. For example, setting the current to match a requirement of <5μV rms noise for ECG signal in 180nm will increase amplifier bandwidth to approximately 20kHz, which exceeds the sub-kHz ECG bandwidth requirement. To reduce the front-end amplifier power consumption, this paper proposes a novel multi-chopper technique to establish a new trade-off between bandwidth and white noise, and achieves a best-reported NEF.

Proposed Multi-Chopper Technique

Fig. 1 shows the concept of the multi-chopper technique. First consider a typical chopper amplifier with a single chopping frequency, in which the signal is modulated into a higher center frequency to avoid amplifying 1/f noise. After amplification, a second chopper demodulates the signal back into the baseband. In this case the noise added to the signal is the amplifier noise around the chopper frequency bandwidth.

In the multi-chopper scheme, multiple chopper switches are used along with a multiple-input / multiple-output current-reuse core amplifier. The target of the chopper here is both 1/f noise and white Gaussian noise. The amplifier operates as follows: 1) The input signal is modulated up into N different center frequencies by the different chopper switches (N=2 in Fig. 1 for clarity); 2) In the amplifying process, the signal is amplified by A for each of the N center frequencies. The output signal consists of the signal, which is A times larger than the input signal, plus the added amplifier noise at each center frequency; 3) Each chopper demodulates the amplified signal and added noise back into the baseband frequency; 4) A summing amplifier combines all N signals producing an output signal that is N×A times larger than the input. However, as explained shortly, the summed noise sources are uncorrelated and therefore sums only as $\sqrt{N}$, providing the key benefit of the approach. Since the clock of the chopper is a square wave rather than a sine wave the center frequencies are selected to be even multiples, thus avoiding coinciding harmonics. Fig. 2 shows the signal flow of the amplifier.

To quantify the benefits of the proposed scheme, the SNR improvement is calculated assuming a flat gain A throughout the entire amplifying bandwidth: 1) for N different chopper frequencies, the final output signal is N×A times larger. 2) Since the noise is uncorrelated in each chopper frequency domain, the summing amplifier sums the power rather than voltage amplitude. Hence, the power of the noise will be N times larger while the noise amplitude increases by only $\sqrt{N}$. 3) Since the gain of the signal is N×A while the gain in noise is $\sqrt{N}$, the proposed scheme improves SNR by $\sqrt{N}$. The choice of the number of chopper switches represents a trade-off between signal bandwidth (since the signal bandwidth f will be reduced by 1/(2N+1)) and Gaussian noise.

Fig. 3 shows the detailed implementation of the technique, focusing on a 2 chopper frequency version of the amplifier (N=2). The input signal is modulated up by a standard chopper switch and fed into corresponding input pairs of the multiple-input, multiple-output current-reuse core amplifier. AC coupling is used to achieve high CMRR. Fig. 3 also includes the schematic of the stacked differential pairs, which is similar to [5]. In this work, however, we implement the differential pairs in both NMOS and PMOS (rather than just PMOS [5]) to further reduce the noise introduced by the current reuse scheme. With both NMOS and PMOS inputs, the design operates similarly to an inverter-based technique [6], further improving NEF by $\sqrt{2}$. To avoid the low PSRRs commonly found in inverter-based amplifiers, power and ground are isolated by a current source as shown in Fig 3. The design also uses a simple common mode feedback scheme to balance the current mirror at PMOS and NMOS side.

Fig. 4 gives the small signal analysis of the amplifier. The top differential pairs operate as the traditional pairs. The output current of the topmost differential pair flows into the next pair, equally distributed to the positive and negative paths. A similar current is generated by the NMOS side and passes through the output resistor R_{out} to generate the output voltage. Note that the input signal at each pairs must be in different frequency domains or the signals will cancel each other, rendering the approach invalid.

Note that this scheme using N=2 yields 4 (or generally 2^N) output signals. By connecting the outputs with the correct polarity, as shown in Fig. 5, the output signals at the desired bandwidths can be collected, demodulated, and summed through the following summing amplifier. All transistors are biased in the subthreshold region (V_{th}=300mV with <150mV V_{gs}) to maximize current efficiency. As in other chopper amplifiers, the output signal contains ripple at the chopper signal itself. This is removed with a 4th-order filter after the summing amplifier using two biquad G_m-C filters connected in series (Fig. 5).

Both the capacitors inside the summing amplifier and the G_m-C filter can be tuned to retarget the amplifier to other applications. This allows the appropriate signal bandwidth and gain to be selected to match system requirements. Higher gain and lower bandwidth can be selected for EEG measurements while ECG will employ lower gain and higher bandwidth.

Measurement Results

To verify the efficacy of the proposed technique, 2-stack (N=2) and 3-stack (N=3) versions are implemented in 180nm standard CMOS. The 3-stack version is identical to the 2-stack version but includes one additional stack in the differential pair and sums 8 output signals. Fig. 6 shows gain and bandwidth for the 2-stack and 3-stack amplifiers. Fig. 7 shows their noise spectrum. The measured rms noise is 1.73μV and 1.54μV for the 2-stack and 3-stack versions, respectively, at a current consumption of 273nA and 266nA. From measurement results, the amplifier NEF is 1.71 and 1.38 with PSRR/CMRR of 93/87dB and 92/89dB for N=2 and N=3, respectively. Table I compares the amplifier performance to other designs. Fig. 8 shows the test chip die photo.

References

[1] V. Helleputte et al, ISSCC, 2012.
[2] W.-M. Chen et al., ISSCC, 2013.
[3] D.-Han et al., ISSCC, 2013.
[4] J. Fan et al., JSSC, 2011.
[5] B. Johnson et al., JSSC, 2013.
[6] J. Holleman et al., EMBS, 2007.

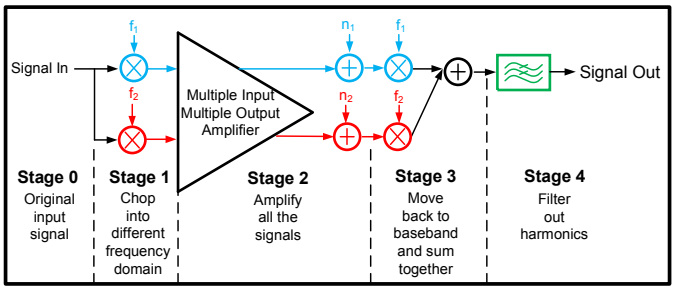

Fig. 1. Conceptual diagram of the multiple-chopper amplifier (2-stack version).

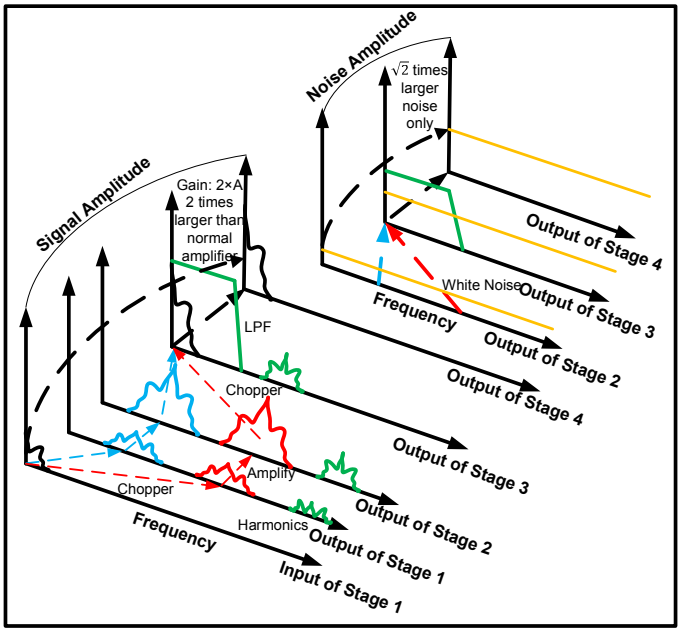

Fig. 2. Signal and noise flow for each amplifier stage (2-stack version) .

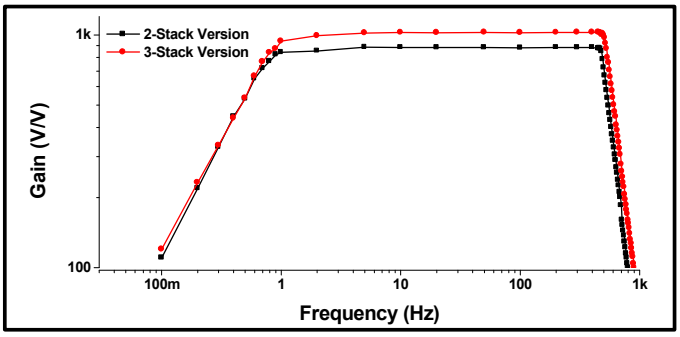

Fig. 6. Measured gain across frequency range with 500Hz bandwidth.

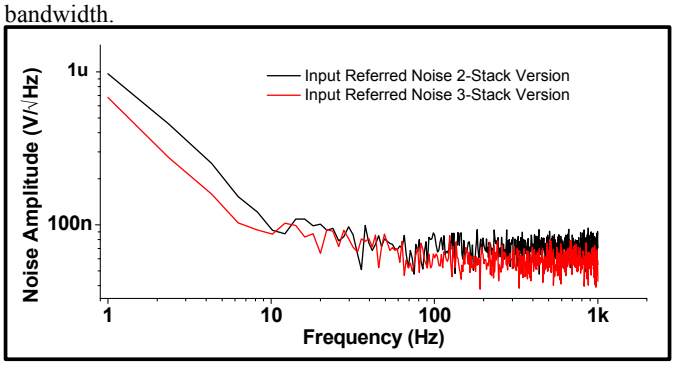

Fig. 7. Measured noise across 1Hz - 1kHz.

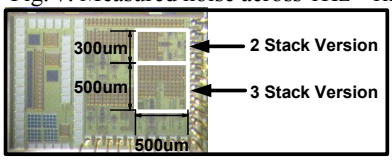

Fig. 8 Die photo in 180nm CMOS.

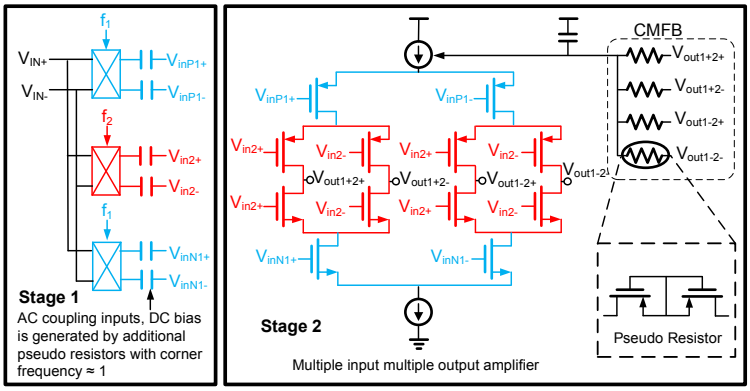

Fig. 3. Schematic of stage 1 (left) and stage 2 (right) of the amplifier (2-stack version).

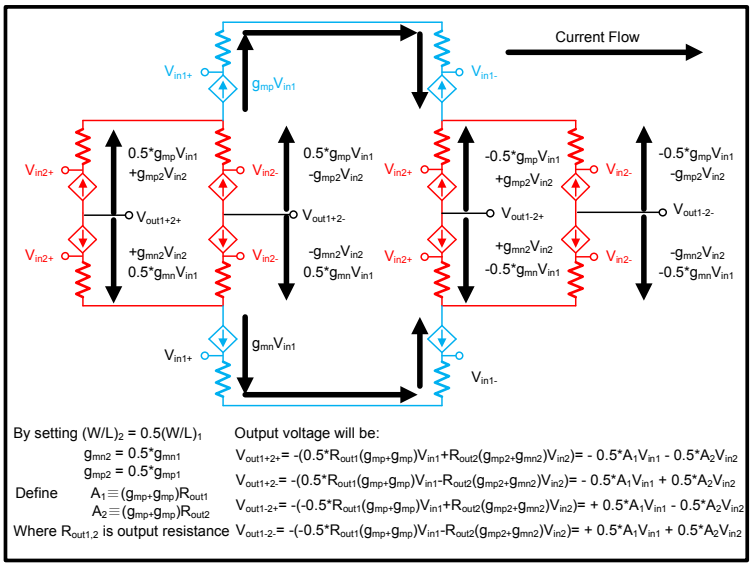

Fig. 4. Small signal analysis of the amplifier (2-stack version).

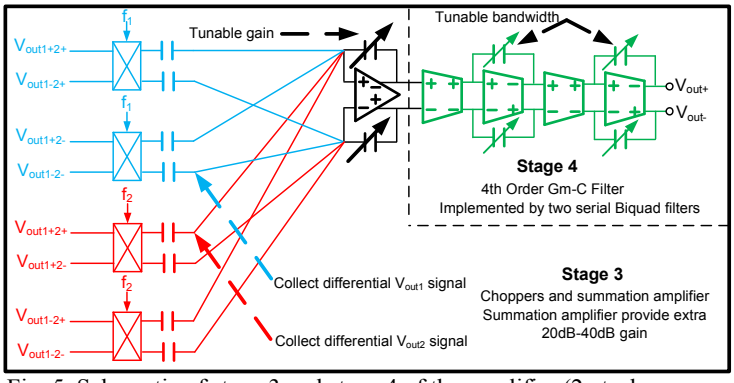

Fig. 5. Schematic of stage 3 and stage 4 of the amplifier (2-stack version).

Table I Summary Table

	[3]	[4]	[5]	[6]	2 Stack	3 Stack
Process	180nm	65nm	130nm	500nm	180nm	180nm
Power	0.73uW	1.8uA@1V	3.9μW	805nA@1V	273nA@1V	266nA@1V
Noise	3.2uV	1uV	3.7uV	3.6μV (0.3-4.7Hz)	1.91μV (1-500Hz)	1.54μV (1-500Hz)
Gain(dB)	52	40	40	36.1	38.91-56.53	41.76-59.15
Bandwidth(Hz)	10k	100	19.9k	4.7k	407.1-815.5	402.9-804.3
NEF	1.57	3.3	1.64	1.80	1.71	1.38
PSRR(dB)	73	120	80	5.5	93	92
CMRR(dB)	N/A	134	78	Single-Ended	87	89
THD	N/A	N/A	1% @ 16.7mVpp	7.1% @ 1mVpp	0.47% @ 1mVpp	0.54% @ 1mVpp
Area(mm^2)	N/A	0.1	0.125	0.046	0.15	0.25