An Ultra-Low Power Fully Integrated Energy Harvester Based on Self-Oscillating Switched-Capacitor Voltage Doubler

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Abstract—This paper presents a fully integrated energy harvester that maintains >35% end-to-end efficiency when harvesting from a 0.84 mm² solar cell in low light condition of 260 lux, converting 7 nW input power from 250 mV to 4 V. Newly proposed self-oscillating switched-capacitor (SC) DC-DC voltage doublers are cascaded to form a complete harvester, with configurable overall conversion ratio from 9× to 23×. In each voltage doubler, the oscillator is completely internalized within the SC network, eliminating clock generation and level shifting power overheads. A single doubler has >70% measured efficiency across 1 nA to 0.35 mA output current (>10^5 range) with low idle power consumption of 170 pW. In the harvester, each doubler has independent frequency modulation to maintain its optimum conversion efficiency, enabling optimization of harvester overall conversion efficiency. A leakage-based delay element provides energy-efficient frequency control over a wide range, enabling low idle power consumption and a wide load range with optimum conversion efficiency. The harvester delivers 5 nW–5 µW output power with >40% efficiency and has an idle power consumption <3 nW, in test chip fabricated in 0.18 µm CMOS technology.

Index Terms—DC-DC converter, energy harvester, self-oscillating, switched capacitor, ultra low-power, voltage doubler.

I. INTRODUCTION

RECENT advances in low power circuits have enabled mm-scale wireless systems [1], [2] for wireless sensor networks and implantable devices, among other applications. Energy harvesting is an attractive way to power such systems due to the limited energy capacity of batteries at these form factors. However, the same size limitation restricts the amount of harvested power, which can be as low as tens of nW for mm-scale photovoltaic cells in indoor conditions. Efficient

DC-DC up-conversion at such low power levels (for battery charging) is extremely challenging and has not yet been demonstrated.

Boost DC-DC converters are widely used to harvest energy from DC sources and yield high conversion efficiency [3]–[6]. However, they require a large off-chip inductor at low harvested power levels, increasing system size. Alternatively, switched-capacitor (SC) DC-DC converters can be fully integrated on-chip and are favored for form-factor constrained applications [7]–[14]. At low power levels, SC converter efficiency is constrained by the overheads of clock generation and level-conversion to drive the switches. As a result, efficient SC converter operation has been limited to the µW range.

This paper presents a fully integrated switched-capacitor energy harvester that consists of cascaded self-oscillating voltage doublers [15]. In each voltage doubler, an oscillator is completely internalized and clocking power overhead is reduced. The reduced power overhead of both clock generation and level shifting enables the harvester to operate with very weak power sources, as low as a few nWs. By completely integrating the clock generation in the SC, the overhead scales with the current load resulting in a very wide load range of $\sim 1000\times$. By adjusting the number of cascaded voltage doublers as well as with a new method of modulating the low voltage applied to each doubler stage, the overall conversion ratio can be configured between 9× and 23×.

Section II presents the structure of the self-oscillating voltage doubler and describes the frequency modulation scheme for efficiency optimization. Section III describes the energy harvester structure. Section IV presents measured results and Section V concludes the paper.

II. SELF-OSCILLATING VOLTAGE DOUBLER

A. Motivation and Basic Structure

As shown in Fig. 1, conventional SC DC-DC voltage doublers generally consist of three parts: clock generator, level shifter and switched capacitor network (SCN). The clock generator produces a clock, which is fed into the level shifters. The level shifters take the clock and create switch control signals for the SCN. As the clock oscillates, the SCN periodically
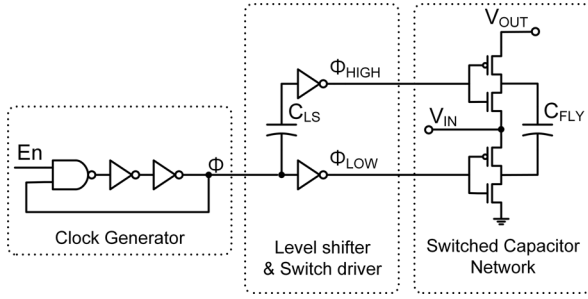
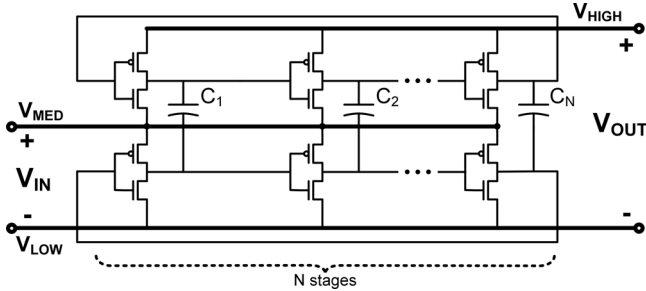Fig. 1. Structure of a conventional capacitive voltage doubler.

Fig. 2. Basic structure of the proposed self-oscillating voltage doubler.

changes its connections to generate the output voltage. Each of these blocks introduces power overhead, reducing efficiency. Looking at each transistor in the complete converter circuit, the dynamic power consumption of SCN switches directly contributes to generating output power, whereas the clock generator and level shifter power consumption does not contribute to output power. As a result, the basic motivation of the proposed self-oscillating voltage doubler is to remove the unnecessary power consumption of those secondary blocks and transistors.

Fig. 2 shows the basic structure of the self-oscillating voltage doubler. It consists of two stacked ring oscillators with output nodes of corresponding stages connected through flying caps ($C_1 \sim C_N$). In each stage, inverters from the top and bottom ring either charge or discharge the flying cap, thereby transferring power to the upper ring. Simultaneously, the inverters drive the next stage in their ring, creating a multi-phase DC-DC converter with overlapping charge/discharge phases and self-sustaining operation. Every transistor in this structure is essentially a flying cap switch and hence dynamic power loss is minimized since there are no superfluous transistors. The natural multi-phase operation reduces output voltage ripple with little cost.

Another advantage of this structure lies in reduced level shifting overhead. Conventional level shifters generally use output keepers, which generate contention loss in addition to dynamic power loss. This contention loss comes from the timing mismatch among the signals of a level shifter; depending on the amount of mismatch, contention loss can dominate dynamic power consumption and greatly reduce overall efficiency. Some previous SC voltage converters have used nonoverlapping clocks to reduce level shifting contention

loss [10]–[12]. However, this introduces another overhead, i.e., generation of the nonoverlapping clocks. Additionally, such a converter does not actively convert power during the nonoverlapping periods, reducing its maximum output power.

The self-oscillating voltage doubler has no dedicated level shifter because both ring oscillators actively generate their own clock signals. However, contention loss can still arise from phase mismatch between the two oscillations. This is mitigated by the fact that the two oscillators are synchronized at every stage and hence the amount of mismatch is very small, avoiding the need for nonoverlapping clocks. According to simulation results, phase mismatch is less than 1% of a fanout-of-4 (FO4) inverter delay, and contention loss from this mismatch is also under 1% of total dynamic power loss.

The self-oscillating voltage doubler is capable of self-startup regardless of its initial state. When V_{IN} is initially supplied to V_{MED}, the bottom oscillator starts oscillating. In each SCN stage of the doubler, both the nodes before and after the flying cap driver are coupled between the top and bottom oscillator. Therefore, even when V_{HIGH} is very low and the top oscillator is not oscillating by itself, the coupled nodes in the top oscillator will be rising and falling, and hence some charge is transferred to V_{HIGH} solely due to the driving capability of the bottom oscillator. Due to this fluctuation of the top nodes, V_{HIGH} can rise above the average voltage level of the top nodes. As V_{HIGH} becomes higher, the average level of the top nodes also increases, forming a positive feedback that raises V_{HIGH} above V_{MED}. As V_{HIGH} rises higher than V_{MED}, the top oscillator starts normal oscillation on its own. Because the top oscillator is initially much weaker than the bottom, the top oscillation is naturally synchronized to the bottom oscillator. After synchronization, the voltage doubler starts normal operation, continually generating output power.

B. Modulation Scheme for Optimum Conversion Efficiency

The self-oscillating voltage doubler is modulated to maintain optimum conversion efficiency over a wide range of output power levels. The specific goal of the modulation is to balance conduction and switching losses by examining the ratio of output to input voltages ($R_{DIV} = V_{OUT}/V_{IN}$). A low R_{DIV} indicates a large voltage across the switches and dominant conduction loss. Conversely, high R_{DIV} indicates low conduction loss (zero as $R_{DIV} \to 2$) and more dominant switching losses due to a higher frequency needed to transfer the same amount of load current.

To find optimum R_{DIV}, we first define C_{FLY} as the total amount of flying cap, f as the oscillation frequency, and Δ as the amount of voltage drop:

$$\Delta = 2V_{IN} - V_{OUT}. \tag{1}$$

The voltage doubler operates in a multi-phase manner with low ripple, and hence V_{OUT} is assumed to be constant in this analysis. In this case the input power to the voltage doubler P_{IN} can be approximately written as

$$P_{IN} = 2C_{FLY}V_{IN}\Delta f \tag{2}$$

by additionally assuming that $\Delta \ll V_{\mathrm{IN}}$ and that the top and the bottom oscillators have similar total parasitic capacitances. With these additional assumptions, the active current going out from V_{HIGH} to V_{MED} through the top oscillator is nearly reused as the active current flowing from V_{MED} into V_{LOW} through the bottom oscillator. Therefore, only a small portion of the total parasitic effect, or switching loss, is actually incorporated into the true input power, hence the approximate equation is relatively accurate. Simulation results also support the existence of this current reuse and the P_{IN} approximation. For example, in a simulation with $\Delta = 0.2V_{\mathrm{IN}}$, true input power differs from P_{IN} in (2) only less than 15% of the total switching loss.

Conduction loss L_C comes from the effective internal resistances of the voltage converter. Assuming DC at the power rails, this loss is the same as the loss from charge sharing, and can be written as

$$L_C = C_{\mathrm{FLY}} \Delta^2 f. \tag{3}$$

Switching loss L_S is the total dynamic power loss in the voltage doubler:

$$L_s = \left(\sum_{\mathrm{non-flying}} \alpha_i C_i V_{\mathrm{swing}_i}^2 \right) f = C_{\mathrm{EFF}} V_{\mathrm{IN}}^2 f \tag{4}$$

where C_i is every non-flying capacitor including parasitic capacitance, and V_{SWING} and α are the voltage swing and activity factor of each non-flying capacitor, respectively. C_{EFF} is defined as

$$C_{\mathrm{EFF}} = \sum_{\mathrm{non-flying}} \alpha_i C_i \frac{V_{\mathrm{SWING}_i}^2}{V_{\mathrm{IN}}^2} \cong \sum_{\mathrm{non-flying}} C_i \tag{5}$$

and is independent of the oscillation frequency. This value depends on Δ because the V_{SWING} of the top oscillator nodes depend on Δ, however it is fairly constant with $\Delta \ll V_{\mathrm{IN}}$.

The ratio of these losses to input power can then be written as

$$\frac{L_C}{P_{\mathrm{IN}}} = \frac{C_{\mathrm{FLY}} \Delta^2 f}{2 C_{\mathrm{FLY}} V_{\mathrm{IN}} \Delta f} = \frac{\Delta}{2 V_{\mathrm{IN}}} \tag{6}$$

and

$$\frac{L_S}{P_{\mathrm{IN}}} = \frac{C_{\mathrm{EFF}} V_{\mathrm{IN}}^2 f}{2 C_{\mathrm{FLY}} V_{\mathrm{IN}} \Delta f} = \frac{C_{\mathrm{EFF}} V_{\mathrm{IN}}}{2 C_{\mathrm{FLY}} \Delta}. \tag{7}$$

These two ratios are clear functions of Δ. Assuming $\Delta \ll V_{\mathrm{IN}}$ and neglecting the weaker dependency of C_{EFF} on Δ, the inequality of arithmetic and geometric means

$$\frac{x + y}{2} \geq \sqrt{xy} \tag{8}$$

can be applied as illustrated in Fig. 3, to obtain the lower bound of total loss ratio:

$$\frac{L_{\mathrm{TOTAL}}}{P_{\mathrm{IN}}} = \frac{L_C + L_s}{P_{\mathrm{IN}}} = \frac{\Delta}{2 V_{\mathrm{IN}}} + \frac{C_{\mathrm{EFF}} V_{\mathrm{IN}}}{2 C_{\mathrm{FLY}} \Delta}$$

$$\geq \sqrt{\frac{\Delta}{V_{\mathrm{IN}}} \times \frac{C_{\mathrm{EFF}} V_{\mathrm{IN}}}{C_{\mathrm{FLY}} \Delta}} = \sqrt{\frac{C_{\mathrm{EFF}}}{C_{\mathrm{FLY}}}}. \tag{9}$$
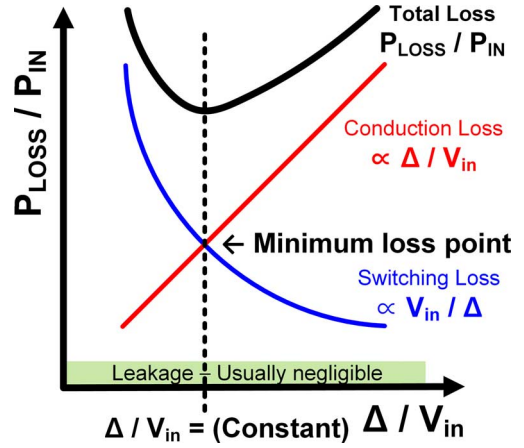

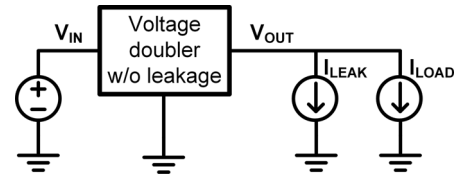Fig. 3. Rough dependency of voltage doubler loss elements on Δ.

Fig. 4. Leakage loss model of the voltage doubler.

Therefore, maximum efficiency η_{MAX} is

$$\eta_{\mathrm{MAX}} = 1 - \left(\frac{L_{\mathrm{TOTAL}}}{P_{\mathrm{IN}}} \right)_{\mathrm{MIN}} = 1 - \sqrt{\frac{C_{\mathrm{EFF}}}{C_{\mathrm{FLY}}}} \tag{10}$$

when the following equality condition is satisfied:

$$\frac{\Delta}{2 V_{\mathrm{IN}}} = \frac{C_{\mathrm{EFF}} V_{\mathrm{IN}}}{2 C_{\mathrm{FLY}} \Delta} \tag{11}$$

put differently:

$$\frac{\Delta}{V_{\mathrm{IN}}} = \sqrt{\frac{C_{\mathrm{EFF}}}{C_{\mathrm{FLY}}}} = \left(\frac{L_{\mathrm{TOTAL}}}{P_{\mathrm{IN}}} \right)_{\mathrm{MIN}} \tag{12}$$

or

$$R_{\mathrm{DIV}} = \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = 2 - \frac{\Delta}{V_{\mathrm{IN}}} = 2 - \sqrt{\frac{C_{\mathrm{EFF}}}{C_{\mathrm{FLY}}}} = 1 + \eta_{\mathrm{MAX}}. \tag{13}$$

Therefore, as long as the circuit operates properly and these two losses are dominant, its optimum efficiency is nearly a constant value that is determined by the ratio of total parasitic capacitances to the total flying capacitances C_{FLY}, and R_{DIV} at optimum efficiency is also a constant.

As output power becomes smaller, leakage power loss becomes dominant over the conduction and switching losses. Leakage loss can be modeled as a constant current sink attached to the output node, as shown in Fig. 4. In simulation, amount of equivalent leakage current, I_{LEAK}, does not vary over 8% across a wide output voltage range ($V_{\mathrm{IN}} < V_{\mathrm{OUT}} < 2 \times V_{\mathrm{IN}}$). In this model, overall conversion efficiency is

$$\eta_{\mathrm{overall}} = \eta_{\mathrm{without-leakage}} \times \frac{I_{\mathrm{LOAD}}}{I_{\mathrm{LOAD}} + I_{\mathrm{LEAK}}} \tag{14}$$
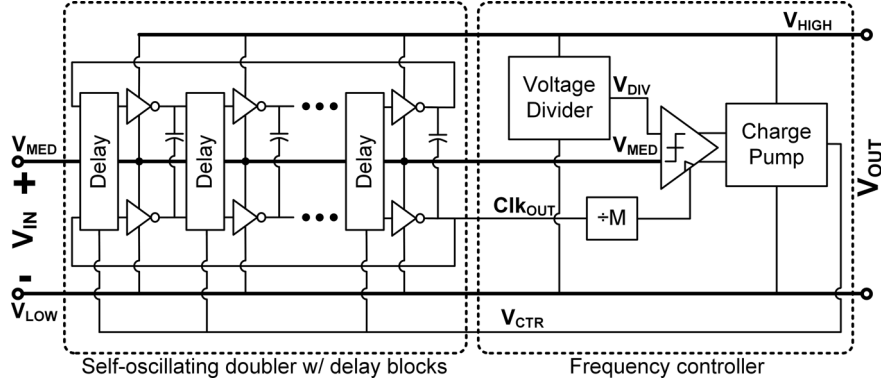
Fig. 5. Implementation of the voltage doubler with frequency modulation.

and is optimized with the same arguments as a voltage doubler with no leakage, if the load can be approximately considered as a constant current sink. Therefore, even when output power is very small, the optimum efficiency point is still at a similar condition to (13), namely:

$$R_{\text{DIV}} \cong 2 - \sqrt{\frac{C_{\text{EFF}}}{C_{\text{FLY}}}}. \qquad (15)$$

In this work, voltage doubler oscillation frequency is modulated to achieve optimum R_{DIV}. Delay blocks are inserted in the oscillation paths and their delay is controlled by an analog delay tuning voltage, V_{CTR} (Fig. 5). Negative feedback control of V_{CTR} adjusts the output voltage level to the desired optimum level.

Instead of frequency modulation, a block enabling scheme is another candidate approach to use the proposed design in a high performance setting with higher power demands. In this scheme, several independent voltage doubler blocks that share the same input and output ports are prepared, with each block capable of being turned on/off independently. According to the desired output power level, the number of turned-on blocks are adjusted to keep optimum output to input voltage ratio. This scheme does not require any delay elements in the oscillation paths, eliminating efficiency loss from delay elements. To match time constants for charging/discharging flying caps to the oscillation period, the ring structure can be lengthened (i.e., more stages) to match its open-loop clock signal path effort to each stage effort for charging/discharging a flying capacitor. In this scheme, the coarser granularity control relative to frequency modulation reduces efficiency when output power is lower than the optimal output power of a unit voltage doubler block. The block enabling scheme also requires more transistors and flying capacitors, increasing area. To focus on the ultra-low power design space, this work adopts the frequency modulation scheme.

C. Circuit Implementation

Fig. 5 shows the detailed implementation of the voltage doubler with frequency modulation. To modulate oscillation frequency, delay blocks are inserted in the oscillation paths. As shown in Fig. 6, a delay block consists of two coupled leakage-based delay elements [1] and a pass transistor T_P controlled by

V_{CTR}. When the inputs H_I and L_I of a stage switch from high to low, output nodes H_{OD} and L_{OD} (driven low) become isolated. T_P then provides a leakage path from L_O to L_{OD} that slowly raises L_{OD} and, through C_C, also H_{OD}. Back-to-back inverters in the delay element provide positive feedback and amplify the transition once it reaches V_{TH}, creating a sharp edge. This transition is then passed to the next stage. The opposite transition functions similarly.

A higher V_{CTR} allows T_P to provide more leakage, reducing the delay and speeding the oscillation. The leakage through T_P can be adjusted to any amount between its on and off currents, offering a very wide range of delay controllability. Additionally, due to the output isolation, the structure can produce very long, synchronized delays while the coupled positive feedback creates a sharp edge that limits short-circuit current and contention loss, enabling ultra-low power operation with very slow oscillation speed.

This structure also has an advantage for low-power self-startup and idle power minimization. It can oscillate even when the control voltage is 0, though very slowly, and therefore, is capable of self-startup. When the input voltage become available from the cold stage, V_{CTR} goes up from zero voltage, speeding up its oscillation until it reaches optimum. Start-up energy is reduced because its initial oscillation starts from the slowest speed, minimizing dynamic energy loss during start-up. When no input power is available from the power source, V_{IN} always becomes lower than V_{DIV}, pulling down the control voltage V_{CTR} to its lowest possible value. This automatically minimizes the idle power consumption.

V_{CTR} is adjusted through negative feedback. A clocked comparator, operating at a fraction of the internal oscillator frequency, takes in a divided form of the output voltage ($V_{\text{DIV}} = V_{\text{OUT}}/R_{\text{DIV\_DESIRED}}$) and the input voltage V_{IN}. A charge pump then takes in the corresponding pull-up/pull-down signals and adjusts the delay tuning voltage V_{CTR} as needed to either speed or slow the oscillation. As shown in Fig. 7, the voltage divider is implemented with a combination of a diode stack and a capacitive divider, to provide both fast response and good low-frequency behavior. In the charge pump (Fig. 7, right), two input inverter chains with small capacitive loads, C_{STEP}, determine the amount of charge transfer per cycle to be similar to
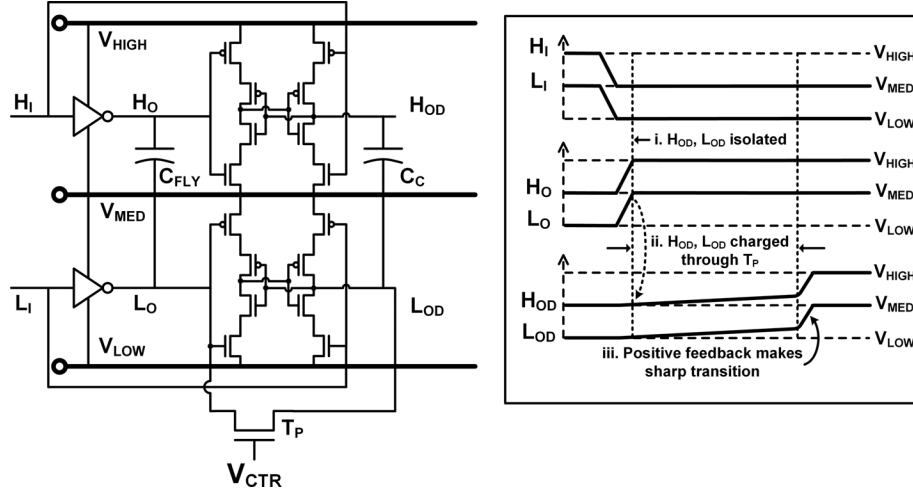
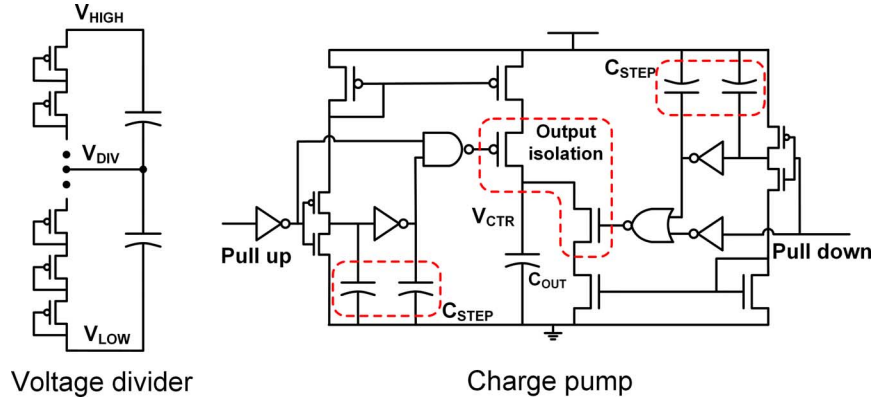Fig. 6. Detailed implementation (left) and timing diagram (right) of the delay block.

Fig. 7. Detailed implementation of the voltage divider (left) and the charge pump (right) from Fig. 4.

$VDD \times C_{STEP}$. Each chain also generates a short pulse at an output isolation transistor, turning it on briefly and only while the mirrored current flows through. The isolation transistors are turned off otherwise and help sustain the output voltage more than 1000 times longer in simulation than without isolation, even when clock frequency is as low as a few Hz.

III. ENERGY HARVESTER

A. Overall Structure

Fig. 8 shows the block diagram of the complete harvesting system, consisting of four stages of cascaded voltage doublers, a negative voltage generator, and circuits for conversion ratio control. A negative voltage is used to boost overall conversion ratio over $16\times$ and to power control circuits. The negative voltage generator is implemented by connecting V_{HIGH} and V_{MED} of the doubler to V_{IN} and ground, respectively, resulting in $V_{NEG} \approx -V_{IN}$ at the V_{LOW} port of the doubler. The target R_{DIV} of each voltage doubler is adjusted for its optimal operation.

To facilitate energy harvesting from a low voltage source (e.g., a photovoltaic cell under low light), the first stage and negative voltage generator use low V_{TH} (~ 300 mV) devices for their flying cap drivers. Bootstrapping is also used with these
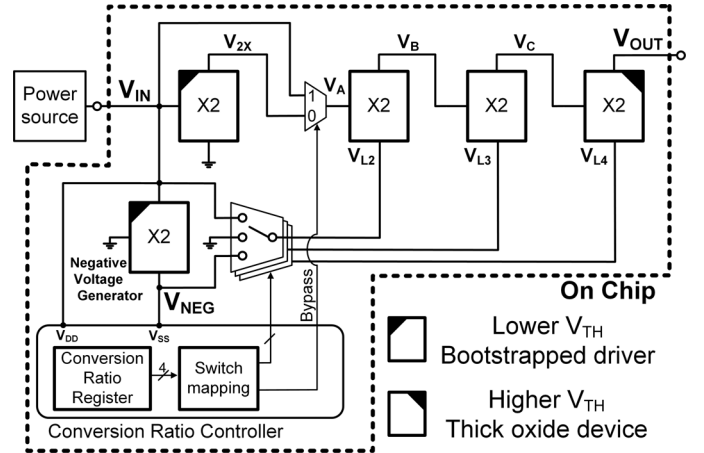

Fig. 8. Overall energy harvester architecture.

low V_{TH} switches, as shown in Fig. 9, to improve I_{ON}/I_{OFF} ratio at low input voltages. To ensure the bootstrapped signal does not decay in a clock cycle, every transistor in the bootstrap circuit uses a regular threshold voltage. For robust bootstrapping with a fast oscillation frequency, a reset switch for each bootstrap capacitor is driven by the output Φ_I, which has an increased voltage swing. To eliminate the short-circuit path
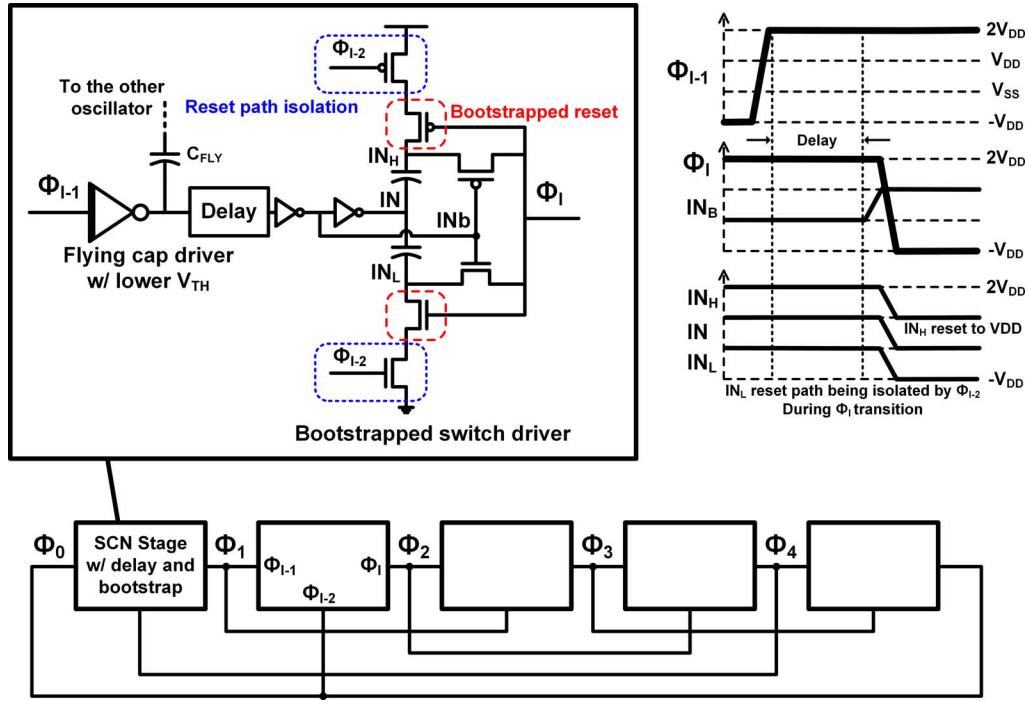
Fig. 9. 5-stage bootstrapped ring oscillator for voltage doublers with lower VTH switches and its timing diagram (top right).
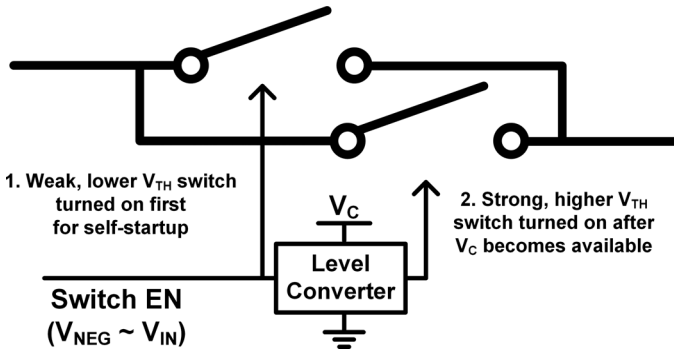

Fig. 10. Dual switching scheme for the harvester to reconfigure its conversion ratio while maintaining its capability of self-startup.
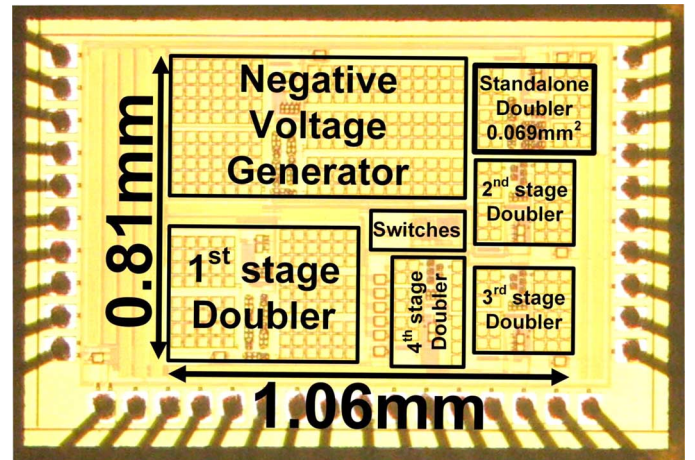

Fig. 11. Die micrograph of 0.18 μm CMOS test chip. Total flying cap sizes of the standalone voltage doubler and the harvester are 54 pF and 600 pF, respectively.

through the reset switches, an isolation transistor is inserted in each reset path, which is driven by Φ_{I-2}, the output signal of one of the previous bootstrap stages. Thick oxide I/O devices are used in the final doubler stage to protect the circuit from high voltages used to charge energy storage devices such as batteries or supercapacitors.

B. Conversion Ratio Modulation

The conversion ratio is adjusted by changing the number of cascaded stages. We propose an additional adjustment scheme where the V_{LOW} of a doubler is switched among V_{IN}, G_{ND}, and V_{NEG}, as shown in Fig. 8. If V_{LOW} is set to $-V_{\text{IN}}$, the voltage across the flying cap increases, resulting in $V_{\text{OUT}} = (V_{\text{MED}} + V_{\text{IN}}) \times 2 - V_{\text{IN}} = 2 \times V_{\text{MED}} + V_{\text{IN}}$. If V_{LOW} is set to ground for all 4 cascaded stages, the overall conversion ratio is $16 \times$. However, if the final stage V_{LOW} is set to V_{NEG}, the

overall conversion ratio increases by $1 \times$ to become $17 \times$. Similarly, setting the third stage V_{LOW} to V_{NEG} raises voltage V_C by $\sim V_{\text{IN}}$, resulting in an increase of overall conversion ratio by $2 \times$. On the other hand, setting V_{LOW} to V_{IN} decreases conversion ratio. In this way the conversion ratio is controlled in a binary manner as shown in Table I, generating any integer ratio from $9 \times$ to $23 \times$. By changing the conversion ratio, harvester input voltage V_{IN} can be adjusted to closely approximate the maximum-power point of the power source, thereby optimizing the power harvested from the source. By selecting the bottom voltage from among three choices rather than just two, the overall conversion ratio range is greater and also the voltage across each doubler can be chosen properly for best operation.

TABLE I
SWITCH MAPPING FOR HARVESTER'S OVERALL CONVERSION RATIO CONTROL FROM 9× TO 23×

| Ratio	9×	10×	11×	12×	13×	14×	15×	16×	17×	18×	19×	20×	21×	22×	23×
Bypass	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
V_{L2}	V_{NEG}	V_{NEG}	V_{NEG}	V_{NEG}	V_{NEG}	V_{NEG}	V_{NEG}	GND	V_{NEG}	V_{NEG}	V_{NEG}	V_{NEG}	V_{NEG}	V_{NEG}	V_{NEG}
V_{L3}	V_{IN}	V_{IN}	GND	GND	GND	V_{NEG}	V_{NEG}	GND	V_{IN}	V_{IN}	GND	GND	GND	V_{NEG}	V_{NEG}
V_{L4}	V_{IN}	GND	V_{IN}	GND	V_{NEG}	GND	V_{NEG}	GND	V_{IN}	GND	V_{IN}	GND	V_{NEG}	GND	V_{NEG}
V_A	1×	1×	1×	1×	1×	1×	1×	2×	2×	2×	2×	2×	2×	2×	2×
V_B	3×	3×	3×	3×	3×	3×	3×	4×	5×	5×	5×	5×	5×	5×	5×
V_C	5×	5×	6×	6×	6×	7×	7×	8×	9×	9×	10×	10×	10×	11×	11×
V_{OUT}	9×	10×	11×	12×	13×	14×	15×	16×	17×	18×	19×	20×	21×	22×	23×
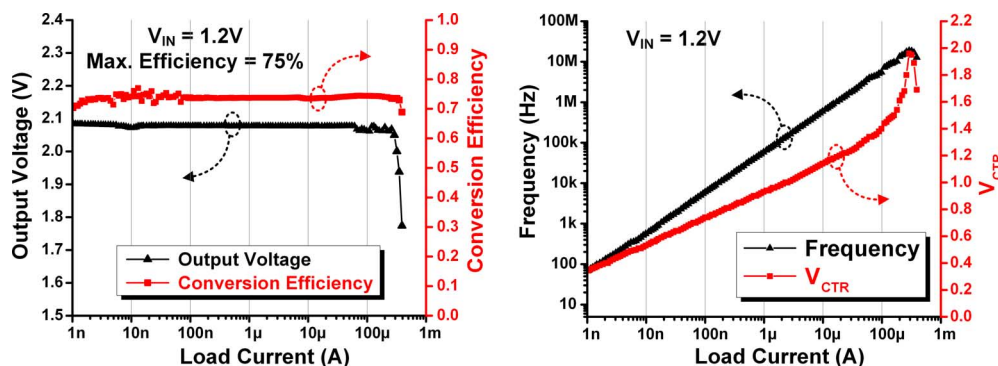
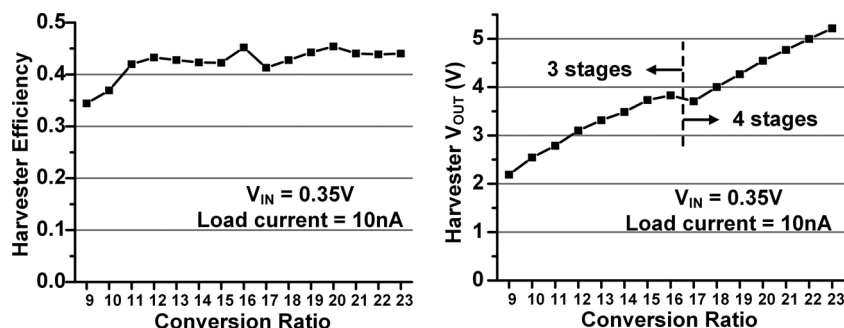Fig. 12.   Measured results of the voltage doubler.

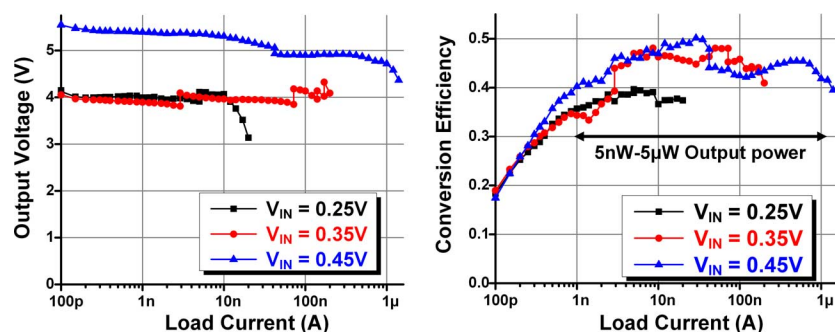Fig. 13.   Measured results of the harvester with different conversion ratios.

Fig. 14.   Measured results of the harvester at different V_{IN}.

For example, the switch mapping shown in Table I first seeks to develop a larger voltage across the second doubler since its use of standard V_{TH} transistors, coupled with its lower amplitude (relative to later stages) make its operation more challenging.

To enable cold start of the complete system, the control logic (including the conversion ratio register) operates between V_{NEG} and V_{IN} rails. Upon initial system startup, V_{NEG} and V_{2X} become available first, thus allowing the control logic to turn on
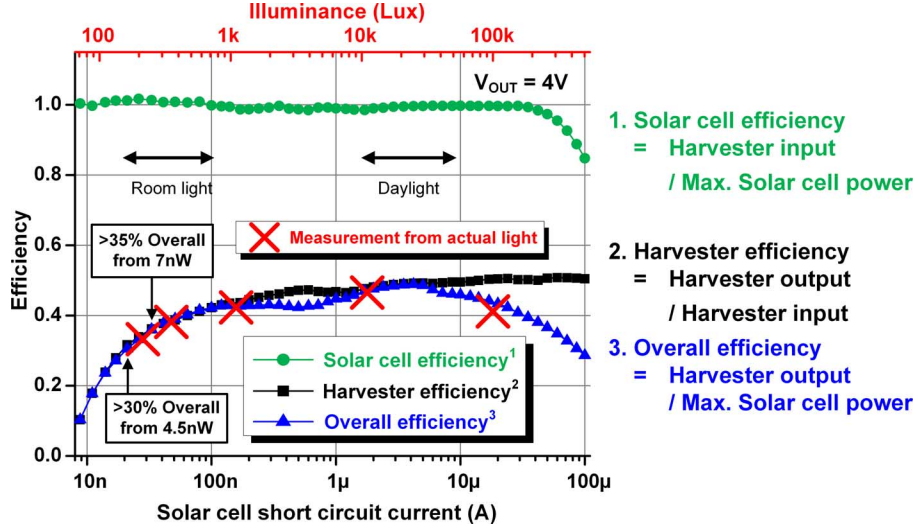
Fig. 15. Measured results of the harvester with a 0.84 mm² silicon solar cell at the input.
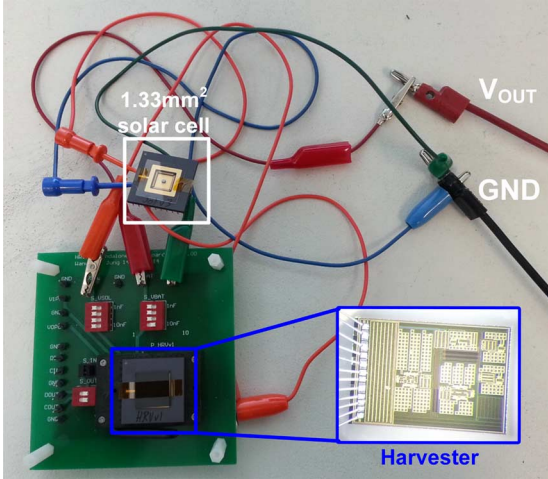

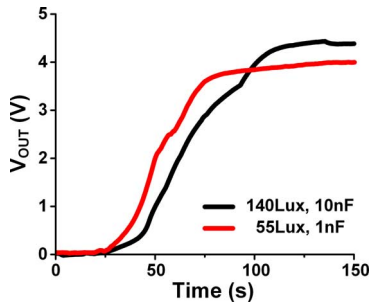Fig. 16. Measurement setup for the second harvester chip's self-starting behavior.

Fig. 17. Cold start behavior of the harvester powered by a 1.33 mm² solar cell. Output is connected to a capacitor. Light is turned on at some time between 0 ~ 20 s.

and configure the switches. As shown in Fig. 10, every switch is realized with a dual structure, one controlled with lower voltages for harvester self-startup, and the other controlled by a level-converted higher voltage to strongly turn on the switch for high output power levels. As each stage is powered up, its
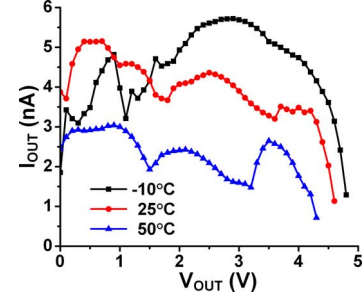

Fig. 18. Measured results of the harvester in different temperatures, with solar cell $I_{SC} = 180$ nA.

internal frequency modulation begins to control the frequency for optimum efficiency.

IV. Measured Results

The proposed voltage doubler (standalone) and energy harvester are fabricated in 0.18 μm CMOS (Fig. 11). The standalone voltage doubler uses bootstrapping to minimize its leakage. The division ratio of the output voltage divider in the frequency feedback control circuit (see Fig. 5), which is equivalent to the desired output to input voltage ratio ($R_{\text{DIV\_DESIRED}}$), is set to 1.73 for the standalone voltage doubler in all measurements. Fig. 12 shows a single doubler has >70% measured efficiency across 1 nA to 0.35 mA output current (>10^5 range) with low idle power consumption of 170 pW. Internal clock frequency is modulated to maintain constant R_{DIV} and is proportional to the load current until the clock period becomes too short relative to the time constant for charging/discharging a flying cap. As described in expression (13) in Section II-B, the conversion efficiency of the doubler is nearly flat within its operational range with an efficiency of roughly $R_{\text{DIV\_DESIRED}} - 1 = 73\%$.

Fig. 13 shows measured results of the harvester with different conversion ratios. Results show that a 0.35 V input can be converted to a 2.2 V–5.2 V voltage range with similar conversion
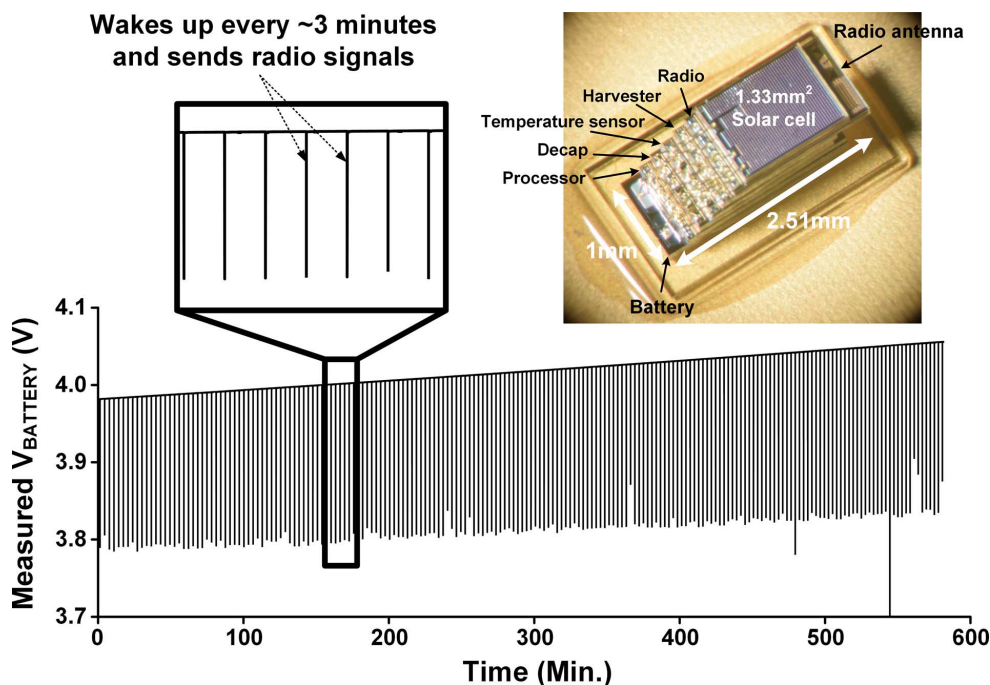
Fig. 19. Micrograph of a small M3 wireless sensor node system [2] with harvester (top right), and a graph of measured battery voltage (bottom) showing that its battery is continuously charged by the harvester during system operation.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON OF THE STANDALONE VOLTAGE DOUBLER

	[11]	[12]	[13]	This work (Doubler)
Technology	32nm CMOS	45nm SOI CMOS w/ trench cap	0.13μm CMOS	0.18μm CMOS
Architecture	Multi-phase voltage doubler	1:2 step-up/down converter	Multi-phase voltage doubler	Self-oscillating voltage doubler
Conversion ratio	1 : 2	2 : 1, 1 : 2	1 : 2	1 : 2
Tested input voltage	1V-1.2V	1V	1V-1.2V	1.2V
Frequency	250MHz-2GHz [1]	100MHz	N/R	70Hz-19MHz
Peak efficiency	64%	90%	82%	75%
Load range	0.4mA-9mA w/ >40% efficiency [1]	0.5mA-5mA w/ >80% efficiency [1]	0.15mA-2.2mA w/ >70% efficiency [1]	1nA-0.35mA w/ >70% efficiency
Load range in ratio	1 : 23 [1]	1 : 10 [1]	1 : 15 [1]	1 : 350,000
Area	0.0067mm²	0.0012mm²	2.25mm²	0.069mm²

N/R: Not reported
[1] Estimated number from the paper

efficiencies across settings. As conversion ratio goes up, output voltage level monotonically increases except for a transition from $16\times$ to $17\times$. At this transition, the number of cascaded stages increases from 3 to 4, thereby introducing another power loss at the first stage and lowering output voltage level. Fig. 14 shows measured results of the harvester at different V_{IN}. Conversion ratio is adjusted to maintain a similar V_{OUT} level. With $V_{IN} = 0.45$ V, corresponding to an outdoor condition, the harvester delivers 5 nW–5 μW output power with >40% efficiency and an idle power consumption < 3 nW. For $V_{IN} = 0.25$ V, corresponding to a solar cell under very low light, the harvester can take in between 10 nW and 120 nW to charge a ~ 4 V battery with >35% efficiency. For both V_{IN}, the harvester's output power range well covered expected solar cell power range.

Fig. 15 shows the measured results with a small silicon solar cell (0.84 mm²) at the input. In one test, the harvester is connected to the solar cell under various light conditions. These results are shown in the graph as the X-marked points. In the second test, the solar cell operation is emulated using an external current source in parallel with the solar cell, to perform a finer grain sweep of harvester performance. These two test results are very consistent as shown together in this graph, showing that the harvester can convert input power from the solar cell with up to 50% efficiency under a wide range of light condition, from dim room lighting to beyond outdoor daylight. Because of its low idle power consumption, the harvester shows >35% end-to-end efficiency even under a dim light of 260 lux, where the solar cell generates only 7 nW output power. By adjusting

TABLE III
PERFORMANCE SUMMARY AND COMPARISON OF THE HARVESTER

	[3]	[8]	[14]	This work (Harvester)
Technology	0.13μm CMOS	65nm CMOS	0.35μm CMOS	0.18μm CMOS
Architecture	Transformer self-startup	Integrated charge pump	Integrated charge pump	Cascade of integrated voltage doublers
Fully integrated	No (off-chip transformer)	Yes	Yes	Yes
Self-startup	Yes (min. 40mV)	Yes (min. 120mV)	N/R	Yes (min. 140mV)
Input voltage	40mV-300mV	0.12V-0.16V	0.6V-4V	0.14V-0.5V
Output voltage	2V	1V, 1.8V, 3V	N/R	2.2V-5.2V (0.35V VIN, 10nA I_{LOAD})
Peak efficiency	61% @ 0.3V V_{IN}	38.8% @ 0.12V V_{IN}	70% @ 2V V_{IN}	50% @ 0.45V V_{IN}
Output power range	N/R	1μW-3μW @ 0.12V V_{IN} [1] 2μW-7μW @ 0.14V V_{IN} [1] 3μW-10μW @ 0.16V V_{IN} [1] (w/ >15% efficiency) [1]	1μW-1mW (Only peak efficiency reported)	5nW-5μW w/ >40% efficiency
Idle power consumption	N/R	N/R	2μW @ 100μW input 7μW @ 1mW input	<3nW
Minimum input power	N/R	N/R	N/R	6nW for self-startup 1.7nW to sustain harvesting
Area	0.093mm^2	0.78mm^2	59mm^2	0.86mm^2

N/R: Not reported
[1] Estimated number from the paper

the conversion ratio the harvester can take in nearly 100% of the solar cell output power at its maximum power point for incident light up to 200 klux, covering almost all practical light conditions (Fig. 15, "Solar cell efficiency" curve).

A second chip is fabricated in 0.18 μm CMOS that includes the harvester with the same design specifications previously described but has interfaces compatible with the M^3 (Michigan Micro-Mote) sensor system [2]. This chip is tested with a solar cell of 1.33 mm^2 area to measure its self-startup characteristic (Fig. 16). As shown in Fig. 17, the harvester cold starts with 55 lux of light and a 5.2 nW power source and charges an output capacitance to 4 V, which is a voltage enough to charge a battery. Fig. 18 shows measured results in different temperatures, with solar cell short circuit current overridden to 180 nA to emulate room lighting. The results show the harvester's robust operation across $-10°C - 50°C$ temperature range.

This chip is integrated in a very small M^3 wireless sensor node system (Fig. 19, top right) with volume of approximately 1 mm^3 [2]. A graph at the bottom shows the system battery voltage during operation. As shown in the graph, the system periodically wakes up and sends a radio signal every $\sim$ 3 minutes. The positive slope in the battery voltage plot during sleep cycles show that the battery is being charged effectively by the proposed harvester. Tables II and III summarize the voltage doubler and harvester performance and compares to prior related work.
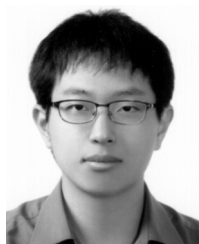
V. CONCLUSIONS

This paper presents an ultra-low power fully integrated energy harvester based on a novel SC voltage doubler structure.

Internalized clock generation and clock frequency modulation allow the doubler to operate across a wide load range ($> 10^5 \times$) with low idle power consumption of 170 pW. Four voltage doublers are cascaded to form an energy harvester, which can operate with a very limited power source of a few nWs. Overall harvester conversion ratio is configurable from $9 \times$ to $23 \times$ using bottom voltage switching, a negative voltage generator, and cascaded stage count, generating 2.2 V–5.2 V V_{OUT} from 0.35 V V_{IN}. Measured results with a small silicon solar cell (1.33 mm^2) show the harvester cold starts with 55 lux of light and a 5.2 nW power source. The harvester chip is integrated in an actual wireless sensor node system and demonstrates charging of the system battery during typical operation.
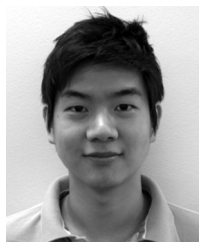
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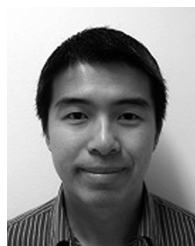
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