A 1.6nJ/bit, 19.9μA Peak Current Fully Integrated 2.5mm^2 Inductive Transceiver for Volume-Constrained Microsystems

Mohammad Hassan Ghaed, Skylar Skrzyniarz, David Blaauw, Dennis Sylvester

University of Michigan, Ann Arbor, MI 48109

Abstract — A 1.6nJ/bit inductive transceiver targeting volume-constrained microsystems with limited peak current is presented. The transceiver uses a protocol in which the external unit sends the same packet multiple times to shift the power consumption burden to the external TRX unit and relax jitter requirements on the mm-scale receiver. The transceiver receives data from a 2W external unit at 1m distance using a dual-coil LNA design and fast-startup front-end. The 2.5mm^2 transceiver draws 19.9μA from a 2mm^2 thin-film battery at 40.7kbps.

I. INTRODUCTION

Short communication range wireless sensor nodes are in great demand for biomedical [1,2] and other emerging applications. A differentiating feature of such nodes is their highly miniaturized form factor [3], often in the mm range. As a result, the substantial work in low power RFID is incompatible with this new class of devices due to the large antennas of RFID card-type devices [4]. Present near-field solutions require large peak currents that are infeasible in such systems [5]. Very small (1-10mm^2) thin-film batteries offer the only reliable power source for such systems (Fig. 1). While their 10-50mJ capacities are sufficient for the transmission of several Mb of data between battery recharges

(at ~1nJ/bit), their peak output current of 10-50μA is a key challenge for RF blocks (mA range). Therefore, these blocks must operate using a capacitive charge reservoir (nF range) that is recharged between radio transmissions. However, ms-scale recharge times reduce bit rate and place tight requirements on timing reference jitter in order to maintain synchronization throughout the longer communication process. This in turn increases timing reference power (typically integrated on-chip in such systems), which can come to dominate overall power consumption. Further, receiver start-up time/energy becomes critical given the limited charge reservoir.

To address these issues we propose a 2.5mm^2 near-field transceiver with integrated coils that uses a novel analog front-end and transmission protocol to relax synchronization requirements on the heavily constrained receive side. It uses a 14.3nF charge reservoir and draws 19.9μA peak current. The front-end uses a new fast-startup scheme to minimize start-up overhead and a new dual-coil LNA structure to maximize inductive coupling. The transceiver consumes 42.7nA during the heavily duty cycled monitoring mode and 19.9μA at 40.7kbps during active mode. Energy is drawn from a custom 2mm^2 3.6V thin-film battery that is suitable for 3D stacking with the radio die.

II. TRANSCEIVER DESIGN

The proposed CMOS transceiver consists of an asynchronous controller, a receiver front-end and decoder, and an inductive transmitter (Fig. 1). To address the peak output current limitations of highly integrated microsystems, the transceiver uses a new half-duplex protocol that does not require accurate timing to receive data from an external unit (Fig. 2). To initiate data transfer, the external unit sends out a beacon for ~100ms, after which it ceases transmitting and listens for acknowledgement (Fig. 2). The receiver is periodically awoken by a pW-level leakage-based oscillator [6]. Upon activation via beaconing by the external unit, the receiver responds (after a delay T_{wakeup}) by sending an acknowledgement via its on-chip transmitter. Next, the external unit begins data transmission by continuously sending a payload packet (header + data) (Fig. 2). After recharging its charge reservoir, the receiver wakes up briefly to capture data. Since the wakeup window will be arbitrarily aligned to the continuously transmitted Manchester-encoded
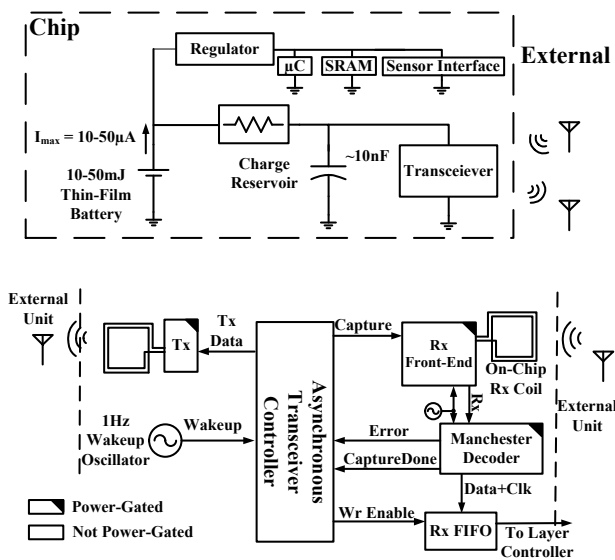

Figure 1. The most practical power source for ultra-small wireless integrated microsystems is a 10-50mJ thin-film battery with limited peak current (top). Block diagram of the proposed transceiver (bottom).
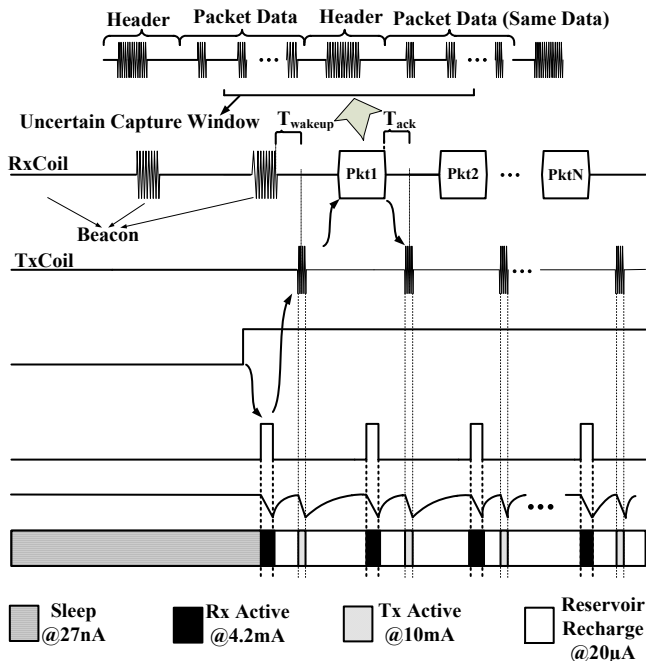
Figure 2. The new transceiver protocol shifts link power and complexity to the external side, which has much less stringent energy constraints.

data, the decoder must locate the header to correctly rotate the captured window.

By transmitting the same data many times from the external side, uncertainty in the capture window location becomes acceptable (Fig. 2). This greatly relaxes constraints on clock jitter in the chip at the cost of increased power consumption in the external unit (which is typically not constrained). After receiving a packet, the receiver requests the next packet by sending a signal after a digitally tunable delay, T_{ack}, allowing time for the charge reservoir to recharge. If interference or noise cause the received bitstream to differ from the expected pattern, an acknowledgement is sent with a delay of $2T_{ack}$, signaling the external unit to retry the same packet. Data reception continues until the on-chip FIFO is full. Protocol timing is managed by the asynchronous controller (Fig. 1), which is implemented using custom low-leakage
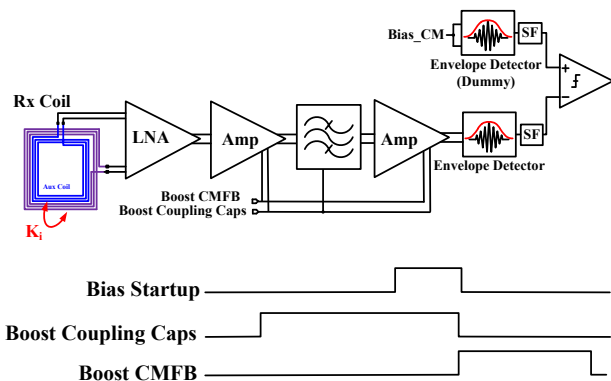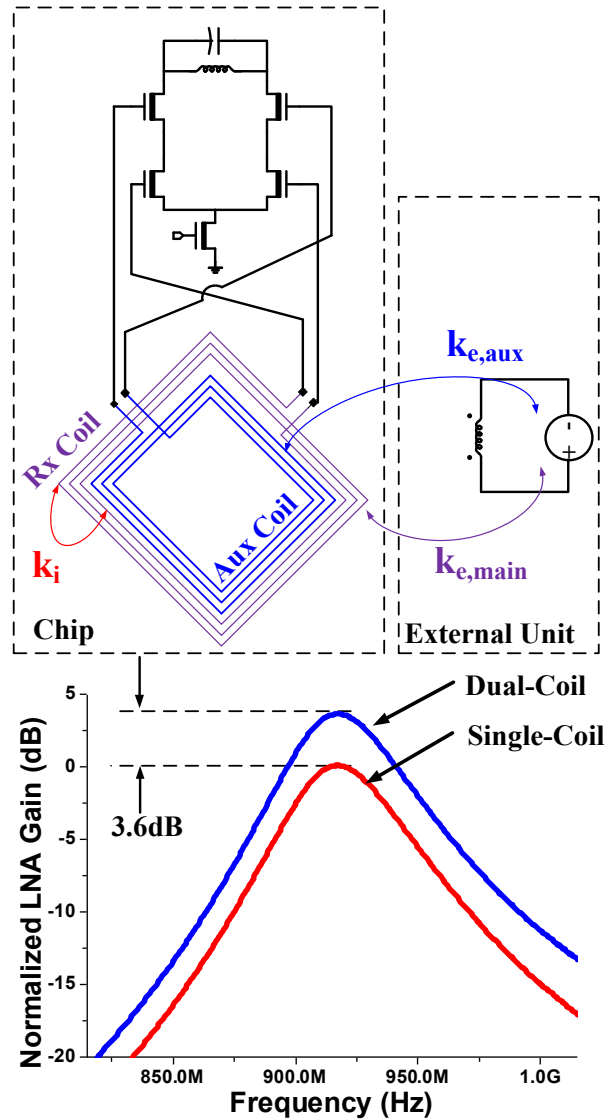

Figure 3. RF front-end block diagram.

Figure 4. LNA schematic and simulated performance compared to a conventional single coil design.

high-Vth standard cells to limit total monitoring mode current to 42.7nA.

Fig. 3 shows the receiver front-end block diagram. A fully differential implementation maximizes immunity to interference and supply variation. It consists of a cascode LNA using a 2-coil configuration, two amplifiers, a bandpass filter, two envelope detectors, and a clocked comparator preceded by a source follower. The dummy envelope detector experiences the same interference, supply, and process variation as the main envelope detector, thus improving power-supply rejection and variation immunity. The 10μA source follower attenuates clock kick-back from the comparator to the high-Z envelope detector output by 21dB. When the front-end turns on (power gating released), startup switches short both plates of AC coupling capacitors to their steady-state values during the period shown in Fig. 3 ("Boost Coupling Caps" high). After this, the "Bias Startup" signal
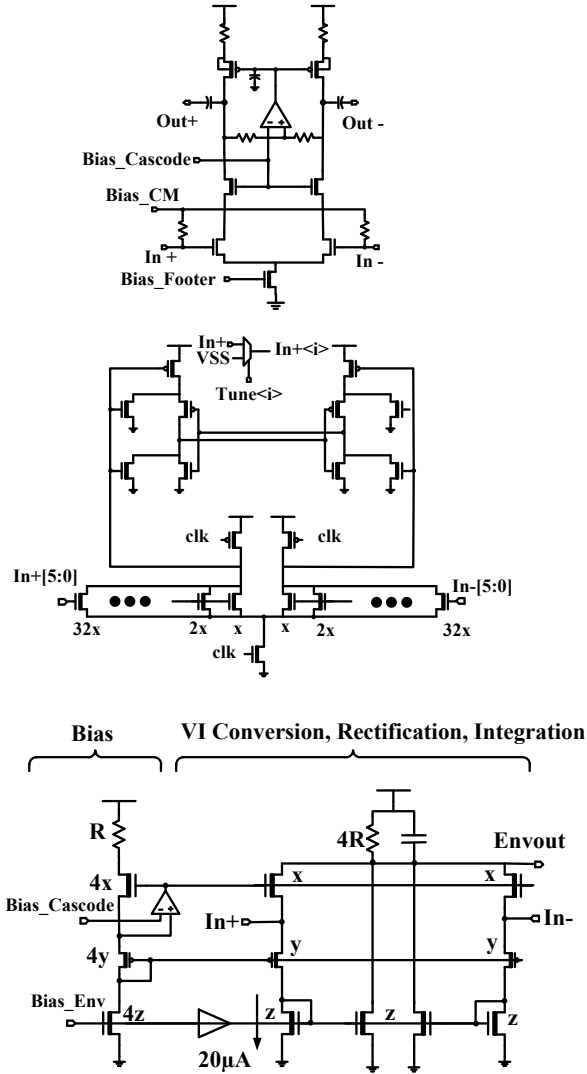
Figure 5. Schematics for the amplifier, comparator, and envelope detector. The comparator adjusts the strength of each side based on digital tuning bits from the controller.
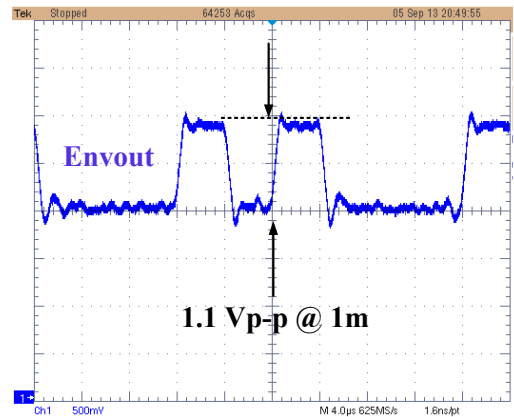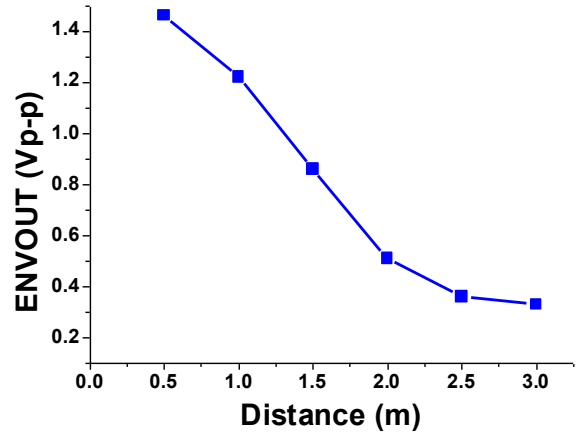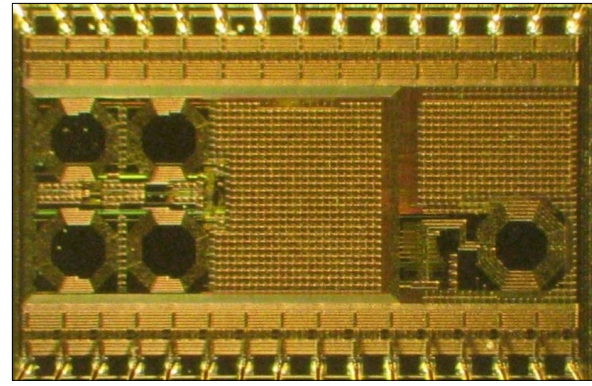

Figure 6. Measurement results. Chip micrograph (top); Received peak-to-peak output as a function of distance (middle); Sample oscilloscope shot of envelope detector output (bottom).

kick-starts the bias circuitry to prevent unnecessary power consumption when front-end voltages stabilize. Finally, all common-mode feedbacks (CMFB) are boosted by injecting additional current into the error amplifiers until floating nodes approach their final values. Since transistors are not yet biased when CMFB boosting is asserted, instabilities caused by extra loop gain in CMFB are avoided. Using these techniques, receiver front-end start up time is reduced from 179µs to 0.45µs, rendering start-up energy less than 3% of total energy consumption for each received packet.

Unlike conventional antenna-driven LNAs, the inductive receiver uses an on-chip coil to couple to the external unit. Introducing a resistive input impedance by inductive degeneration would reduce the quality factor of our critical receive coil, degrading receive distance by 20%. To maximize mutual coupling between the on-chip coil and the external unit,

the inductor magnetic moment must be increased. Two options are to increase area and/or the number of turns, however, the correspondingly lower self-resonance-frequency (SRF) would cause the larger inductor to operate as a capacitor at the frequency of interest. Based on 3D EM simulations, 4-turn inductors are the largest possible that still enable 915MHz operation. Therefore we introduce a second 4-turn coil (Fig. 4). This coil couples to the external coil in the same way as the main coil and is connected to the LNA cascode inputs ($k_{e,main}$ and $k_{e,aux}$ in Fig. 4). When the auxiliary coil resonates, this approach provides extra feedback to the input by coupling to the main coil via k_i (≈ 0.6), enabling a 3.6dB frequency-selective gain improvement, which translates to 22% added range (Fig. 4).
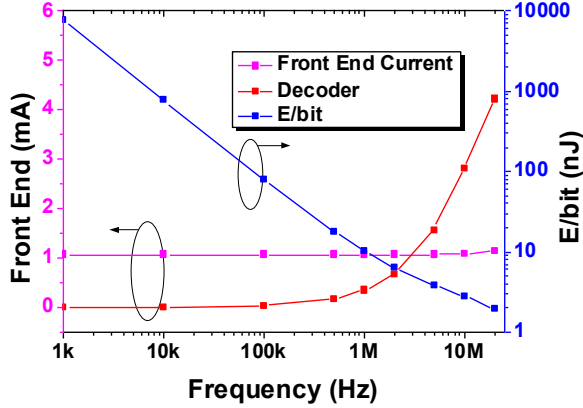
Figure 7. Measured active power and energy per bit (top); Oscilloscope shot of system wakeup scheme (bottom).

Fig. 5 shows schematics for the amplifiers, comparator, and envelope detector. The amplifier with CMFB provides 20dB of gain at 915MHz with 100µA of current. Resistors are used instead of active loads to increase output resistance with only 250mV loss of headroom. This reduces the number of required bias voltages, enabling lower Vdd operation down to 3.1V. Comparator offset voltages as large as ±3V are possible using digital tuning bits to trade off distance for better noise immunity. Since the front-end is directly supplied by the 3.6V battery, we can use an efficient envelope detector architecture with three stacked transistors. The four rectifying branches of the envelope detector are biased at 20nA to minimize power.

III. MEASUREMENT RESULTS

The transceiver is fabricated in 0.18µm CMOS and occupies 2.5mm^2 core area (Fig. 6). It consumes 71.6µW of active power at 40.7kbps and reliably receives data from a 2W source positioned 1m away. The envelope detector output amplitude plots (Fig. 6, middle) show that the front-end chain can easily amplify signals at distances up to 1m. Fig. 7 (bottom) provides an oscilloscope shot of the Wakeup−Capture−CaptureDone sequence. Examining the active power breakdown in Fig. 7, energy/bit becomes dominated by digital power at high bitrates, as expected. Table I shows a comparison with recent inductive transceivers. The

TABLE I
COMPARISON WITH PRIOR ART IN MINIATURIZED INDUCTIVE TRANSCEIVERS.

	[7]	[8]	[1]	[9]	This Work
Modulation	DPSK	PSK	FSK	OOK	OOK
Carrier Freq.	20 MHz	256 KHz	915/433MHz	67.5 MHz	915 MHz
Energy per Bit	3.1nJ Rx No Tx	N/A	Passive Rx 4.7nJ Tx	0.29nJ Rx 0.34nJ Tx	1.6nJ Rx 4.7nJ Tx
Active Power	6.2 mW @ 2Mbps	1.7* µW	N/A	3 mW @ 10.2Mbps	71.6 µW @ 40.7kbps
Rx Coil Location	Off-Chip	Off-Chip	On-Chip	Off-Chip	On-Chip
Rx Coil Max Dimension	22mm	20mm	0.5mm	15mm	1.7mm
Technology	0.35 µm	0.35 µm	0.18 µm	0.5 µm	0.18 µm
Receive Distance	1.5 cm	1 cm	0.4 cm	1 cm	100 cm
Monitoring Mode Power	N/A	N/A	7 nW	N/A	153 nW

transceiver is the first fully integrated radio to achieve 1m range while operating from a battery of mm-scale.

REFERENCES

[1] G. Chen *et al*., "A cubic-millimeter energy-autonomous wireless intraocular pressure monitor," *IEEE International Solid-State Circuits Conference*, 2011.

[2] X. Meng *et al*., "Implantable wireless devices for monitoring of intraocular pressure," *IEEE International Symposium on Consumer Electronics*, 2012.

[3] I. Chen *et al*., "personalized biomedical devices and systems for healthcare applications," *Frontiers of Mechanical Engineering*, Vol. 6, No. 1, pp. 3-12, 2011.

[4] D. Yeager *et al*., "A 9.2µA gen 2 compatible UHF RFID sensing tag with -12dBm sensitivity and 1.25µVrms input-referred noise floor," *IEEE International Solid-State Circuits Conference*, 2010.

[5] Y. Darwhelkar *et al*., "A 45nm CMOS near-field communication radio with 0.15 a/m rx sensitivity and 4mA current consumption in card emulation mode," *IEEE International Solid-State Circuits Conference*, 2013.

[6] M. Wieckowski *et al*., "A hybrid DC-DC converter for nanoampere sub-1V implantable applications," *IEEE Symposium on VLSI Circuits*, 2009.

[7] M. Zhou *et al*., "A non-coherent DPSK data receiver with interference cancellation for dual-band transcutaneous telemetries," *IEEE International Solid-State Circuits Conference*, 2008.

[8] S. Lee *et al*., "A programmable implantable microstimulator SOC with wireless telemetry," *IEEE International Solid-State Circuits Conference*, 2011.

[9] F. Inanlou *et al*., "A 10.2 Mbps pulse harmonic modulation based transceiver for implantable medical devices," *IEEE International Solid-State Circuits Conference*, 2011.