# FOCUS: Key Building Blocks and Integration Strategy of A Miniaturized Wireless Sensor Node

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***Abstract*—Recently, miniaturized sensor nodes have been widely studied for various applications. The advances in these studies have greatly reduced energy consumption, leading to a mm$^3$-scale system and optimized circuit performance well suited for sensor node applications. This paper focuses on the ultra-low power circuit techniques on the major building blocks and demonstrates integration strategy of an image sensing platform.**

## I. INTRODUCTION

Smart sensor nodes have been a popular research topic in recent decades, as the demand for collecting and processing environmental data has grown. Consequently, promising research outcomes have been published in various areas of medical care [1], environmental monitoring [2] and surveillance [3]. Such wireless sensor nodes (WSNs) require new circuit techniques as they are placed in a very distinctive operating environment with specialized purposes compared to the conventional applications. Form factor of the system is one of the most challenging constraints in designing a WSN. For instance, medical implants or smart dust usually require mm$^3$-scale size, which makes it very difficult to achieve a viable power budget.

Fig. 1. shows the lifetime of a system according to battery capacity and power budget. A 0.92mm$^3$ Li thin-film battery, for example, has nearly a million times smaller energy capacity compared to an Alkaline AA battery, which forces the circuit design regime to move from milli-watt to nano-watt level.

Energy harvesters using a solar cell, RF-DC converter, or piezoelectric component can alleviate this problem. Typically, an energy harvester transforms energy from external sources such as light, electromagnetic waves, or mechanical vibration to a voltage or current, which in turn is converted to a certain voltage level to charge a rechargeable battery while the rest of the system is in sleep mode to save power consumption. Then, the system becomes active for a minimum required period of time and goes back to sleep mode again. In this system scenario, it is critical to design an efficient DC-DC converter to minimize energy loss during voltage conversion. In addition, a highly accurate timer is also required to ensure the synchronization of nodes for radio transmission and to maintain a constant system wakeup period. Simultaneously, circuit techniques to reduce the power consumption in an active mode are also essential not only to increase the activity rate but also to extend the battery lifetime which degrades by repeated charging and discharging operation.

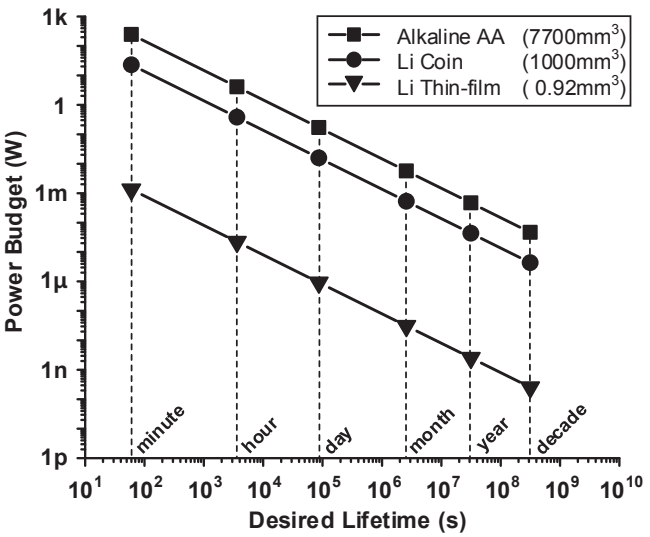


Fig. 1. Lifetime of various batteries according to the system power consumption

In this paper, we review various circuit techniques to reduce the power consumption of building blocks of a WSN while maintaining or improving the key performance metrics. We then review an imaging system to discuss integration strategies and issues.

## II. BUILDING BLOCKS

### A. Frequency Generation

Accurate on-chip frequency generation is critical for WSN applications. A WSN usually sleeps for a long time to save or harvest energy and wakes up to process the data and communicate with each other. The timing mismatch among the sensor nodes causes some of the sensor nodes to waste energy while waiting for the other sensors to wake up. The wasted energy can even exceed the energy used to process the data if their operation is heavily duty cycled. Furthermore, the size constraint makes it difficult to exploit the low noise characteristic of a crystal oscillator in WSN application, so more emphasis is needed to accurately stabilize on-chip clock generation. On the other hand, very low power consumption is also required for such clock generators because the power consumption in the sleep mode can be dominated by the always-on oscillator. In summary, key design goals for an

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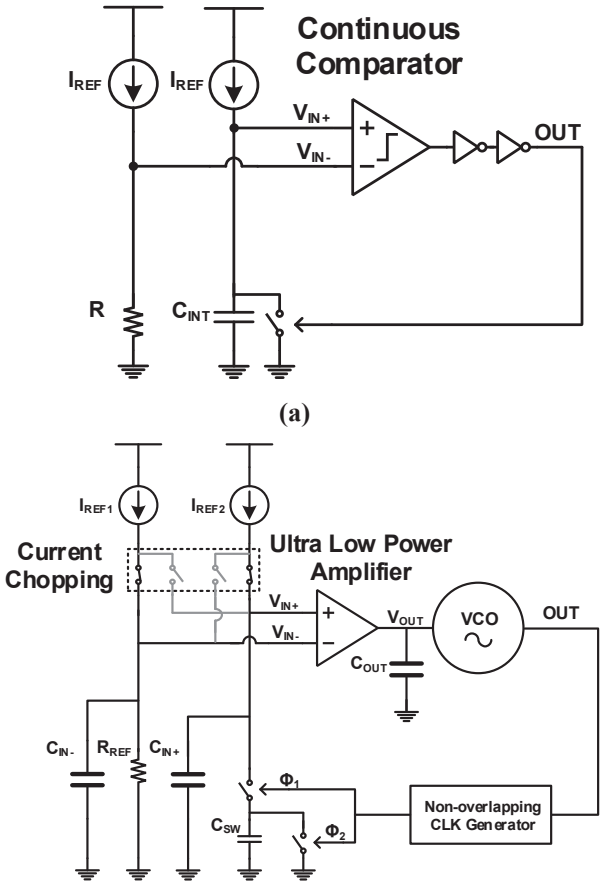


Fig. 2. Circuit schematic of (a) Conventional relaxation oscillator and (b) resistive frequency locking oscillator.

oscillators include ultra-low power while maintaining good frequency stability.

The conventional relaxation oscillator, shown in Fig. 2(a) uses current sources, $I_{REF}$, to charge the integration capacitor, $C_{INT}$, and resets the charge once the voltage on the capacitor, $V_{IN+}$, reaches a reference. In this structure, the clock period depends not only on R-C delay, which can be made insensitive to temperature fairly easily, but also on comparator and buffer delays, which are known to be affected by temperature variation. One simple solution is to increase their speed to make them negligible compared to overall period. However, this incurs high power consumption which makes it not suitable for WSN applications.

[4] proposes an on-chip oscillator using a resistive frequency locking technique that breaks away from the traditional topology by removing the comparator from the oscillation loop. The block diagram of the resistive frequency locking loop is shown in Fig. 2(b). A current, $I_{REF1}$, is injected into a temperature compensated resistor, $R_{REF}$, and develops a reference voltage, $V_{IN-} = I_{REF} \times R_{REF}$. An amplifier forces the voltage on the switched capacitor, $V_{IN+}$, to match $V_{IN-}$ by tuning the VCO frequency, $F_{OUT}$. As a result, $F_{OUT}$ is locked to a frequency which matches the equivalent resistance of a

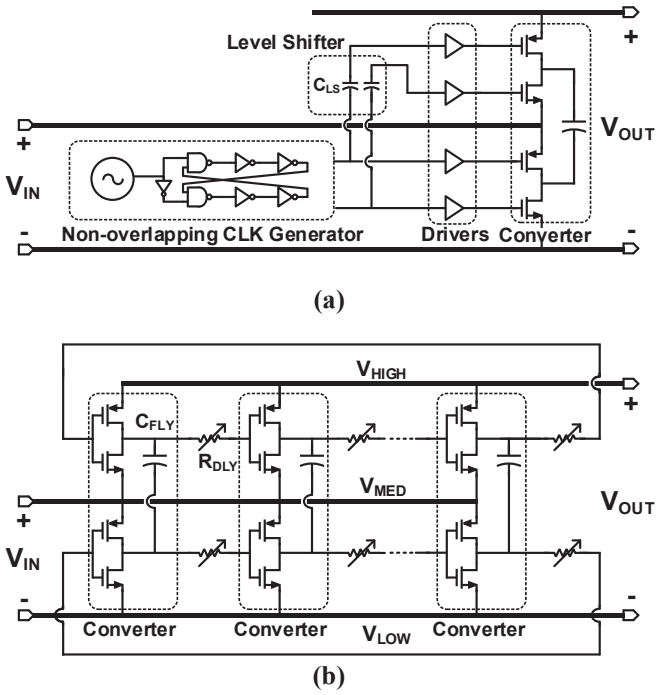


Fig. 3. (a) Conventional switch capacitor based voltage doubler and (b) self-oscillating voltage doubler.

switched capacitor ($1/(C_{SW}F_{OUT})$) to $R_{REF}$, thereby defined as the following equation.

$$F_{OUT} = \frac{1}{R_{REF}C_{SW}} \quad (1)$$

Since $R_{REF}$ is temperature compensated and $C_{SW}$ is a metal-insulator-metal (MIM) capacitor that is inherently temperature insensitive, a highly temperature-stable frequency is generated.

The currents injected into the resistor, $I_{REF1}$, and the switched capacitor, $I_{REF2}$, alternate their connections to the amplifier inputs, thus effective current at each input is the average of $I_{REF1}$ and $I_{REF2}$. In this way, the temperature instability caused by the temperature dependent current mismatch is eliminated. The amplifier that provides frequency locking tracks the impact of temperature changes on the VCO. As temperature change is slow, the amplifier can be low-bandwidth and ultra-low power.

A prototype of the oscillator consumes 99nW with temperature coefficient of 27.4ppm/°C and voltage sensitivity of 0.5%/V over the temperature range of -40 to 80°C. The proposed work shows good long-term frequency stability of less than 7 ppm.

### *B. Energy Harvester*

Power management unit (PMU) is also a key building block. A solar cell is widely used to harvest energy and a DC-DC converter can be used to charge a battery or regulate supply voltage levels of the system. Fig. 3(a) shows a conventional

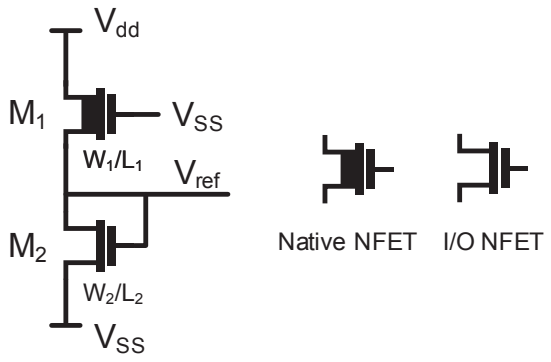


Fig. 4. Schematic of 2T voltage reference.

structure of a voltage doubler. A non-overlapping clock generator, level-shifter, and drivers are essential to control a switched capacitor but causes additional power overhead.

The energy harvester in [5] removes such overhead by implementing a self-oscillating voltage doubler as shown in Fig. 3(b). The switched capacitors are configured in a ring fashion to enable self-oscillation. By configuring the top and bottom ring oscillators to run between $V_{HIGH}$-$V_{MID}$ and $V_{MID}$-$V_{LOW}$, respectively, the phase mismatch between the two becomes negligible, enabling the flying capacitor, $C_{FLY}$, to transfer charge from the lower to upper voltage rail without contention loss. As this structure is naturally multi-phased, it results in low ripple at $V_{OUT}$. Conduction and switching losses are balanced by dynamically adjusting the delay element, $R_{DLY}$, based on the ratio between the output and input voltages. This helps to achieve optimum efficiency over a wide range of load currents. A complete harvesting system is composed of multiple voltage doublers cascaded with each other so that conversion ratio can be adjusted by reconfiguring the number of cascaded stages or by modulating the bottom voltage, $V_{LOW}$, of each voltage doubler. As a result, the proposed harvester generates a wide range of conversion ratios: from 9 to 23.

The harvester output power ranges from 5nW to 5μW with more than 40% efficiency while dissipating less than 3nW of idle power when $V_{IN}$ is 450mV. More than 35% efficiency is achieved while charging a 4V battery when a millimeter-scale solar cell is used at 260lux indoor light condition.

### C. Reference Generation

Voltage and current references are widely used for many analog circuits. However, conventional design techniques like bandgap or beta-multiplier do not meet the demanding low power consumption, small design area, and low functional supply voltage requirements of WSN applications [6][7].

[6] proposes a pico-watt temperature compensated voltage reference operating at 0.5V. The proposed scheme uses two transistors, $M_1$ and $M_2$, with different threshold voltages as shown in Fig. 4. By equalizing the subthreshold current of the two transistors, the output voltage ($V_{ref}$) can be expressed as,

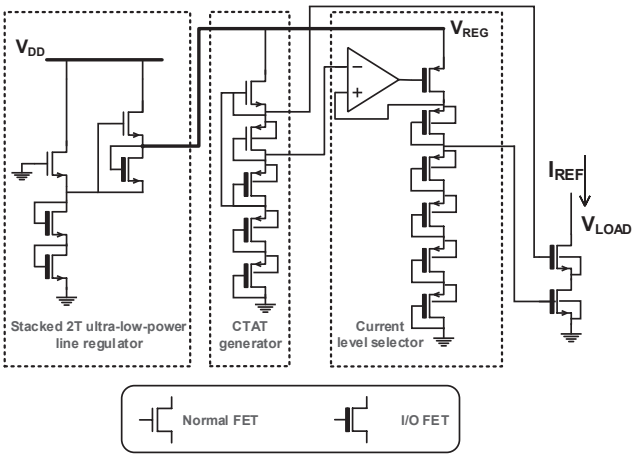


Fig. 5. Schematic of 2T voltage reference.

$$V_{ref} = \frac{m_1 m_2}{m_1 + m_2}(V_{th2} - V_{th1}) + \frac{m_1 m_2}{m_1 + m_2} V_T \ln\left(\frac{\mu_1 C_{ox1} W_1 L_1}{\mu_2 C_{ox2} W_2 L_2}\right) \quad (2)$$

where $m$, $V_{th}$, $\mu$, $C_{ox}$, $W$, and $L$ are subthreshold slop, mobility, oxide unit capacitance, transistor width and transistor length, respectively. As shown in (2), both the first and second terms are either proportional or complementary to absolute temperature. By selecting appropriate width and length of the two devices, the temperature dependence of the two terms can be cancelled out and achieve temperature insensitivity.

The measurement results of the prototype chips show temperature coefficient of 16.9 ppm/°C and line sensitivity of 0.033%/V.

A pico-watt temperature compensated current reference is proposed in [7]. The area is reduced by adopting resistor-less approach as shown Fig. 5. The CTAT generates a gate voltage of a subthreshold transistor to compensate for the temperature coefficient of the threshold voltage. The supply voltage of the CTAT is connected to the aforementioned 2T voltage reference and the output stage is cascoded to improve the line and load sensitivity, respectively.

The proposed current reference generates 20pA current while consuming 23pW with a temperature coefficient of 780ppm/°C and line sensitivity of 0.58%/V.

### D. Logic Gate

Leakage current of logic gates composing the micro-processor sets the lower bound of power consumption in active mode. Therefore, it is preferred to have a low leakage logic gate specialized for WSN applications.

[8] proposes a dynamic leakage-suppression logic (DLS) which is used to implement a sub-nW Cortex-M0+ processor operating under a wide supply range: from 0.16 to 1.15V. Fig. 6. explains the operation of the proposed gate. The bottom PMOS, $M_{PB}$, and the top NMOS, $M_{NT}$, are added to the ground and power paths of a conventional inverter. In this

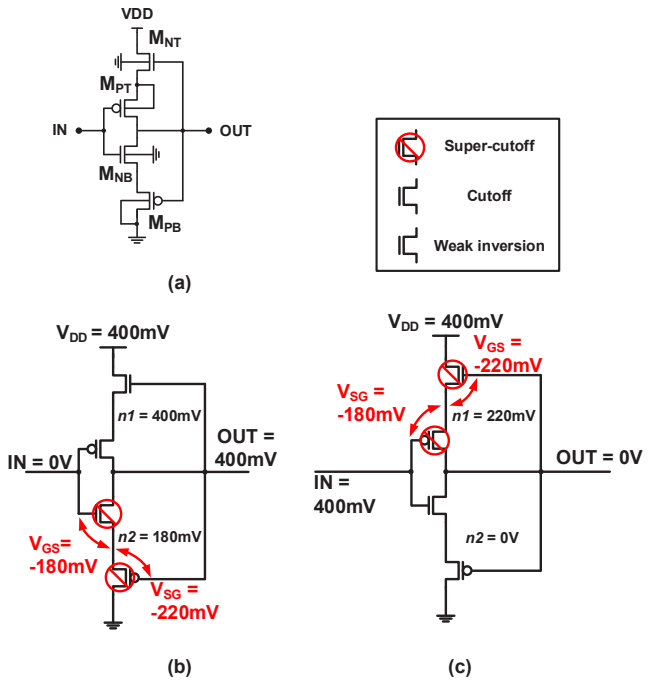


Fig. 6. (a) Schematic of a dynamic leakage-suppression logic and its steady state transistor states (b) when the input is 0 and (c) when the input is VDD.

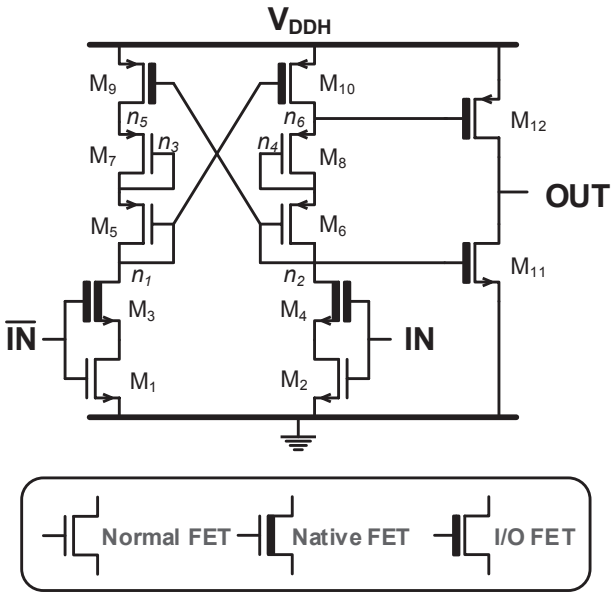


Fig. 7. Circuit diagram of Split-controlled Level Converter (SLC).

configuration, all the transistors on the leakage paths are in a super-cutoff state after the output is stabilized. For instance, when the input and output are 0 and VDD, respectively, $V_{SG}$ of $M_{PB}$ becomes negative which sets it to be in a super-cutoff state. The bottom NMOS transistor, $M_{NB}$, is also in a super-cutoff state because the gate voltage is 0 while the source voltage is higher. Similarly, both $M_{NT}$ and $M_{PT}$ are in a super-cutoff state when the input and output are VDD and 0, respectively. Consequently, the leakage current of the proposed device is 320 times smaller than a standard low-leakage stacked inverter.

A prototype design of Cortex-M0+ processor in a 180nm CMOS technology consumes 0.295pW under 550mV supply voltage, which even ensures its functionality with a 0.09mm$^2$ solar cell at a room lighting condition of 240lux.

### E. Level Shifter

In order to cope with challenging power consumption constraints, various levels of supply voltage can be used for different building blocks. Therefore, low power voltage level shifters are also required.

Conventional level shifters are often based on differential cascode voltage switch (DCVS) logic. In this structure, bottom pull-down devices are highly susceptible to process and supply variations because they operate in a subthreshold region, which leads to the possibility of functional failure.

Split-control LC (SLC) proposed in [9], on the other hand, includes diode-connected PMOS stacks ($M_5$-$M_8$) between pull-up and pull-down devices as shown in Fig. 7. Therefore $|V_{GS}|$ of $M_9$ and $M_{10}$ is equal to $VDD_H - V_D$ instead of a full supply voltage, $VDD_H$, where $V_D$ corresponds to the diode voltage drop across $M_5$, $M_6$, $M_7$, and $M_8$. In addition, $|V_{DS}|$ of $M_9$ and $M_{10}$ is reduced by the diode stacks. This weakens PMOS pull-up current which results in less functional failure and helps to make the falling transition of $n_1$ and $n_2$ faster. The gate of $M_{12}$ is controlled by $n_6$, which swings from $VDD_H$ to prevent the leakage current, hence the name: "Split-control" level converter. Zero-$V_{TH}$ devices, $M_3$ and $M_4$, are cascoded to $M_1$ and $M_2$ to prevent the oxide breakdown.

The proposed level shifter achieved 2.3×, 9.9×, and 5.9× improvements in delay, static power, and energy per transition, respectively, compared to the conventional DCVS structures.

### F. Electrostatic Discharge

Protection from electrostatic discharge (ESD) is required in WSN applications for better reliability. Conventional ESD clamp circuits, however, are extremely wide in size and thus exhibit leakage currents of 10nA to 10uA. Therefore, an ESD structure specialized for WSN is highly demanded.

An ultra-low leakage ESD clamp structure proposed in [10] is shown in Fig. 8 together with a conventional design. In the conventional design, $M_2$ turns on when a high voltage is applied to the supply rail and pulls up the detection node to enable the large shunt device, $M_4$. The leakage current is composed of two major components: 1) detection circuits (particularly $M_2$ as it is sized up to speed detection) 2) the large shunting device M4. Due to the high supply voltage, gate-induced drain leakage (GIDL) of $M_4$ is larger than its subthreshold leakage. In the proposed scheme, a bias voltage of approximately half VDD is generated by a diode stack, $M_5$-$M_{10}$, and is then applied to the topmost stacked output device, $M_{11}$, to reduce GIDL in $M_{11}$ and $M_{12}$. Since there is no leaky PMOS switches, the total area and overall leakage is reduced. Note that $M_5$-$M_{10}$ have minimum width and large length since they only need to overcome the subthreshold leakage of $M_4$ and gate leakage of $M_{11}$. As a result, the diode stack leakage is negligible across temperature and process variations.

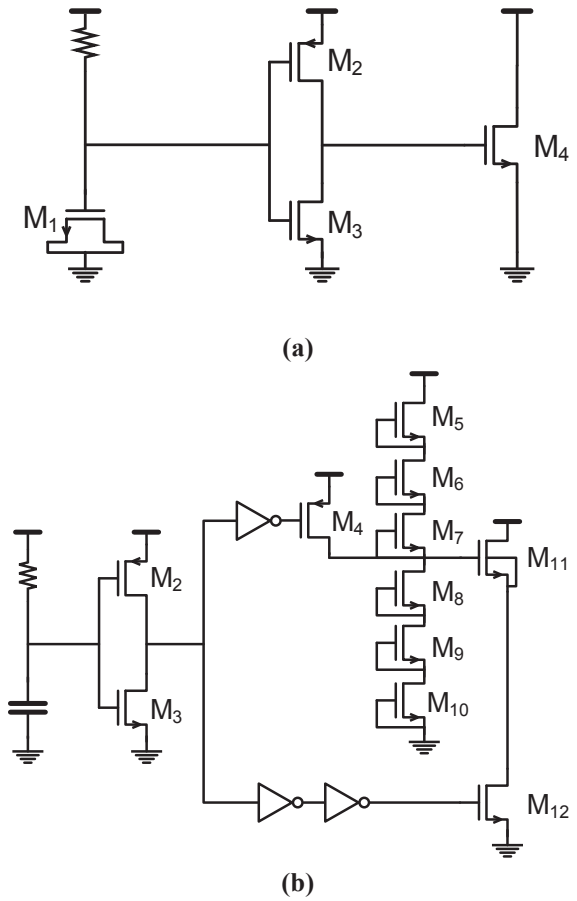


Fig. 8. Schematic of (a) conventional ESD protection circuit and (b) leakage-based GIDL reduction method.

The proposed ESD clamp circuit achieved 18-139× leakage reduction while maintaining 4500V human body model and 400V machine model protection.

### G. Capacitance-to-Digital Converter

Capacitance-to-digital converters (CDCs) are widely used to measure various physical quantities including position, pressure, and concentration of chemicals. However, integrating capacitive sensors into WSN is challenging due to their large power consumption.

Conventional CDCs use charge sharing or charge transfer between capacitors to convert the sampled capacitance to voltage, which is then measured with an ADC. This approach tends to increase design complexity and power consumption.

Fig. 9 explains the conversion method proposed [11]. The top node of sensed capacitor, CT, is directly connected to the supply node of a ring oscillator and initially charged to $V_{HIGH}$. Then, the voltage is discharged gradually by the ring oscillator after the precharge switch is disconnected. As a result, the propagation delay of the ring oscillator increases–this is compared to a constant delay reference. A counter records the number of ring oscillator transitions until the period of the ring oscillator becomes longer than the reference delay, which becomes the output code, $D_{OUT}$.

The proposed scheme greatly reduces circuit complexity and thereby improves the energy efficiency and saves silicon area. It

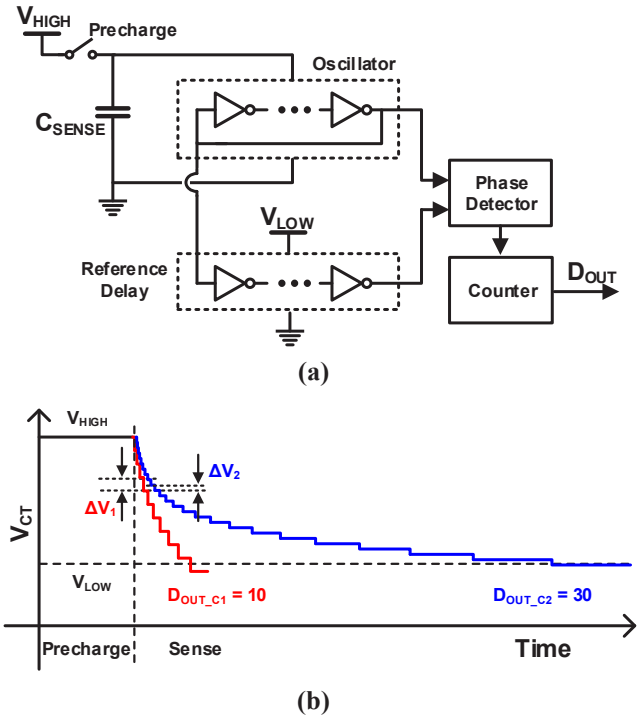


Fig. 9. (a) Schematic of capacitance-to-digital converter using iterative delay-chain discharge and (b) its operation.

provides a capacitor sensing range of 0.7p to 10nF with a 0.06% linearity error and 0.109% resolution (when input capacitance is 11.3pF) and occupies 0.0017mm$^2$ in 40nm CMOS technology.

## III. System Integration

A miniaturized die-stacked imaging system proposed in [3] includes optics, wireless communication, battery, power management, solar harvesting, processor, and memory functionalities as shown in Fig. 10 and Fig. 11. The processor layer includes a Cortex-M0 processor, an optical receiver and a master of inter-layer communication bus (Mbus). The image sensor in the IMG layer is designed to produce 9-bit 160×160 images and has an ultra-low power motion detection capability. An RF transmitter is implemented in the RAD layer and forms two way wireless communication together with the optical receiver in the PRC layer. A 5.7μAh thin-film Li battery is scaled to match the die size and decoupling capacitors in the DCP layer, and it stabilizes the supply voltages.

This stacked structure, shown in Fig. 12, offers a degree of freedom to build a system based on the user's needs by replacing each layer with a proper function. Also, each layer can be fabricated in different processes to maximize benefits from various technologies. For example, the main processor layer that consists of a Cortex-M0 processor, an always-on 3kB retentive SRAM, and a power management system is fabricated in a low leakage 180nm CMOS technology process while the image layer is fabricated in a 130nm.

Bonding wire interconnects overall stacked layers, and then the glass package and dark epoxy encapsulates the system

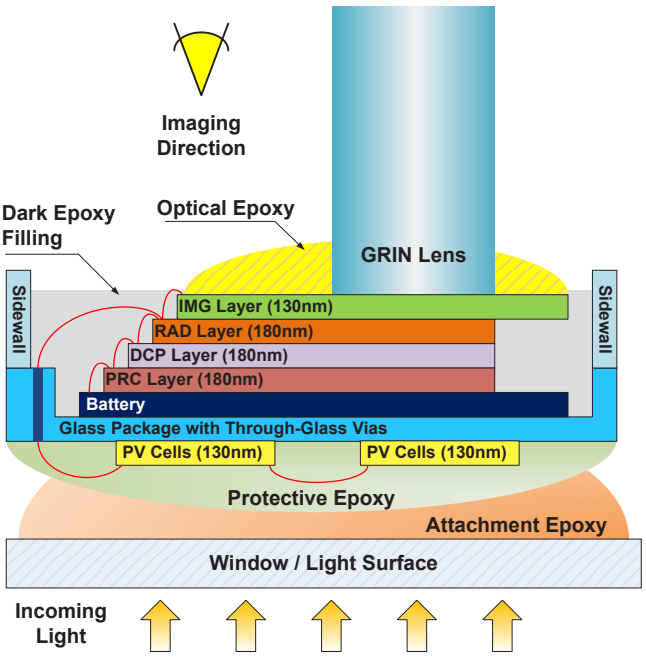


Fig. 10. Cross sectional view of a mm$^3$ scale imaging system.

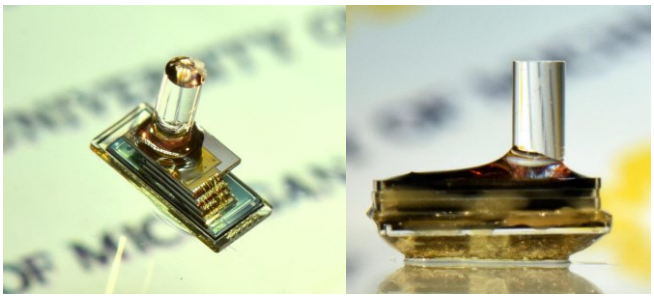

Fig. 11. Photograph of the imaging system. Total area is 2mm × 4mm × 4mm (W×L×H).

preventing light-induced leakage current. A through-glass via in the glass package connects bottom facing photovoltaic (PV) cells to a power management unit (PMU) and a global optical communication (GOC) for harvesting energy and receiving optical data, respectively. A mm-scale gradient-index rod lens is mounted on top of the IMG layer with an optical epoxy.

The proposed imaging system can either survive up to 60 days in a 4nA sleep mode or 3.4 days in an 80nA motion detection mode with the power provided by the battery layer. The image data is sent through RF transmitter with 4nJ/bit energy consumption. Inductive receiver shows -70dBm of sensitivity when it is positioned 15mm away from the system.

## IV. Conclusion

This paper provides a review on the recent advances in ultra-low power circuit techniques to overcome the limited power budget of mm$^3$-scale wireless sensor node applications. A strategy for the system integration is also reviewed with a die-stacked imaging system. It is believed that such advances accelerate the commercialization of robust and efficient wireless sensor nodes.

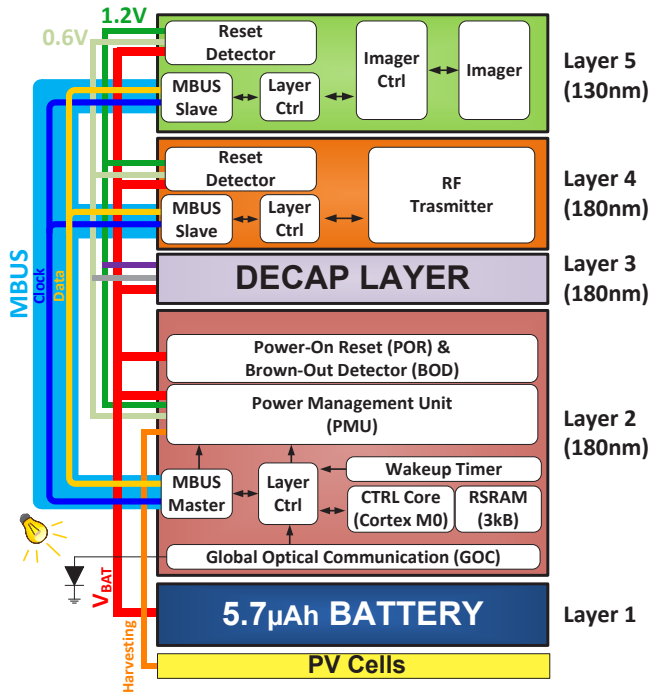


Fig. 12. System level block diagram of imaging system. Key blocks for each layer are shown.

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