Guest Editorial
Low Power Electronics and Design

LOW power design has played an important role in very large scale integration (VLSI) design, particularly as we continue to double the number of transistors on a die every two years and increase the frequency of operation. One important aspect of low power is mobile communications and its impact on our lives. We are at the start of the proliferation of mobile PDA's (Personal Digital Assistants), cellular phones, and portable computing. All of these devices are shaping the way we will be interacting with our family, peers, and workplace and require new and innovative low power design techniques. In addition, low power design techniques are becoming paramount in high performance desktop applications, such as high performance microprocessors, due to cooling and power supply integrity concerns. Hence, low power design can be expected to increase in its prominence as we move to next-generation designs.

In all, 11 papers were accepted for this special issue, which were solicited from the Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED'00). There are seven full papers and four brief papers. These papers were divided into two categories: 1) design tools, systems, and software and 2) architecture, circuits, and technology.

The design tools, systems, and software section has four papers. The first paper by Kruse *et al.* describes a calculation of lower and upper bounds on the power consumption from scheduled data flow graphs. The second paper by Simunic *et al.* discusses low power hardware and software optimization for an embedded system. The last two papers are brief papers. The third paper is a brief by Martin *et al.* that explores different system level factors that affect the power-performance tradeoff and then proposes a method for setting a low bound on CPU speed. The final paper is a brief by Leung *et al.* proposes a low power Turbo decoding approach a reduced number of iterations and dynamic voltage scaling. The architecture, circuits, and technology section has seven papers. The first full paper is by Muhammad *et al.* and describes a finite impulse response filter for magnetic recording. The second paper by Kim *et al.* discusses an adiabatic circuit technique with two times lower energy efficiency over previous work. The third paper by Meninger *et al.* covers a system that translates mechanical vibrations into electrical energy. The fourth paper by Powell *et al.* proposes to reduce the leakage current of an instruction cache through dynamically resizing the cache during the application execution. The last full circuit paper by Soeleman *et al.* discusses a subthreshold logic circuit for ultralow power. The last two circuit briefs are by Svelto *et al.* who describe a CMOS low noise amplifier (LNA) and mixer for GPS applications without using external components, and by Bishop *et al.* who describe a charge recovery databus method that uses adiabatic techniques to reduce power dissipation.

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He worked at the Engineering Accelerator Technology Division, IBM Corporation, Endicott, as a Development Staff Member, until August 1993 . Since then, he has worked for Motorola, Inc., in Austin, TX, where he has been the Manager of the High Performance Design Technology group since September 1994. He manages an international team of approximately 30 people. His work has focused on VLSI design and CAD with particular emphasis on circuit analysis and optimization problems for high performance microprocessor designs and low power DSPs. He has published over 50 papers in refereed journals and conferences, two book chapters, and holds 13 issued patents.

Dr. Blaauw received the Distinguished Innovator Award at Motorola in 2000 and the Best Paper Award at the ACM/IEEE Design Automation Conference in 2000. He has given a number of invited talks and tutorials and is a member of the technical program committee for a number of conferences. He is currently the Technical Program Co-Chair and member of the Executive Committee of the ACM/IEEE Design Automation Conference. He was the Technical Program Chair for the International Symposium on Low Power Electronic Design in 1999 and the General Chair for this symposium in 2000.

Thaddeus Gabara (S'77–M'85) received the B.S. and M.S. degrees in electrical engineering from the New Jersey Institute of Technology, Newark, NJ.

He is a Distinguished Member of the Technical Staff in the Wireless Systems Research at Agere Systems, Murray Hill, NJ. He is involved in the design of architectures for wireless broad-band VLSI systems. His past efforts includes high-speed full custom circuit design, low-power, high-performance clock recovery techniques, RF circuits, speech recognition and synthesis applications, adiabatic circuit design, full custom ATM, and microprocessor chip design. He has authored 50 technical papers and holds over 40 U.S. patents with several pending.

Mr. Gabara is a member of the Technical Committee of the IEEE Custom Integrated Circuits Conference.