

# A Reconfigurable Sense Amplifier with 3X Offset Reduction in 28nm FDSOI CMOS

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## Abstract

This work proposes an area-efficient approach to fully exploit redundancy in reconfigurable sense amplifiers (SAs). The proposed SA can combine/invert offsets of sub-unit SAs, reducing offset by up to  $3.1\times$  at iso-area in 28nm FDSOI.

## Introduction

Sense amplifier (SA) offset is among the most critical factors determining speed, power, and yield in SRAMs. Typically, a 1mV SA offset increase requires 10mV larger bitline voltage differential to maintain a targeted yield [1]. Offset worsens with technology scaling due to increasing random variations [2], and it cannot be mitigated via simple transistor up-sizing without sacrificing array efficiency. Various approaches have been proposed to mitigate offset at a given area, such as selection among different reference voltages (single-ended sensing only) [3], capacitor/transistor strength tuning (with decreasing benefits at finer technologies) [4], and offset cancellation/bitline voltage pre-amplification (uses complex timing, large short-circuit current) [5]. In [6], a novel SA redundancy approach was proposed, based on the observation that selection between two small SA can improve offset compared to one large SA. In this paper, we build on this general direction of using redundancy and show how it can be extended to cancel as well as average offset of smaller SA subunits to obtain significant offset improvement.

## Proposed Topology

The proposed reconfigurable SA is based on the observation that multiple SA sub-units in parallel have a total offset that is the average of the individual offsets (Fig. 1): the individual offsets either subtract each other or sum together depending on whether they have opposite or same signs. Hence, we introduce a reconfigurable SA with the new capability to 1) individually (dis)connect each available SA sub-unit, and 2) individually maintain/swap the two differential inputs. This permits to 1) include/exclude the offset contribution of each SA sub-unit, 2) maintain/flip the sign of each SA offset contribution. Such reconfiguration enables full offset minimization by choosing the best configuration, and enables the possibility of canceling offsets with opposite signs. The proposed approach also makes more efficient use of area than conventional SA redundancy since all SA sub-units can simultaneously contribute to the minimization of offset.

Fig. 1 shows the proposed SA and conventional redundancy SA [6]. The proposed SA consists of two smaller SA sub-units with three pairs of switches. The switches connect the bitlines to the two SA sub-units according to one of four possible SA configurations: 1) only SA1, 2) only SA2, 3) both SAs in parallel (denoted as SA1+SA2), 4) both SAs in parallel with swapped SA2 inputs (denoted SA1-SA2).

Fig. 2 shows SA failure rate versus area, assuming the offset is Gaussian and proportional to  $1/area^{0.5}$  [2]. In this analysis two redundant SAs each with area of 1/2 to 1/9 of a conventional SA are assumed. From Fig. 2, the proposed SA and even the SA1±SA2 configurations alone are able to reduce offset at lower area, compared to conventional SA and conventional redundancy. For example, the typical failure rate of  $1E-8$  (i.e.,  $5.7\sigma$ ) is achieved by the proposed SA and the

(SA1±SA2) configuration with approximately  $3.5\times$  and  $2\times$  smaller area, respectively, compared to the conventional SA. The proposed SA in Fig. 3 is implemented in the same total area as the baseline (conventional SA without reconfigurability). Proposed SA area includes the switch control logic and a bitcell row that stores the SA configuration (Fig. 4), which occupies the two bitcells immediately above the SA (assuming 2:1 column multiplexing). The configuration is normally written into the last-row bitcells and is directly hard-wired to the SA.

## Measurement Results

The offset reduction offered by the proposed technique is measured in a 28nm FDSOI test chip (die photo in Fig. 10), comprising two arrays (conventional and proposed SA array) with 1,000 SAs. For each SA, the configuration, enable, and digital read-out are implemented through scan chains. All SAs share the same input voltage, which is swept to evaluate the resulting offset of all SAs. To limit the kick-back and simultaneous switching noise on SA inputs, two large capacitors are placed on SA inputs, and each SA is enabled individually and sequentially. The overall offset cumulative distribution for the reconfigurable and conventional SAs across 19 dies is shown in Fig. 5, demonstrating much tighter spread that can translate to higher SRAM performance and/or yield. As expected, from Fig. 6 the SA1+SA2 and SA1-SA2 configurations are more likely to minimize the offset compared to other configurations; hence they are more frequently the best configuration. Fig. 7 shows the distribution of measured offset from 19,000 SAs on 19 different dies for each configuration. The proposed technique improves offset by  $3.1\times$  over the conventional SA, and by  $2.1\times$  over conventional SA redundancy with the same area.

The proposed reconfigurable SA is effective at low voltages down to the near-threshold regime (Fig. 8), retaining significant  $2\times$  gains at 0.4V. From Fig. 8, individual selection becomes less effective (and even worsens offset) at low voltages, whereas the proposed redundant SA methods remain beneficial. This also holds true even when restricting the configurations to SA1±SA2 redundancy. Offset increase at reduced voltages is due to the worse voltage scaling of pass-gate reconfiguration switches than other devices. From Fig. 9, the proposed reconfigurable SA has a slightly larger advantage at higher temperatures. The offset of both approaches decrease at higher temperatures, due to lower threshold voltages and larger gate overdrive at high temperatures.

## Acknowledgements

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## References

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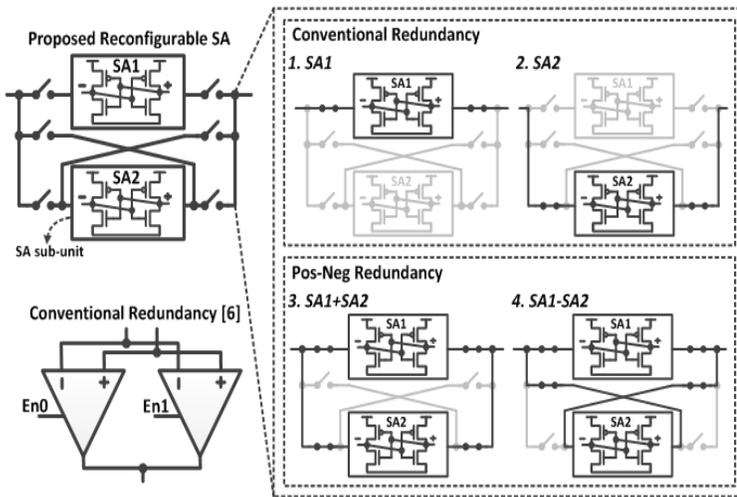


Fig. 1. Block diagram of the proposed reconfigurable SA.

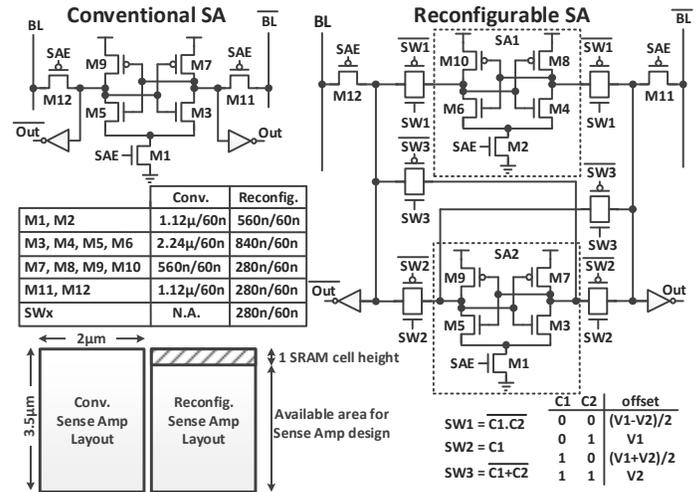


Fig. 3. Schematic, layout, and transistor sizes of conventional and reconfigurable SA. Both SAs are designed with same total area including SRAM bitcell row storing configuration (see Fig. 4).

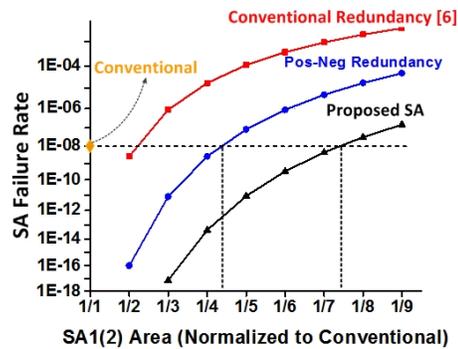


Fig. 2. Statistical analysis of proposed SA offset.

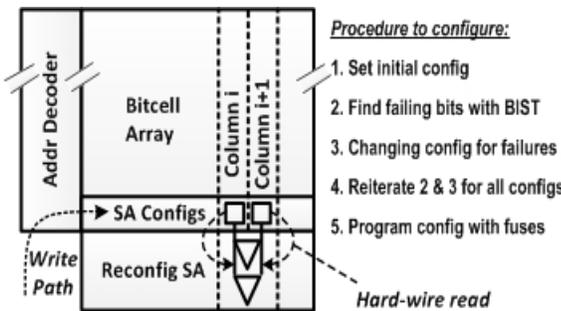


Fig. 4. Conceptual diagram of insertion of the proposed reconfigurable SA in an SRAM array.

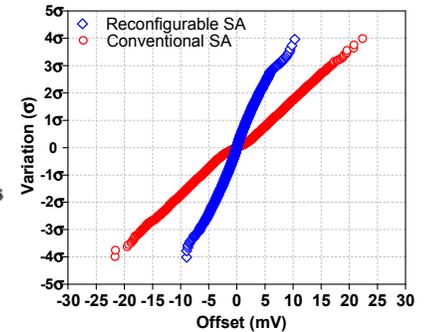


Fig. 5. SA measured offset vs. number of sigma.

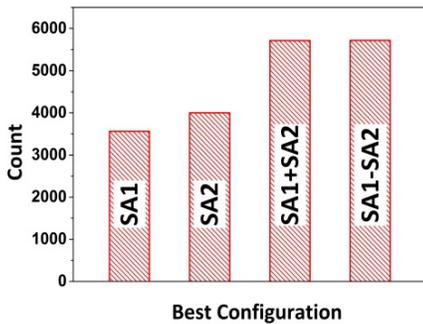


Fig. 6. Reconfigurable SA: statistical distribution of measured best SA configuration leading to minimum offset.

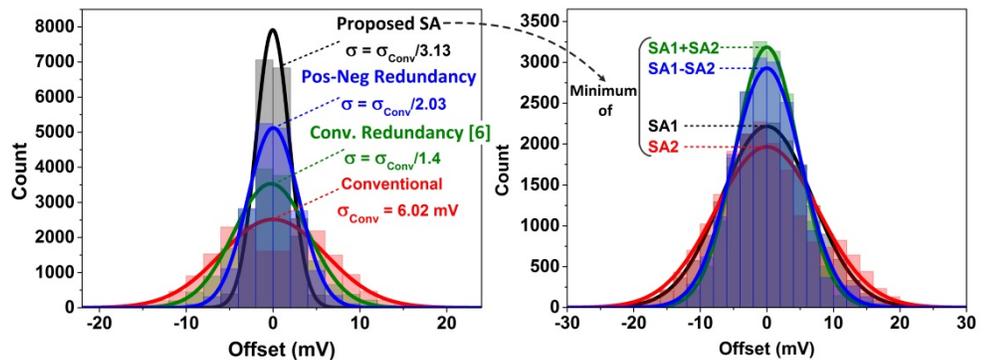


Fig. 7. Comparison of measured offset of proposed and conventional SA for 19k SAs from 19 die (left) and distribution of each single configuration of the proposed SA (right).

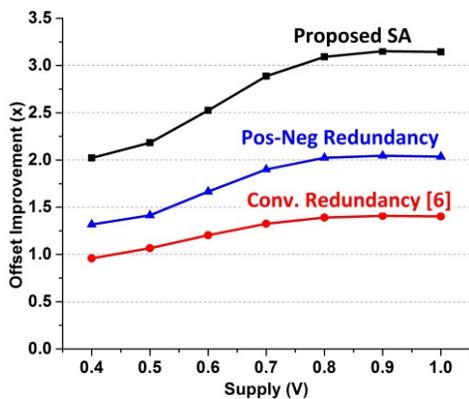


Fig. 8. Measured offset improvement vs. supply.

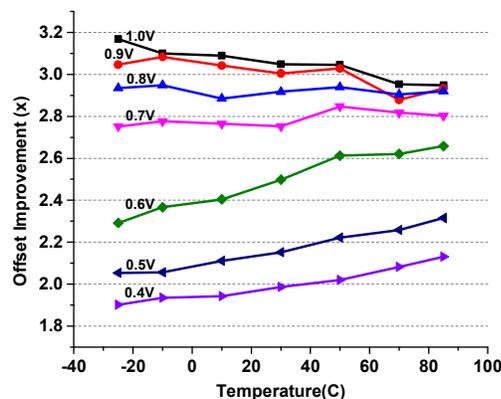


Fig. 9. Measured offset improvement vs. temperature.

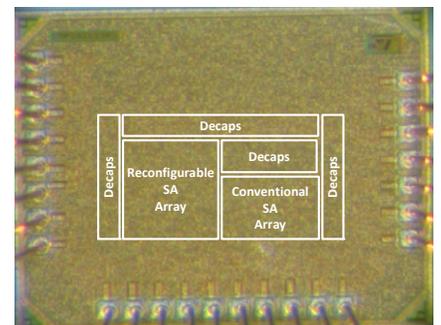


Fig. 10. Die photo of the prototype chip in 28nm FDSOI.