Wide Input Range 1.7µW 1.2kS/s Resistive Sensor Interface Circuit with 1 cycle/sample Logarithmic Sub-Ranging

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Abstract

A wide input range 1.7µW, 1.2kS/s resistive sensor interface circuit fabricated in 0.18µm CMOS is presented. This circuit consumes 6.6× lower power and 31.8× less energy than previous state-of-the-art work, considering the worst-case cycle count required for correct conversion. The proposed design uses a logarithmic subrange detector based on comparator metastability to convert an input resistance ranging from 10kΩ to 10MΩ in 1 cycle/sample.

Introduction

Resistive sensing is widely used in chemical [1], gas [2], and pressure sensing [3], with applications in implantable and point-of-care diagnostics among others. Sensor interface circuits for these systems are challenging due to the wide input resistance (R_{IN}) range (kΩ to MΩ) and µW power constraint to achieve long battery life. In a resistance-to-digital converter (RDC), R_{IN} is first converted to a voltage V_{IN}, then measured by an ADC (Fig. 1). The resistance to voltage conversion is performed by connecting the input resistor to a fixed current source. However, accommodating a high R_{IN} range results in one of two issues: the ADC input voltage will saturate at high R_{IN} or an extremely high resolution ADC is required to sense low R_{IN} that produce very small voltages. Hence, a common approach is to divide the R_{IN} range into sub-ranges and apply different currents for each sub-range using a current DAC (I-DAC) [1,5,6]. This technique greatly increases accuracy across the total R_{IN} range (Fig. 1).

A key challenge in sub-ranging RDCs is finding the correct sub-range. Typically, the RDC starts with an arbitrary sub-range, performs a complete conversion (including ADC step), and examines the resulting code. If this code is out of range, the sub-range is changed (±1 step) and the process repeats until the correct sub-range is found [1,4]. This requires worst-case N iterations to obtain the correct code for 2N-1 sub-ranges, increasing energy and slowing the sampling rate.

To address this issue, we propose a new sub-ranging RDC that finds the correct sub-range within 1 sampling cycle using a novel logarithmic converter. We also note that the energy consumed by the I-DAC is a major portion of total energy consumption. This work minimizes I-DAC energy by dynamically adjusting its on-time according to the sub-range setting, whereas previous RDCs enable the I-DAC for the worst-case stabilization time. In addition, a switched capacitor (SC) amplifier is inserted prior to the ADC; it improves ADC resolution and reduces energy via shorter V_{IN} settling time. The proposed design consumes 1.7µW. It reduces energy per conversion by 31.8× compared to current state-of-the-art RDCs [1,2,4] and achieves 1000× R_{IN} range with 0.21% measurement error.

Logarithmic Sub-Range Detector

Fig. 2 shows the logarithmic sub-range detector. The full R_{IN} range is divided into sub-ranges that increase in geometric fashion. Hence, the correct sub-range is found by taking the log of R_{IN}. To implement this log function, we use the intrinsic behavior of a comparator operating near its metastable point. R_{IN} is first converted to V_{IN} by the I-DAC, sampled on C_{SAMPLE} and shifted up by V_{REF} to position both V_L and V_R at the metastable point. At this point, φ2 switches are opened and a cross-coupled inverter pair starts to resolve V_L and V_R. If V_{IN} is large, V_L (V_R) resolves to 1.2V (0V) quickly, while this resolution time increases exponentially as V_{IN} becomes smaller. The subsequent inverter chains and XOR output 0 and stop the counter when V_R becomes lower than $V_{DDI}/2$ (mathematical analysis in Fig. 2). The proposed log converter determines the correct sub-range in one comparison, enabling 1 cycle/sample operation. To remove the effect of charge injection, the voltage transfer circuit uses bottom-plate sampling and the SC structure uses stray-capacitance insensitive topology. Auto-zeroing is also adopted for offset cancellation, resulting in offset of σ=0.24mV (40× smaller than without auto-zeroing, simulation). Across process corners, comparator gain is one-point calibrated to maintain a consistent code range.

Resistance to Digital Conversion

After the correct sub-range is found for a particular R_{IN}, the corresponding I-DAC current is selected and V_{IN} is generated from the resulting IR drop (Fig. 3). V_{IN} is transferred to V_{OUT+} and V_{OUT-} (with opposite sensitivities to V_{CM}) via two SC amplifiers and then digitized by a 10-bit SAR ADC. The SC amplifiers are used for three reasons: 1) they perform pseudo-differential sampling to cancel out common-mode voltage; 2) they increase usable ADC output range by SC amplifier gain and thus enhance resolution by 1.98×; 3) they decouple the large capacitor DAC (C_{DAC+}, C_{DAC-}) from the R_{IN}. If the large C_{DAC} is used as the sampling capacitor, the I-DAC must remain on for a longer time due to the large RC time constant. By sampling with the smaller $C_{SAMPLE+,-}$ (1pF) and charging $C_{DAC+,-}$ (9.3pF) in a different phase, energy is reduced by 7.7× compared to an approach where $C_{DAC+,-}$ is used as the sampling capacitors.

Fig. 4 shows the flow chart of the RDC conversion process. First, a 300nA current ($I_{INITIAL}$) is applied to the unknown R_{IN} and the resulting $I_{INITIAL}\times R_{IN}$ is sampled. This $I_{INITIAL}$ is chosen to map the entire R_{IN} range (10kΩ – 10MΩ) to the log converter's operating range. The log converter then produces a counter value that is compared to 4 threshold values to determine 4 coarse sub-ranges. According to the coarse sub-range, a second current (6.4µA, 1.6µA, 0.4µA, or 0.1µA) is activated on the I-DAC resulting in an $I_{COARSE}\times R_{IN}$ spanning 50−800mV in each coarse sub-range. The same procedure repeats to divide each coarse sub-range into 5 fine sub-ranges, yielding 14 possible sub-ranges. Sub-ranges overlap to guarantee correct conversion for the entire R_{IN} range. Each of the 14 fine sub-ranges specifies an I-DAC setting that ensures $I_{FINE}\times R_{IN}$ lies in the SC amplifier operating range. This voltage is then pseudo-differentially sampled and converted into a digital code by the 10b SAR ADC. Also, each fine sub-range specifies a sampling time, minimizing I-DAC activation time and reducing worst-case power consumption by 21%. Finally, recall that in the proposed RDC, sub-range determination is performed every conversion cycle, in contrast to traditional RDCs that can require multiple cycles to determine the correct sub-range.

Measurement Results

Fig. 5 shows measured log converter counter values at different V_{IN}. Because the converter is based on metastability, it is susceptible to noise and hence ±1σ curves are shown. Each sub-range overlaps with its adjacent sub-ranges to provide error tolerance and ensure the probability of a sub-ranging failure (i.e., R_{IN} falls outside a correct sub-range) to be $< 3.2\sigma$ probability for sub-range 1 and $< 5\sigma$ probability for sub-ranges 2 − 4. The worst-case measurement error is 0.21%. Off-chip 0.01% precision resistors are used to measure accuracy and the resistor bottom node voltage is swept with a sourcemeter to obtain additional equivalent resistances. The error pattern reflects repeated error behavior in each sub-range. A 10b ADC with SC amplifier shows DNL of +0.37/-0.56LSB and INL of +0.93/-1.48LSB. The SC amplifier slightly degrades INL but improves resolution by 1.98×, resulting in better accuracy overall. At the minimum input resistance, the circuit consumes its maximum 1.7µW at a sampling rate of 1.2kS/s. Power consumption is 6.6× smaller than the state-of-the-art work in [4]. Table 1 compares the RDC with prior work showing large resistive range and similar conversion rate while worst-case energy/conversion is reduced by ~31.8×. A resistive CdS light sensor was successfully measured with the RDC (Fig. 6). Total design area is 1.5×0.82mm^2 in 0.18µm CMOS (Fig. 7).

References

[1] Taeg Sang Cho, et al., *JSSC*, Feb. 2009.
[2] Grassi, M., et al., *JSSC*, Mar. 2007.
[3] Rong Wu, et al., *ISSCC*, 2011.
[4] Hyunsoo Ha, et al., *CICC*, 2012.
[5] Xiaoyi Mu, et al., *ISCAS*, 2011.
[6] A. Lombardi, et al., *Sensors and Actuators B 142*, 2009.

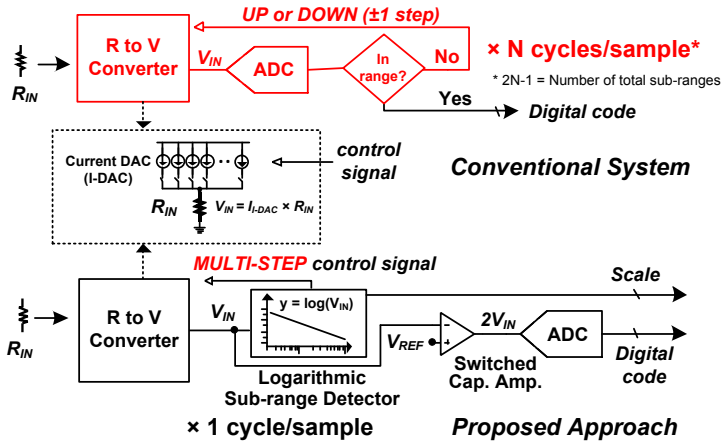

Fig. 1. An overview of N cycles/sample conventional RDC and a proposed 1 cycle/sample RDC with logarithmic sub-range detector.

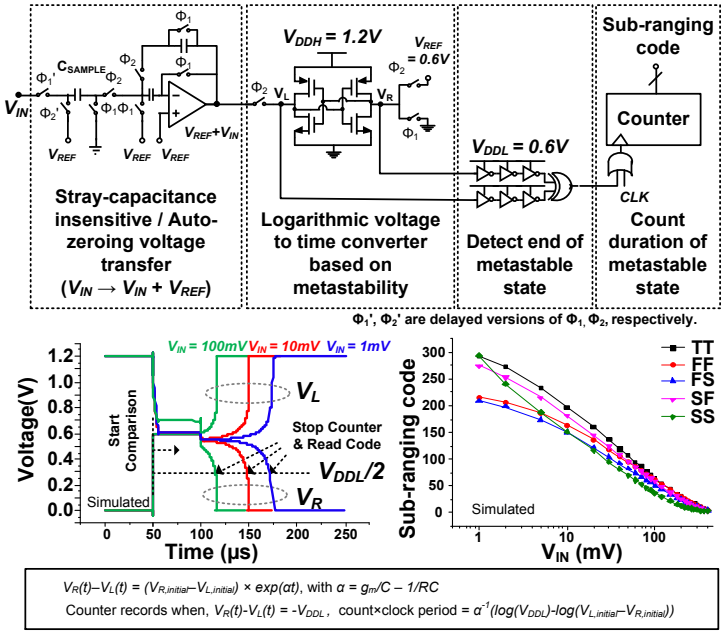

Fig. 2. A logarithmic voltage-to-time converter based on comparator meta-stability resolution time, and its transient voltage behavior and sub-ranging code output vs. V_{IN}.

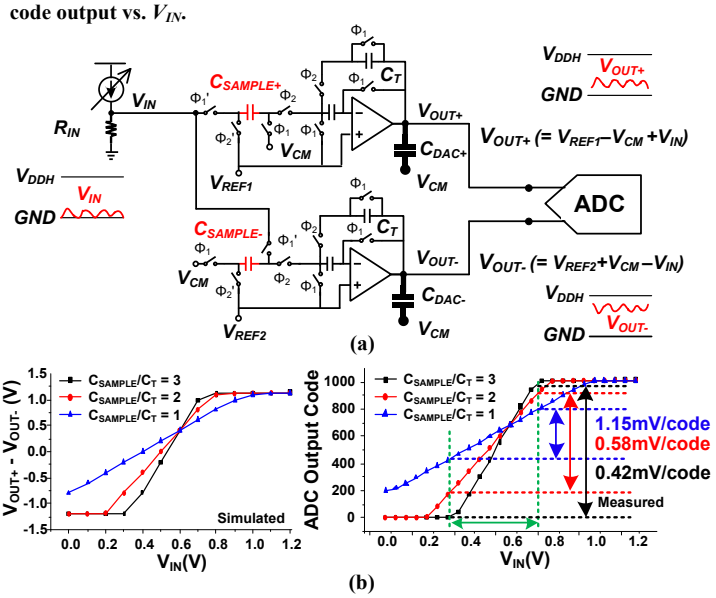

Fig. 3. (a) A switched capacitor amplifier that pseudo-differentially samples input and (b) improvement of ADC resolution by SC amplifier gain.

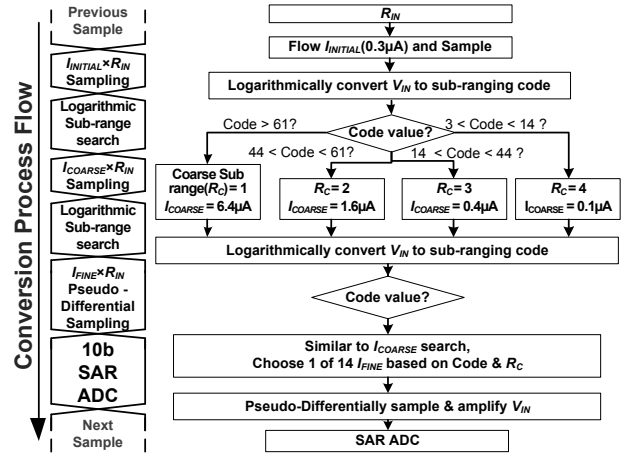

Fig. 4. Conversion process flow chart of 1 sample. R_{IN} is logarithmically compressed, sub-ranged, then converted by 10b ADC.

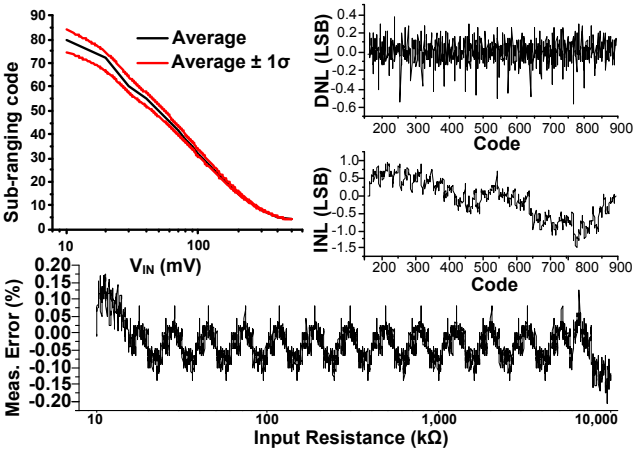

Fig. 5. Measured results of a sub-ranging, DNL & INL of 10b ADC with SC amplifier, and measurement error for input resistance range.

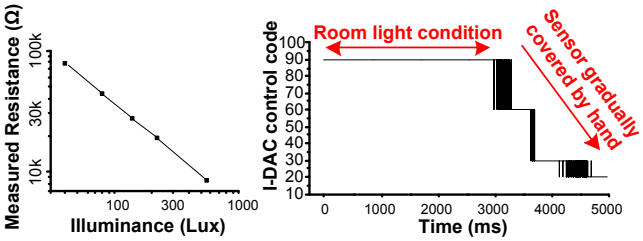

Fig. 6. Conversion result measured with off-the-shelf CdS light sensor.

TABLE I. Performance summary and comparison.

	This work	CICC 2012 [4]	ISCAS 2011 [5]	JSSC 2009 [1]	JSSC 2007 [2]	Sensors and Actuators B 142 2009 [6]
Technology (μm)	0.18	0.13	0.5	0.18	0.35	0.35
Required number of cycle (worst case)	1	4	N/A	5	6, (5 cycles with coarse ADC)	8
Supply (V)	1.2/0.6	0.5	3.3	1.2/0.5	3.3	N/A
Input Range (Ω)	10k – 10M	23k – 4.6M	60k – 10M	10k – 9M	100 – 20M	10k – 2G
Max. R / Min. R	1,000	200	166.7	900	200,000	200,000
Conv. Rate (kS/s)	1.2	1	N/A	1.83	0.1	N/A
Meas. Error (%)	< 0.21	< 0.32	N/A	< 1.32	< 0.14	< 2.7
Energy/conversion (nJ) (worst case)*	1.42	45.2	N/A	87.4	> 60**	N/A
Power (μW)	1.7	11.3	66	32	6,000	10,000

* Assumes a worst case cycle count and minimum input resistance.
** Coarse ADC power is not reported, thus extra energy needed for finding sub-range is not included.

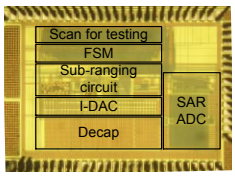

Fig. 7. Microphotograph (1.5 × 0.82mm^2).