SOI transistor model for fast transient simulation

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Abstract

Progress in semiconductor process technology has made SOI transistors one of the most promising candidates for high performance and low power designs. With smaller diffusion capacitances, SOI transistors switch significantly faster than their traditional bulk MOS counterparts and consume less power per switching. However, design and simulation of SOI MOS circuits is more challenging due to more complex behavior of an SOI transistor involving floating body effects, delay dependence on history of transistor switching, bipolar effect and others. This paper is devoted to developing a fast table model of SOI transistors, suitable for use in fast transistor level simulators. We propose using body charge instead of body potential as an independent variable of the model to improve convergence of circuit simulation integration algorithm. SOI transistor has one additional terminal compared with the bulk MOSFET and hence requires larger tables to model. We propose a novel transformation to reduce number of table dimensions and as a result to make the size of the tables reasonable. The paper also presents efficient implementation of our SOI transistor table model using piece-wise polynomial approximation, nonuniform grid discretization, and splitting the transistor model into the model of its equilibrium and non equilibrium states. The effectiveness of the proposed model is demonstrated by employing it in a fast transistor level simulator to simulate high performance industrial SOI microprocessor circuits.

1 Introduction

SOI technology is one of the most promising ways to increase switching speed of MOS transistors without changing their size [1], [2]. SOI transistors have significantly less source and drain diffusion capacitances and lower body effect resulting in reduction of gate delays and power dissipation. Another very attractive feature of SOI technology is the possibility to use the same schematic solutions that were used by bulk digital chips. Unfortunately, designing SOI VLSI circuits is more difficult than designing traditional bulk MOS circuits due to significantly more complex behavior of SOI transistors [1]. Unlike their bulk MOS counterparts, SOI transistors are fabricated in electrically isolated islands of silicon. So their bodies are completely isolated from each other. This allows to use them in different configurations: connect body to transistor source, connect body to any node of the circuit or, leave body floating. The last case is the most common as it requires the least transistor size and provides the fastest switching speed. However, the behavior of floating body SOI transistor is the most complex. The most important phenomena are: history, bipolar, and I-V curve kink effects [1], [2]. Due to history effect, delays of logic cells depend on their switching history. Bipolar effect is an additional source of noise in circuits that may lead to malfunctions.

Transistor level simulation is traditionally used for designing and characterizing library cells and critical blocks of custom VLSI circuits. Due to complex behavior of the SOI transistor, designing SOI circuits requires even more simulations at transistor level than do traditional MOS circuits. Large amount of simulations and relatively low performance of SPICE simulators are critical issues in VLSI design flow. To reduce simulation time, it was proposed to use fast simulators for simulating large digital blocks at transistor level [3], [9]. Fast simulators generally are simplified versions of SPICE simulators with significantly higher simulation speed obtained at the expense of slightly low accuracy. Fast transient simulators for SOI circuits are even more beneficial than for bulk CMOS circuits as the speed of SPICE simulators for SOI circuits is usually much less than for bulk ones. This is due to significantly higher complexity of the SOI transistor model, smaller time step, and worse convergence properties of the SOI transistor model.

One of the key components of a fast transient simulator is a transistor model. Obviously the accuracy of the simulator cannot be better than the accuracy of the model. Efficiency of any kind of transistor level simulator greatly depends on the efficiency of its transistor model. In case of a fast simulator, this is especially true because it uses simplified simulation algorithms and the relative amount of transistor model computation is much higher than that for a traditional simulator. Accurate transistor models such as BSIM3SOI [8] used in SPICE, are not suitable for fast simulators because of their complexity and low speed.

Models of MOS transistors for fast simulation attract lots of interest. In this well studied field of computer aided design, it was widely recognized that only table models can provide both high speed and acceptable accuracy [3], [4], [5], [6], [7]. As many authors have observed, there are two contradictory goals of constructing transistor table models: accuracy and size of tables.

The traditional bulk MOSFET requires 3 dimensional tables for describing its currents and charges [5]. However it was noticed that MOSFET behavior can be approximated by two dimensional tables using the so called "gate-offset-voltage concept" [5], [6] that was very successfully used in PowerMill [3] and many other fast circuit simulators. It is based on the observation that substrate voltage does not change significantly the shape of source-drain I-V curves, but only shifts them by affecting gate threshold voltage. According to this concept, the source-drain current is expressed not as a function of drain, gate and substrate voltages V_d, V_g, V_s, but as a function of drain voltage and effective gate voltage $V_{g,eff}$ which is the difference between gate voltage and threshold voltage $V_{g,eff} = V_g - V_{th}$. The threshold voltage V_{th} is expressed as a function

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of substrate voltage V_y and modeled by a one-dimensional table. However, our experiments showed that, although this approximation is sufficiently accurate for long channel MOSFETs, it is less accurate for deep submicron devices, especially for their low threshold varieties and even less accurate for SOI transistors. We therefore do not use this approach for building our model, though it is completely orthogonal to our technique and can be combined with it if the goal is a smaller model size at the cost of accuracy.

Another useful technique for constructing accurate compact MOS transistor models is using non uniform discretization grid [4],[6]. This approach exploits the fact that MOSFET I-V curves have different degree of non-linearity in different voltage regions. Model tables for nonuniform grids have complex structure and require special access structures like trees [4],[6]. In our models we use nonuniform discretization grid combined with binary access trees. To reduce approximation error and to use coarser discretization grid, we also found it useful to use piece-wise polynomial approximation instead of the commonly used piece-wise linear approximation.

Above mentioned research on table models of MOSFETs considers only traditional bulk transistors. SOI MOSFET has many added features and significantly more complex behavior that poses additional challenge to constructing a compact accurate table model suitable for fast simulation. In this paper we consider the main differences between modeling of SOI and bulk MOS transistors, and present an SOI transistor model developed for our fast transient simulator FSIM. This tool is used in our VLSI design flow for transistor level simulation of both SOI and bulk CMOS circuits. It is used both as an independent circuit simulator and as part of noise analysis [10] and power estimation tools. The main goal we set while constructing FSIM was obtaining high simulation speed without significant loss of accuracy. For high efficiency and controlled accuracy we used tables for both current and charge to model both resistive and capacitive non-linearities.

Constructing a table based model for an SOI transistor is a significantly more difficult problem than for a bulk one. The accuracy requirement is significantly higher than that for a bulk transistor because even a small error in computing floating body charge may accumulate during simulation and result in a completely wrong prediction of its potential and consequently a wrong value of the transistor threshold voltage. On the other hand all floating body effects are extremely sensitive to simulation inaccuracy due to very small capacitance of the transistor body.

An SOI transistor has an extra external terminal compared to a bulk transistor. Therefore, an SOI transistor model requires an additional independent variable. The resulting size of multidimensional tables of such a transistor model is too large to provide reasonable efficiency. Thus the problem of reducing size of SOI model tables is even more important than in the case of bulk transistors. In the proposed model we use a novel transformation to reduce the number of independent table variables, exploiting an assumption about linearity of capacitance between transistor backgate and body. Additionally we reduce the size of tables by using nonuniform grid and piece-wise polynomial approximation. For increased simulator accuracy we construct a table model minimizing the errors in both the function and its derivative. For fast access to table values, we use a multidimensional binary search tree, providing logarithmic access time to individual grid cells.

As mentioned above, the SOI transistor body which has very small capacitance can change its potential very fast due to capacitive coupling. On the other hand the speed of the body charge variation is significantly slower[2]. As a result, the differential equations describing SOI circuits are very stiff and difficult to integrate. We therefore propose to use body charge as an independent variable instead of its potential. This helps integrating circuit equations since body charge cannot change as fast as its potential. In order to support this change of variables, our transistor model uses body charge as an independent variable.

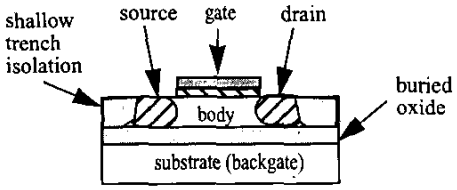
The rest of the paper is organized as follows. In section 2 we describe possible types of SOI transistors and their main features affecting and complicating construction of a compact table model. Section 3 presents the proposed table model of SOI transistor. It describes our approach to reduce the number of table dimensions and improve model characteristics required by a fast transient simulator. Section 4 provides important details of nonuniform discretization of the model domain, approximation technique, and data structures for fast table access. In section 5 we briefly describe our technique and algorithm for building table models at transistor characterization time. Section 6 gives some numerical characteristics of our model and demonstrates the results of using this model in our fast transistor level simulator FSIM. In section 7 we draw conclusions and outline some future work.

2 SOI transistor and its effects

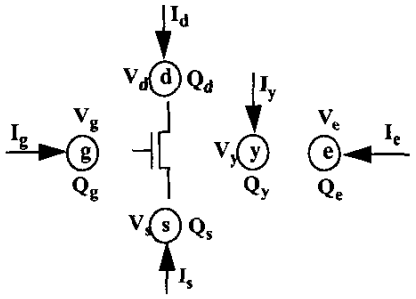
The structure of an SOI transistor is shown in Figure 1 (a). In general it is similar to traditional bulk MOSFET. However each SOI transistor is fabricated in its own silicon island that is isolated both from the silicon substrate by buried oxide and from all the other transistors by shallow trench isolation. Due to oxide isolation an SOI transistor has very small diffusion capacitance [1], [2]. Therefore performance of SOI circuits is significantly higher than that of traditional ones.

The substrate of an SOI chip is the 5-th terminal of an SOI transistor, affecting its behavior through capacitive coupling. Thus, unlike traditional MOSFET, the electrical model of an SOI transistor has 5 terminals (Figure 1 (b)) thus increasing the number of independent variables and correspondingly the number of dimensions of a table model. In our model we apply special transformation of variables to reduce the number of table dimensions.

The body of an SOI transistor plays the same role as the substrate of a traditional MOSFET but it is electrically isolated from bodies of all other transistors. Electrical isolation of transistors bodies provides several ways of using an SOI transistor in circuits that differ with body connection [2]. The simplest and the most common way to use an SOI transistor is to leave its body floating. This requires the smallest area for the transistor. Another benefit of this usage is that in most cases transistors with floating body are faster because of reduced body effect on the transistor threshold voltage. However, transistors with floating body are the most difficult case for simulation. Unlike traditional bulk MOSFET, the state of an SOI transistor with floating body is not defined uniquely by the voltages applied to the external transistor terminals: source, drain, gate and backgate. The state of the transistor depends additionally on the body potential that can not be directly controlled externally. The transistor body can be either in an equilibrium or non-equilibrium state with the other transistor terminals. In the equilibrium state, the transistor body voltage has reached a stable



(a) structure of SOI transistor



(b) electrical model of SOI transistor:
d-drain, s source, g - gate, y- body, e-backgate substrate
I_d, I_s, I_g, I_y, I_e - transistor terminal currents
V_d, V_s, V_g, V_y,V_e- transistor terminal voltages
Q_d, Q_s, Q_g, Q_y, Q_e- transistor terminal charges

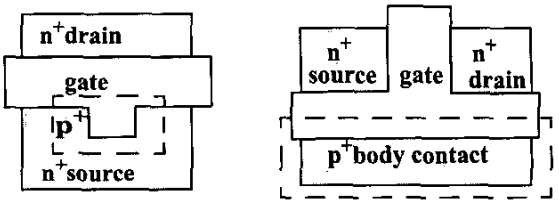
Figure 1. Structure and model of SOI transistor

value after setting external transistor terminal voltages. In this state, transistor charges are also stable. However immediately after changing terminal voltages, transistor body has the charge and voltage different from the equilibrium values and these values will change due to internal currents even without any external causes.

The potential and charge of a floating body is affected by multiple influences and can vary in a very wide range. Body potential depends on both own body charge and potentials of the other transistor terminals affecting the body through capacitive coupling. In the transistor off state its body is completely isolated from other circuit nodes and can abruptly change its potential without changing its charge because of capacitive coupling to other transistor terminals. That kind of behavior is very difficult for simulation in the traditional way when circuit node potentials are independent variables defining circuit state. In order to improve accuracy of integrating circuit differential equations, we use body charge as an independent variable. Thus, in our fast transient simulator circuit state is defined as a combination of nodes potentials and transistors body charges. For implementation, we developed necessary transformation of transistor and circuit equations.

Another difficult problem of modeling an SOI transistor with floating body is related to so called "history effect". Transistor threshold voltage depends on body potential and through it on body charge. On the other hand, body charge depends on rather small currents due to impact ionization and junction leakage that occur during transistor switching and in its off state too. The characteristic time of this mechanism is of the order of magnitude of milliseconds. As a result, body charge acts like a memory remembering switching history of the transistor [1], [2]. That kind of transistor behavior creates significant difficulties for circuit simulation because even very small errors in a model or integration can accumulate over the simulation time and result in large error of body charge and potential and, consequently in wrong value of transistor threshold voltage. Therefore simulation of SOI circuits requires very high accuracy of the transistor model both for its currents and charges. The necessity of computing accurate transistor charges requires non-linear models of transistor capacitances. To accommodate these requirements, our model includes tables for both currents and charges, imposing stringent constraints on the table sizes.

The second type of body connection is connecting it to the transistor source through P^+ diffusion region and salicide covering N^+ and P^+ regions as shown in Figure 2(a). That kind of an SOI transistor is called a source tied SOI transistor [2]. Its usage is significantly rare in digital circuits because it requires larger area for transistor and does not provide significant benefits. Characteristics of an SOI transistor with source tied body are similar to those of the traditional MOSFET with source connected to substrate.



(a) layout with source tied body

(b) layout with T-shaped body contact

Figure 2. Layout of SOI transistors

The third type of body connection is through construction of a separate contact for body as shown in Figure 2 (b) [2]. Using this contact, the body can be connected to any node of the circuit. This type of connection is sometimes used in analog circuits and some other special cases such as memory sense amplifiers when explicit body potential control is required. With this connection transistor behavior is easier to model than a floating body transistor as the body potential is equal to the potential of the circuit node that it is tied to. Furthermore, the body connected this way attenuates the influence of the transistor backgate.

3 Simplified SOI transistor model

The electrical model of an SOI transistor is shown in Figure 1 (b). It includes 5 terminals: source, drain, gate, body and substrate or backgate. For each terminal we have its potential V, charge Q and current J flowing to it. Transistor behavior is invariant to the constant shift of all its terminal potentials. So we can select 4 terminal potentials as independent variables and measure them with respect to the fifth terminal. Following tradition, we use the source of the transistor as a reference terminal. Due to charge conservation law, the sum of all the transistor terminal charges is 0 and due to Kirchoffs current law, sum of all its terminal currents is also 0.

So we can use terminal potentials V_d, V_g, V_y,V_e as independent variables and consider terminal charges Q_d, Q_g, Q_y, Q_e and currents I_d, I_g, I_y, I_e, as their functions. Then the transistor behavior in a circuit is described by the following differential equations:

$$\dot{Q}_i(V_d V_g V_y V_e) + J_i(V_d V_g V_y V_e) = I_i \qquad \text{(EQ 1)}$$

where:

- V_i (i = d, g, y, e) are transistor drain, gate, body and backgate voltages measured with respect to the transistor source
- J_i and Q_i (i = d,g,y,e) are transistor terminal currents and charges
- I_i (i = d,g,y,e) are external currents at transistor terminals

These equations are the formulation of Kirchoff law for currents at transistor terminal nodes. They should be accompanied by equations of the transistor model:

$$Q_i = Q_i(V_d V_g V_y V_e)$$
$$J_i = J_i(V_d V_g V_y V_e) \qquad \text{(EQ 2)}$$

In our model, we neglect the gate and backgate currents because they are close to 0 for SOI MOS transistors.

3.1 Independent variables change

As it was mentioned above, floating body potential of an SOI transistor can change its value very abruptly even when the body charge does not change at all. It happens due to capacitive coupling of the body with the other transistor terminals. This fast voltage variation can be rather high because floating body capacitance is very small. On the other hand body voltage can vary slowly due to very small impact ionization and leakage currents [1], [2]. This imposes strict requirements both for integration time step and accuracy of circuit simulator. However body charge can not change its value as fast because the value of the body current is limited. Therefore body charge variation has significantly larger characteristic time of variation. So using body charge as an independent variable during circuit simulation, we can increase the minimum simulation time step and, consequently increase the speed of the simulation.

However direct usage of body charge as an independent variable is not convenient enough. Unlike node potentials, body charge may vary significantly from transistor to transistor depending on the transistor size. Therefore we apply a linear transformation to body charge to make its range of variation approximately the same as the range of circuit voltages. This new variable is called normalized shifted body charge:

$$U_y = V_{dd} \cdot \frac{Q_y - Q_{ymin}}{Q_{y,max} - Q_{y,min}} + V_e \qquad \text{(EQ 3)}$$

where $Q_{y,min}$ and $Q_{y,max}$ are minimum and maximum body charges when body voltage changes from 0 to V_{dd}. From this equation we can see that the difference between normalized body charge and backgate voltage U_y-V_e varies linearly from 0 to V_{dd} when body charge varies from minimum to maximum values. This kind of behavior is similar to variation of the other circuit voltages, simplifying error control during integration of circuit equations.

By introducing average body capacitance:

$$\bar{C}_{yy} = (Q_{ymax} - Q_{ymin})/V_{dd} \qquad \text{(EQ 4)}$$

we can simplify the formula for normalized shifted body charge in the following way:

$$U_y = \frac{Q_y - Q_{ymin}}{\bar{C}_{yy}} + V_e \qquad \text{(EQ 5)}$$

From this we can express body charge as follows:

$$Q_y = \bar{C}_{yy} \cdot (U_y - V_e) + Q_{ymin} \qquad \text{(EQ 6)}$$

Splitting transistor equations into the equation describing body currents and the rest, we rewrite EQ1 as follows:

$$\dot{Q}_i(V_d V_g U_y V_e) + J_i(V_d V_g U_y V_e) = I_i \qquad \text{(EQ 7)}$$
$$\dot{Q}_y(V_d V_g U_y V_e) + J_y(V_d V_g U_y V_e) = I_y$$

By computing time derivatives using chain rule and substituting EQ6 for charge, we obtain transistor equations with shifted normalized body charge as an independent variable:

$$\sum_{k\,=\,dge} C_{ik} \cdot \dot{V}_k + \frac{\partial Q_i}{\partial U_y} \cdot \dot{U}_y + J_i(V_d V_g U_y V_e) = I_i \qquad \text{(EQ 8)}$$
$$\bar{C}_{yy} \cdot (\dot{U}_y - \dot{V}_e) + J_y(V_d V_g U_y V_e) = I_y$$

where:

$$C_{ik} = \frac{\partial Q_i}{\partial V_k} \qquad \text{(EQ 9)}$$

3.2 Reduction of independent variables

As it was mentioned above, the behavior of an SOI transistor depends on 4 independent variables which highly complicates constructing a compact model as it requires four dimensional tables. However it is known that transistor currents are almost independent of backgate voltage. Ignoring this dependence we have currents as functions of 3 variables only.

$$J_i(V_d, V_g, V_y, V_e) = J_i(V_d, V_g, V_y) \qquad \text{(EQ 10)}$$

The capacitance between a backgate and the other transistor terminals almost does not depend on the terminal voltages because the backgate is separated from the other parts of the transistor by thick oxide layer that is a good dielectric material. Figure 3 shows that all the transistor terminals charges depend on the backgate voltage linearly. We can use this fact for simplifying our transistor

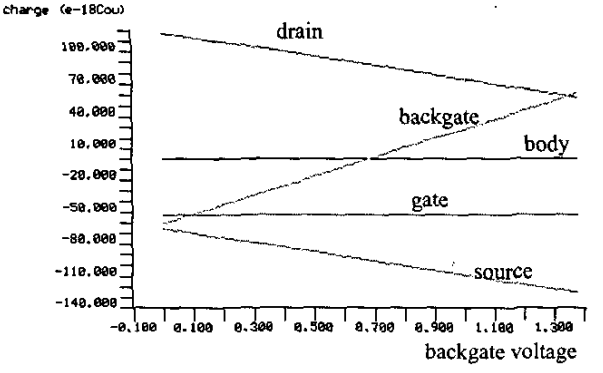


Figure 3. SOI transistor charges as function of backgate voltage

model by separating its linear and non-linear parts.

Assuming constant capacitance between a backgate and the other transistor terminals, transistor charges can be expressed as follows:

$$Q_i(V_d, V_g, V_y, V_e) = Q_i(V_d, V_g, V_y, 0) + C_{ie} \cdot V_e \quad \text{(EQ 11)}$$

where:

$$C_{ie} = \frac{\partial Q_i}{\partial V_e} = const \quad \text{(EQ 12)}$$

Equations EQ10 and EQ11 are used to model an SOI transistor with its body as an independent terminal. They can be modeled using only three dimensional tables. To model charge equations we need to construct tables only for the case when backgate voltage is 0. For all the other backgate voltages, transistor charges can be computed using EQ11. For source tied body the situation is even simpler as body voltage is always equal to the source voltage.

For floating body SOI transistor the model is more complicated because body charge is an independent variable. Comparing EQ6 and EQ11 we can construct the equation for body charge:

$$Q_y(V_d, V_g, V_y, 0) + C_{ye} \cdot V_e = \overline{C}_{yy} \cdot (U_y - V_e) + Q_{ymin} \quad \text{(EQ 13)}$$

By rearranging terms it can be transformed into the following:

$$Q_y(V_d, V_g, V_y, 0) = Q_{ymin} + \overline{C}_{yy} \cdot \left(U_y - V_e - \frac{C_{ye}}{\overline{C}_{yy}} \cdot V_e\right) \quad \text{(EQ 14)}$$

Introducing a new variable U'_y

$$U'_y = U_y - \left(1 + \frac{C_{ye}}{\overline{C}_{yy}}\right) \cdot V_e \quad \text{(EQ 15)}$$

equation EQ14 can be rewritten as:

$$Q_y(V_d, V_g, V_y, 0) = Q_{ymin} + \overline{C}_{yy} \cdot U'_y \quad \text{(EQ 16)}$$

Solving this equation with respect to V_y we can express V_y as a function of V_d, V_g, and U'_y:

$$V_y = V_y(V_d, V_g, U'_y) \quad \text{(EQ 17)}$$

$$= V_y\left(V_d, V_g, U_y - \left(1 + \frac{C_{ye}}{\overline{C}_{yy}}\right) \cdot V_e\right)$$

This equation does not depend explicitly on backgate voltage V_e or body charge. Instead it depends on U'_y that is a linear function of both body charge and backgate voltage. Therefore table model for V_y can be built by assuming 0 backgate voltage, varying body charge and measuring body voltage. Then this model can be used for any value of backgate voltage and body charge computing U'_y by the linear function specified in EQ3 and EQ15.

Substituting equation EQ17 into EQ10 and EQ11 we transfer equations for terminal currents and charges into functions of V_d, V_g, and U'_y only which again allows us to build the transistor model only for *0* backgate voltage and use it for all cases applying the linear function for U'_y EQ15.

The number of independent variables of the table model can be reduced even more by applying the "gate-offset-voltage concept" [5], [6]. However being constrained with very strict accuracy requirements, we selected not to implement it.

4 Organization of model tables

Transistor model is one of the most heavily used parts of circuit simulators. Accurate analytical transistor models like BSIM3SOI [8] are very complicated and rather slow. Table look up technique is the only way for significantly increased speed of transistor models. Therefore we constructed our transistor models as a set of multidimensional tables. Usually multidimensional tables are very large and require lots of memory. We developed a special technique for improving the accuracy of table models while keeping their size reasonably low. We split floating body transistor model into the part describing transistor behavior when the body is in equilibrium state with drain and source voltages and the part describing the deviation of transistor behavior from the equilibrium state. We use piece-wise polynomial approximation on non-uniform discretization grid.

4.1 Splitting model into two parts

The model of an SOI transistor with floating body consists of two sets of tables. The first set of tables describes the currents and charges of the transistor at the condition that its body is at the equilibrium state. The second set of tables describes transistor currents and charges in the general case.

The equilibrium state of the transistor is described by the following set of tables:

- $V_{y0}(V_d, V_g)$ - body voltage as a function of drain and gate voltages measured with respect to the transistor source
- $J_{c0}(V_d, V_g)$ - transistor channel current (from source to drain) as a function of drain and gate voltages measured with respect to the transistor source
- $U_{y0}(V_d, V_g)$ - normalized shifted body charge $U_{y0} = (Q_{y0} - Q_{min}) / \overline{C}_{yy}$ as a function of drain and gate voltages measured with respect to the transistor source

The state of the transistor in general case is described by the following tables:

- $\Delta V_y(V_d, V_g, \Delta U_y)$ - body voltage deviation $\Delta V_y = V_y - V_{y0}$ from its equilibrium state as a function of drain and gate voltages and the deviation of the normalized shifted body charge $\Delta U_y = U_y - U_{y0}$ from its equilibrium state
- $J_c(V_d, V_g, \Delta U_y)$ - channel current (from source to drain) as function of the same variables
- $J_y(V_d, V_g, \Delta U_y)$ - current from drain to body as function of the same variables
- $Q_i(V_d, V_g, \Delta U_y)$ - drain, gate and source charges as functions of the same variables

Splitting the table model into these two sets of tables helps to improve the accuracy of the model. The model for the case of equilibrium floating body state is only two dimensional and can be implemented more accurately. The general case has 3 dimensional tables but describes only deviations of the transistor behavior from the case of floating body equilibrium state. Even higher relative approximation error of 3 dimensional tables results in not very large total error. Therefore we can reduce accuracy requirements for 3 dimensional tables and use coarser discretization grid.

4.2 Piece-wise polynomial approximation

Piece-wise polynomial approximation provides higher accuracy both for function values and its derivatives. This also allows us to use coarser discretization grid. On the other hand piece-wise polynomial approximation requires storing several polynomial coefficients instead of one function value required by piece-wise linear approximation. The higher order of polynomial the better accuracy and the coarser grid we can use but at the cost of more memory for coefficients. In our tables we use 2-nd order polynomials for representing functions of three variables and 3-rd order polynomials for functions of two variables.

$$a_{xx}x^2 + a_{yy}y^2 + a_{zz}z^2 + a_{xy}xy + a_{xz}xz + a_x x + a_y y + a_z z + a \quad \text{(EQ 18)}$$

$$a_{xxx}x^3 + a_{yyy}y^3 + a_{xxy}x^2 y + a_{xyy}xy^2 + a_{xx}x^2 + a_{yy}y^2 + a_{xy}xy + a_x x + a_y y + a \quad \text{(EQ 19)}$$

This aligns well with higher requirements to relative accuracy of transistor model for equilibrium state and possible lower relative accuracy of the model describing deviation of the non-equilibrium state from the equilibrium one.

4.3 Nonuniform discretization

The variation range of the transistor terminal currents and charges is very high. For accurate circuit simulation it is necessary to have small relative error in current and charge approximation for all regions of voltages. Therefore to reduce the size of the model while preserving sufficient accuracy we use nonuniform discretization as shown in Figure 4. Large grid cells are used for regions of slow variation and small grid cells for regions with fast variation. The size of cells is adaptively computed at the time of transistor model characterization.

For fast access to grid cells during circuit simulation, we use multidimensional binary tree, as it is shown in Figure 4 (d) for two dimensional discretization grid. The grid has hierarchical binary structure as well. It is built from two or three dimensional rectangular domain by splitting it into pairs of equal cells as it is shown in Figure 4(b, c, d). Each splitting is independent of the previous ones. The root node of the binary tree corresponds to the whole domain. The leaf nodes correspond to the terminal grid cells. The other nodes of the tree correspond to the intermediate grid cells. Each of them specifies the direction along which a cell is split into a pair of smaller cells. Figure 5 shows the algorithm of computing approximate function value using the table model with non uniform grid and binary access tree. This algorithm requires in average *log(N)* time for accessing a cell of the discretization grid. Moreover, only small regions require more access steps.

4.4 Handling transistor width

For circuit simulation we need to model transistors of different widths. In our simulator we use two approaches. We can create individual model for each transistor width used in the circuit or we build models only for several transistor widths and use linear interpolation for the other transistor widths. The first approach is more accurate but requires more memory for transistor models and

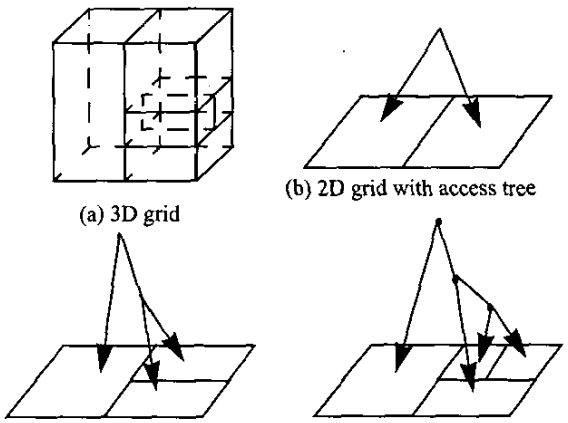


Figure 4. Construction of grid and binary access tree

Input: Values of independent variables for which we should find compute function value

Output: Value of function of the given independent variables

Procedure:

1.Traverse access tree starting from the root node:
  1.1.If the current node n_i is a leaf stop traversing
    else
  1.2.From grid cell description obtain the direction X along which the current cell is split
  1.3.Compare the input value of the variable x with its value at the middle of the current cell and select the lower level cell corresponding to the given value of variable x.
2.Read coefficients of approximation polynomial from the leaf cell description
3.Compute function value by evaluating approximation polynomial

Figure 5. Algorithm of computing function using nonuniform discretization grid

longer characterization time. Therefore it is used only for the situations that require high accuracy simulation. For the second approach we create models for widths in geometrical progression: w, kw, k^2w k^3w, and so on to minimize relative approximation error.

5 Transistor model characterization

Table transistor models are computed from accurate SPICE models. For this purposes fast transient simulator uses SPICE functions implementing accurate MOS models.

Transistor model creation consists of building non-uniform grid in the region limited by possible independent parameter variations and computing coefficients of approximation polynomial for each elementary cell of the grid. This procedure is controlled by the required accuracy of approximation. The simplified algorithms for building non-uniform grid is shown in Figure 6. The algorithm

iteratively constructs approximation polynomials for each elementary cell of the grid and checks the accuracy of the approximation. If the accuracy is acceptable the algorithm stops splitting the cell and makes it a leaf cell of the tree. Otherwise it tries to split the cell in all possible directions and selects the one that provides better accuracy. This procedure continues until the required accuracy is achieved for all cells of the grid.

The coefficients of an approximation polynomial are computed by linear least squares curve fitting. We minimize the approximation error for both the function and its derivatives because for circuit simulation accurate derivatives are as important as function values. We use the following goal function:

$$\sum\left((f-Q)^2+\sum_{x=v1,v2,v3}\Delta x\alpha_x\left(\frac{\partial f}{\partial x}-\frac{\partial Q}{\partial x}\right)^2\right) \qquad \text{(EQ 20)}$$

where:

- f is an approximating polynomial
- Q is an approximated function
- $v1$, v2, v3 are independent variables
- Δx is size of the grid cell
- α_x are weight coefficients for achieving proper relative approximation accuracy for derivatives

The summation in this formula is taken across all test points over the grid cell. For three dimensional cells we use 8 test points

Input: Function to approximate,
rectangular domain D for approximation,
acceptable approximation error
Output: Non uniform discretization grid,
approximation polynomial coefficients for each grid cell
Procedure:
1.Create empty list L of grid cells to build approximation for
2.Insert the whole domain D into list L
3.Build approximation for each cell C from the list L
3.1.Compute accurate function value at test points
3.2.Construct approximation polynomial by least squares fitting
3.3.Check polynomial accuracy
3.4.If the accuracy is acceptable, make cell C to be a leaf and remove it from list L
else
3.5.For each coordinate direction i.
3.5.1.Split cell into pair of equal cells along direction i
3.5.2.Construct approximation polynomial P_i
3.5.3.Compute accuracy of the polynomial e_i
3.6.Split cell C into C_1 and C_2 along the direction providing less approximation error e_i
3.7.Remove cell C from list L
3.8.Insert cells C_1 and C_2 into list L

Figure 6. Algorithm of constructing transistor model grid

and for two dimensional cells we use 9 test points, providing better accuracy for our two dimensional model of the transistor equilibrium state. The number of least squares equations is 3 or 4 times more than the number of test points because we fit both function values and derivatives.

6 Results

The proposed transistor table model is implemented for our fast transient simulator FSIM. FSIM is used as a fast simulation mode of our internal SPICE level simulation tool and as a fast simulation engine for our noise analysis tool [10] for simulating noise clusters. In both modes, FSIM uses accurate transistor models for constructing its table models, invoking functions of our accurate SPICE simulator. Table 1 shows comparison of accuracy and speed of our fast transient simulator using the proposed SOI transistor table models with accurate SPICE simulation on the examples of 5 industrial circuits of different size. The first and second columns provide circuit name and its number of transistors. Columns 3 and 4 give average error of delay and transition time computation. Columns 5, 6, and 7 show average error of computing maximum, average and root mean squared values of power supply current. Column 8 shows fast transient simulator speed up compared with traditional SPICE simulator. High accuracy of computing delays, transition times, and currents proves high accuracy of the proposed SOI transistor table model. Table 2 shows main characteristics of

Circuit	size (#transistors)	average error %					Speed up (times)
		delay	tr. time	vdd current			
				max	avr	r.m.s	
mux	54	2.8	2.6	1.1	0.5	0.7	22.5
csackt	130	2.5	3.6	1.6	2.0	1.5	32.8
incr	1253	4.8	1.3	5.1	2.5	4.1	59.2
comp	508	4.3	2.6	2.3	1.1	1.4	245.3
adder	751	0.9	0.9	1.5	4.1	1.9	56.5

Table 1. Accuracy and speed of fast transient simulator

table model for a typical floating body SOI transistor of 0.13 micron channel length. The model for current is made significantly

Characteristic	Table type	
	Drain current	Drain charge
Actual number of grid cells	1185	77
Equivalent uniform grid	65536*128*32	16*16*8
Nonuniform grid efficiency	226528 times	26.6 times
Access tree depth	27	11
Accuracy	< 5%	< 0.0015 fK
Table size	94,760 bytes	18,360 bytes

Table 2. Characteristics of three dimensional table model

more accurate than for charge due to the fact that transistor current variation is much more non-linear than charge and the simulator requires higher accuracy for currents as even small errors in currents accumulate in time and result in large voltage errors. The first row of the table shows number of cells of nonuniform grid. Row 2 gives the size of uniform grid with the same accuracy. Row 3 demonstrates the efficiency of using nonuniform grid with respect to uniform, showing how many times more cells are required by the uniform grid. Row 4 gives the accuracy of current and charge representation in % and fK. Row 5 presents the size of the table in bytes. From this table we see that nonuniform discretization is very efficient for achieving high accuracy. Figure 7 shows waveforms of

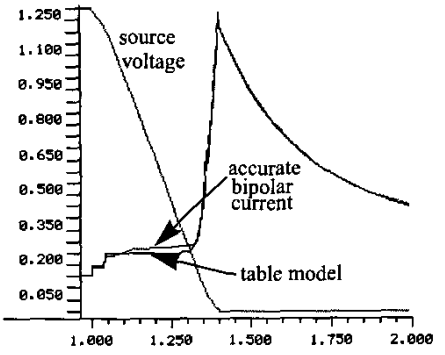


Figure 7. Waveforms of bipolar effect current simulated using accurate and table models

bipolar effect current simulated using accurate and table models. The current waveforms are almost the same. Figure 8 shows simulation of SOI history effect by accurate SPICE simulator and our fast simulator using table models. For demonstrating history effect

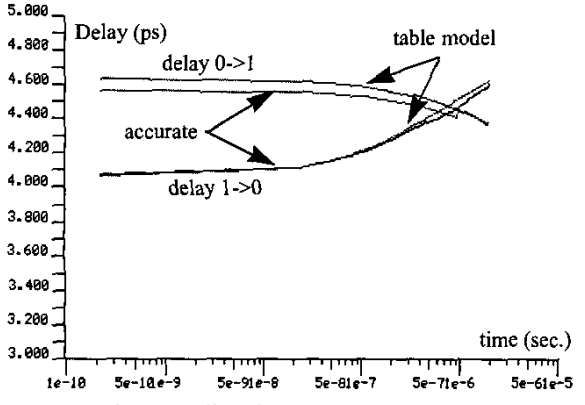


Figure 8. History effect simulated by accurate and table model simulator

a typical SOI inverter was simulated by applying 8000 short pulses (125 ps) with frequency of 4GHz to its input and measuring delay of each pulse at inverters's output. In order to emphasize delay variation the time axis is moved up by 3 ps. We see that the table based simulator accurately predicts delay variation due to inverter switching history. The maximum error for falling delay is 0.01 ps and for rising delay error is 0.06 ps. It proves that the accuracy of the proposed SOI transistor table model is enough even for such a sensitive effect.

7 Conclusion

An accurate table model for SOI transistor is proposed in this paper. The model is used for fast transistor level simulator of CMOS SOI circuits. The proposed model describes both currents and charges of an SOI transistor and is suitable for all types of SOI transistor body connections. For improving convergence of fast simulator integration algorithm, the model uses normalized shifted body charge as independent variable instead of the body potential. By applying transistor equations transformation, the number of table dimensions is reduced from 4 to 3. The model uses piecewise polynomial approximation of second and third order with nonuniform discretization grid and binary access tree. The tables approximate both the function and its first order derivatives.

Experiments carried out on large industrial circuits demonstrated high accuracy and efficiency of the proposed model in simulating SOI circuits by achieving less than 4.8% average error in delay and less than 3.6% average error in transition time. It is demonstrated that nonuniform discretization requires 226528 times less cells than uniform grid for the same accuracy.

Our current and future investigations include reduction of table dimensions from 3 to 2 at the cost of reduced accuracy by using "gate-offset-voltage concept" [5], variable accuracy for different transistor operation regions, developing extrinsic transistor model for 90nm transistors and gate leakage modeling.

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