Static Electromigration Analysis for Signal Interconnects

Chanhee Oh, David Blaauw*, Murat Becer, Vladimir Zolotov, Rajendran Panda, Aurobindo Dasgupta**

Motorola, Inc, Austin TX, *University of Michigan, Ann Arbor, MI, **Intel, Austin, TX

Abstract

With the increase in current densities, electromigration has become a critical concern in high-performance designs. Typically, electromigration has involved the process of time-domain simulation of drivers and interconnect to obtain average, RMS, and peak current values for each wire segment. However, this approach cannot be applied to large problem sizes where hundreds of thousands of nets must be analyzed, each consisting of many thousands of RC elements. In this paper, we propose a static electromigration analysis approach. We show that under conditions that are typically met by VLSI interconnects, the charge transfer through wire segments of a net can be calculated directly by solving a system of linear equations, thereby eliminating the need for time domain simulation. Also, we prove that under these conditions the charge transfer through a wire segment is independent of the shape of the driver current waveform. From the charge transfer through each wire segment, the average current is obtained directly, as well as approximate RMS and peak currents. We account for the different possible switching scenarios that give rise to unidirectional or bi-directional current by separating the charge transfer from the rising and falling transitions, and also propose approaches for modeling multiple simultaneous switching drivers. The results on a number of industrial circuits demonstrate the accuracy and efficiency of the approach.

1. Introduction and Previous Work

Wire widths have been reduced to deep sub-micron dimensions in recent years, while their currents have not been scaled proportionally. This has resulted in very high current densities in wires which has made them susceptible to electromigration failures. Electromigration is the process of metal-ion transport due to high current density stress in metal and has been studied extensively [1-3]. As the metal-ions migrate, metal buildup or depletion occurs at locations in the wires where there is a divergence in the metal-ion flux. Build up of excessive metal produces so-called hillocks which can result in shorts between wires, while excessive metal depletion can result in changes in the metal wire resistance or even catastrophic disconnections.

The failure probability of metal wires is typically characterized using test structures that are stressed with DC currents under accelerated electromigration conditions. During normal circuit operation, the signal interconnects in a VLSI design are actually stressed with pulsed DC currents, rather that with continuous DC currents. However, it has been shown that, in the absence of Joule heating, the mean time to failure of metal interconnect under pulsed DC currents can be expressed as a function of the average DC current [3][4] using Black's equation: [1],

$$t_{50} = A \cdot j_{avg}^{-n} \cdot \exp\left(\frac{Q}{kT}\right) \qquad (1)$$

where A and n are empirically determined variables, j_{avg} is the average current density, Q is the activation energy, and kT is the thermal energy. A simple approach to electromigration analysis therefore checks that each individual metal interconnect meets a specified mean time to failure. In this approach, simple design rules are formulated that express the maximum permissible DC current in a metal interconnect as a function of the metal wire width. Although this approach is commonly used in industry, it does not consider the failure probability of the interconnect system as a whole. Therefore, a so-called statistical electromigration budgeting (SEB) [5] approach has also been proposed. In this model, the expected lifetime of the overall system of interconnects is determined from the failure probability of the individual wire segments. In either approach, the electromigration computation requires knowledge of the *average* or *DC* current in each metal interconnect. This current can be obtained by performing a time domain simulation of a transition of an interconnect and integrating the current through the interconnect over the simulation time, as follows:

$$I_{dc} = \frac{s}{T}\int_0^T i(t)dt \qquad (2)$$

where T is the clock cycle period, $i(t)$ is the time varying current, and the switching factor s represents the average number of times that a signal net is expected to transition in a clock period.

In addition to DC current stress induced failure, interconnect can also fail due to excessive Joule heating. High currents in a metal interconnect can generate significant heat due to resistive energy dissipation of the wire and such Joule heating was found to be a function of the RMS and peak currents in a wire segment. Typically, metal failure due to Joule heating is checked using simple RMS and peak current limits. The RMS current, needed for Joule heating checks, is computed as follows:

$$I_{RMS} = \sqrt{\frac{s}{T}\int_0^T i^2(t)dt} \qquad (3)$$

The peak current is simply the maximum current at any point in time during the signal transition.

A current is said to be *unidirectional* if it flows in the same direction through a metal segment during both the rising and falling transition of the signal as shown for segment x in Figure 1. In this case, the I_{dc} current value is non-zero and the likely failure mechanism will be due to DC current stress. On the other hand, if the current flows in one direction during the rising transition and in the other direction during the falling transition, the current is said to be *bi-directional*, as for example the current through segment y in Figure 1. For this wire segment, I_{dc} is close to zero and the likely failure mechanism is due to Joule heating. In this case, the I_{rms} and I_{peak} currents will determined the lifetime of the segment. Of course, a wire segment may have both significant I_{dc} and I_{rms}/I_{peak} under different driver configurations. In general, the current limits
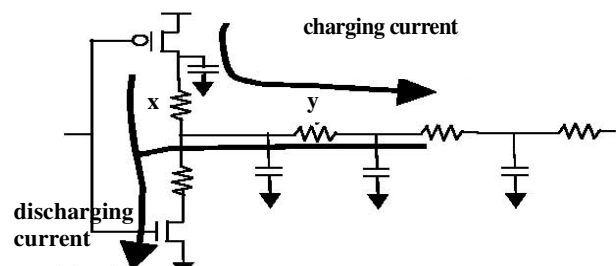

Figure 1. Unidirectional and bidirectional current flow

for I_{rms} and I_{peak} are much higher than for I_{dc}, and therefore, failure due to Joule heating is much less common in a design. Hence, the accuracy required of the I_{rms} and I_{peak} current calculation is lower than that for I_{dc}.

A dynamic approach to circuit-level electromigration analysis uses simulation of the interconnect with a Spice-level simulation tool to obtain time-varying current waveforms for each interconnect segment, based on which, average, RMS and peak current values are easily computed. These tools incorporate detailed electromigration models and compute the electromigration degradation level of the design. The SPIDER [9] and BERT [10] tools are based on Spice-level simulation. The iTEM tool [8] is based on a fast transistor level simulator using piece-wise quadratic transistor models and also accounts for Joule-heating. The tool presented in [11] is based on an approximate timing simulator. These approaches, however, are limited in that they only apply to small circuit structures. A number of methods for filtering out nets from the analysis using a conservative criteria have been proposed. In [7], a filtering methodology using the so-called 'critical threshold' due to stress induced backflow is presented, and in [6] an approach based on lumped capacitance approximations is proposed. However, for large microprocessors, hundreds of thousands of nets must be analyzed, each consisting of many thousands of RC elements. Therefore, even after filtering small nets with a conservative filtering criteria, the remaining critical nets will be to numerous to allow Spice-level simulation. Note also that reduced-order modeling techniques cannot be used for electromigration analysis, since the currents for each element in the net list must be obtained individually.

The analysis is further complicated by the fact that each signal net often has multiple drivers. In order to determine the worst-case driver transition, a dynamic simulation based approach must simulate all possible rising and falling driver transition combinations (called *switching scenarios*) for an interconnect, and incurs a high run time cost. It also requires the user to perform the laborious and error-prone task of writing simulation vectors.

In this paper, we propose a new static approach for electromigration analysis for large circuits. We compute the average, RMS and peak currents for each metal interconnect statically, without requiring the specification of simulation vectors. First, we prove that under conditions that are typically met by VLSI interconnects, the charge transfer through interconnect elements can be expressed as a set of linear equations derived directly from the nodal formulation of circuit. Hence, we can compute the exact charge transfer through all interconnect elements by solving a single system of linear equations, avoiding time-consuming time domain simulation which has typically been used [6]. We also prove the important property that for a linear circuit, the charge transfer through an element is dependent only on the total charge conducted from the driver circuit(s) and does not dependent on the shape of the driver current. From the charge transfer through a wire segment, we directly obtain the exact I_{dc} current value. We also propose methods for finding approximate I_{rms} and I_{peak} currents based on the charge transfer of the signal net and show how the proposed method can be used in the presence of multiple simultaneous acting drivers.

Finally, we show how different switching scenarios are efficiently evaluated by separating the charge transfer for the rising and falling transitions of the net. This allows the computation of the worst-case current values among all switching scenarios in a time linear with the number of independently-controllable drivers. The proposed algorithms were implemented in an industrial electromi-

gration analysis tool. We demonstrate the accuracy of the proposed approach by comparing the analysis results with Spice simulations. We also show the efficiency of the analysis for a number of large blocks, including a large processor core.

The remainder of this paper is organized as follows. Section 2 presents the new linear system formulation for directly calculating charge transfer. Section 3 presents the approach for finding the worst current values among all switching scenarios. Section 4 presents our results and in Section 5 we draw our conclusions.

2. Calculation of the Charge Transfer

In this Section, we present a formal derivation of the charge transfer and the conditions under which it can be obtained by solving a simple system of linear equations. We consider a general interconnect circuit with nodes $N = \{n_1, \ldots n_m\}$, resistors r_{ij} and capacitors c_{ij} connected between nodes n_i and n_j and one or more driving gates and load gates. Each resistor in the network represents a metal segment or a via between metal layers. Each capacitor represents a load or self-loading of the interconnect, including possible self-coupling capacitors or capacitors in series. The resistors and capacitors are extracted using an extraction tool. A simple example circuit is shown in Figure 2(a). Our goal is to find the net amount of charge

(a)

(b)
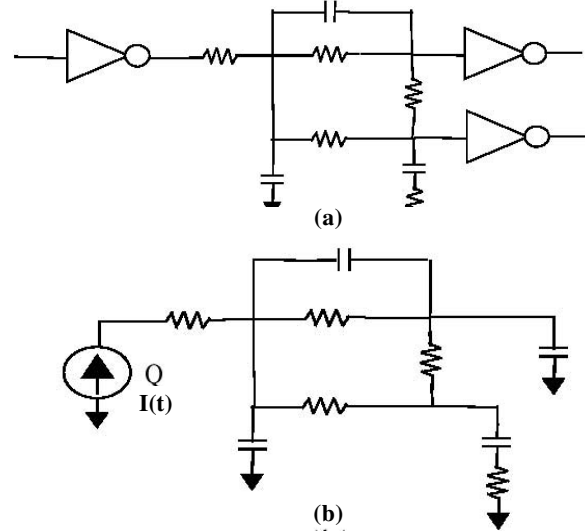
Figure 2. Circuit and linear model for electromigation analysis

that is transferred through each metal segment or resistor in the interconnect during either a rising or falling transition of the net, which we refer to as the *charge transfer q_{ij}*. It is clear that the charge transfer is simply the integral of the current $i_{ij}(t)$ through an element over time as defined below.

Definition 1. The charge transfer q_{ij} though a resistor r_{ij} connected between nodes i and j is:

$$q_{ij} = \int_{t=0}^{\infty} i_{ij}(t)dt \qquad (4),$$

where $i_{ij}(t)$ is the time varying current through resistor r_{ij}.

To calculate the charge transfer q_{ij} without performing a time domain simulation, we first construct a linearized version of the circuit, as shown in Figure 2(b), by replacing the load gates with capacitors and the driver gate(s) with time varying current sources $I(t)$, such that the behavior of the circuit is unchanged. In other words, the current $I(t)$ is exactly equal to the current produced by the driver gate at each point in time and therefore mimics the driver

perfectly without changing the behavior of the circuit. Note that although the example in Figure 2(b) has only one driver, in general a circuit may have multiple simultaneous switching drivers. After linearizing the circuit, we can represent it with the following standard nodal differential equation:

$$GV(t) + C\dot{V}(t) = I(t) \qquad (5),$$

where G is the conductance matrix, C is the capacitance matrix, $V(t)$ are the node voltages and $I(t)$ are the current sources corresponding to the driving gates. We now define the following two useful voltages.

Definition 2.

$$v_i^\infty = \lim_{t \to \infty} v_i(t) \qquad (6)$$

$$v_i^0 = v_i(0) \qquad (7)$$

Voltage v_i^0 is the voltage at node i at the start of the transition, and

v_i^∞ is the steady-state voltage at node i after the transition is completed. We now observe that for all signal interconnects that are of interest to us, there is no DC path from the signal net to the power supply or ground. This means that at the end of the transition, when the driver gate has reached its steady-state voltage, there is no current through any of the resistors in the circuit. We therefore restrict ourselves to circuits that meet the following condition:

Condition 1. If in the circuit two nodes i and j exist, such that $v_i^\infty \ne v_j^\infty$, then the conductance $g_{ij} = 0$.

VLSI interconnect circuits satisfy condition 1, since there is no current from the driver gate at the end of the transition when the circuit reaches a stable state. This means that the charge transfer from a driver gate d to the interconnect is finite and is calculated as follows:

$$Q_d = \int_{t=0}^{\infty} I_d(t)dt \qquad (8),$$

where Q_d is the *driver charge transfer*, and $I_d(t)$ is the driver gate current as a function of time. In the Section below, we show how to compute the charge transfer through a wire based on the driver charge transfer Q. Then in the subsequent Section, we discuss methods to compute the driver charge transfer.

2.1 Wire Charge Transfer Formulation

In the following Theorem and proof, we show that the charge transfer q_{ij} through a wire segment can be computed by solving a single system of linear equations formulated using the driver charge transfer Q_d, without knowledge of the time varying behavior of the driver currents $I_d(t)$.

Theorem 1. Given a linear circuit that satisfies condition 1, and the following linear system of equations:

$$G\hat{W} = Q - C(V^\infty - V^0) \qquad (9)$$

where Q is the vector of driver charge transfer (8), G is the conductance matrix, C is the capacitance matrix, and V^0 and V^∞ are the vectors of initial and final node voltages (6) and (7), then, the charge transfer q_{ij} through element r_{ij} is defined as follows:

$$q_{ij} = g_{ij}(\hat{w}_j - \hat{w}_i) \qquad (10)$$

This theorem therefore states that if we solve the linear system (9) for $\hat{W}$, we can directly calculate the charge transfer through an

element r_{ij} as the difference of the $\hat{w}$ at the two nodes of n_i and n_j multiplied by the conductance of r_{ij}. As shall be come clear, $\hat{w}_i$ can be thought of as the area under the voltage curve of node n_i relative to its final voltage v_i^∞ and $\hat{W}$ is the vector of such voltage areas for all nodes.

Proof. We define $w_i(t)$ as the difference between the voltage value $v_i(t)$ at node i and its stable, final value v_i^∞:

$$w_i(t) = v_i(t) - v_i^\infty \qquad (11)$$

We then substitute the voltage vector $V(t)$ in the first term of the system of nodal equations (5) with $W(t) + V^\infty$ and obtain the following linear system of equations:

$$GW(t) + GV^\infty + C\dot{V}(t) = I(t) \qquad (12)$$

Since G is a conductance matrix, for every row i the matrix/vector multiplication GV^∞ can be expressed as $\sum_j (g_{ij}v_j^\infty - g_{ij}v_i^\infty)$. From Condition 1 it follows that all terms in this summation are zero, since either $g_{ij} = 0$ or $v_j^\infty - v_i^\infty = 0$ and therefore $GV^\infty = 0$. After simplifying (12) accordingly and then integrating over time, we obtain:

$$\int_{t=0}^{\infty} GW(t)dt + \int_{t=0}^{\infty} C\dot{V}(t)dt = \int_{t=0}^{\infty} I(t)dt \qquad (13),$$

and examine each term in turn below:

1. For the first term, $\int_{t=0}^{\infty} GW(t)dt$, we define a new variable $\hat{w}_i = \int_{t=0}^{\infty} w_i(t)dt$. Since the node voltages w_i are exponential decaying functions of time, the integral $\hat{w}_i$ is finite and therefore the first term becomes

$$\int_{t=0}^{\infty} GW(t)dt = G\hat{W} \qquad (14).$$

2. For the second term, we get the following:

$$\int_{t=0}^{\infty} C\dot{V}(t)dt = C(V^\infty - V^0) \qquad (15).$$

3. Finally, for the third term, we get:

$$\int_{t=0}^{\infty} I(t)dt = Q \qquad (16), \text{ which is the same as (8).}$$

From (14), (15) and (16) we obtain: $G\hat{W} = Q - C(V^\infty - V^0)$, where we solve for $\hat{W}$. At the same time, from (1) and (8) we obtain:

$$\int_{t=0}^{\infty} g_{ij}(v_j - v_i)dt = \int_{t=0}^{\infty} (g_{ij}(w_j - w_i) + g_{ij}(v_j^\infty - v_i^\infty))dt$$

From condition 1 it again follows that $g_{ij}(v_j^\infty - v_i^\infty) = 0$, and therefore, $q_{ij} = g_{ij}(\hat{w}_j - \hat{w}_i)$ which proves the theorem. $\square$

Note that Theorem 1 is completely general and holds for any number of current sources and all types of capacitors, including coupling capacitors and capacitor dividers, provided Condition 1 holds. As formulated, the linear system (9) will be singular in that

IEEE
COMPUTER
SOCIETY

the values $\hat{w}_i$ can have an arbitrary offset for each set of nodes belonging to a DC-connected component (DCCC). Each DCCC is only connected to "charge" sources, such that the sum of the total charge injected into and out of the DCCC is zero. Therefore, the values $\hat{w}_i$ of the nodes of the DCCC can have an arbitrary offset, which leads to a singularity of the matrix. This problem can be easily remedied by setting one of the nodes in each DCCC in the system as a reference. Since q_{ij} in (10) depends only on the difference of $\hat{w}$ between two nodes, the reference node in a DCCC and its value do not affect the value of q_{ij} and can be arbitrarily chosen.

From (9) and (10) we can observe that q_{ij} is independent of the shape of the current waveform $I_d(t)$, and is only dependent on its total charge Q_d. We therefore have the following Corollary:

Corollary 1: For a linear circuit satisfying Condition 1, and having one or more current sources $I_d(t)$, all current source waveforms $I_{d,j}(t)$ with total driver charge transfer Q_d will result in the same charge transfer for each element in the circuit.

2.2 Wire Charge Transfer Computation

Based on Theorem 1, we propose the procedure shown below in Procedure 1 for calculating the charge transfer through all wire segments of a signal interconnect. Assume we have one or more driver gates d, switching from an initial voltage v_d^0 (typically, but not necessarily, GND or VDD) to a final voltage v_d^∞.

Procedure 1:

1. Compute the voltage v_i^0 at node n_i at the start of the transition by setting the voltage at the output of the drivers d to v_d^0 and performing a DC solution.

2. Compute the voltage v_i^∞ at node n_i at the end of the transition by setting the voltage at the output of the drivers d to v_d^∞ and performing a DC solution.

3. Compute the driver charge transfer Q_i for each simultaneous switching driver, as explained in the next Section.

4. Form the linear system (9), set one node in each dccc to zero to avoid singularity, and solve for $\hat{w}$.

5. For each element in the circuit, compute q_{ij} using (10).

The above procedure requires a DC solution in Steps 1 and 2. Due to condition 1, there is no current through any resistor in Step 2 and the DC solutions becomes trivial through shorting resistors and removing capacitors. In most cases, the DC solution in Step 1 is similarly trivial. Step 4 requires one linear solution. However, since G is a sparse matrix, $\hat{w}$ can be computed very efficiently, even for very large circuits. Therefore, the overall computation of the charge transfer is extremely efficient, compared to performing a non-linear simulation of the original circuit (such as shown in Figure 2(a)), while the accuracy of the analysis is not compromised.

2.3 Driver Charge Transfer Computation.

Step 3 in the above procedure requires that the total charge transfer from each switching driver is known. If there is only a single driver, its charge transfer Q can be computed through charge conservation from the charge transfer through each of the capacitors:
However, if there are multiple drivers that switch at the same time,

$$Q = \sum_{i=1}^{m} \sum_{j=i+1}^{m} c_{ij}((v_j^\infty - v_i^\infty) - (v_j^0 - v_i^0)) \qquad (18)$$

as is often the case, then this total charge Q is divided between these drivers in some manner: $Q = \sum_d Q_d$. In Figure 3(a), we show an example of a 2-input NOR gate and the associated linearized circuit, where the n-type transistors are folded in the layout. The n-type transistors connected to input b are off and can be modeled as capacitive loads. When input a switches high, its two NMOS transistors turn on, while its PMOS transistor turns off. We therefore model these three transistor connections with current sources and need to determine their charge transfer Q_d as shown in Figure 3(b).

We propose two approaches for determining the charge transfer distribution between multiple simultaneous switching drivers. The most accurate approach is to perform a non-linear simulation of the gate, with a pi-model [12] representing the interconnect loading. During the non-linear simulation, we compute the integral of the current through each driver output to obtain its charge transfer which is then used in Step 4 of Procedure 1. Although this requires a non-linear simulation of the transistors, this simulation is relatively fast since it involves only a small number of non-linear device belonging to the driver gate and a small pi-model representing the entire interconnect.

A faster, more approximate approach that avoids this non-linear simulation makes the simplifying assumption that the short-circuit current is negligible (meaning $I_3(t) = 0$ in the example in Figure 3(b)). We then divide the total charge Q computed through charge conservation (18) between the remaining current sources according to their transistor sizes: $Q_d = Q \cdot \dfrac{W_d}{\sum_i W_i}$, where W_i is the size of transistors i and W_d is the size of the transistor for which we are computing the charge transfer Q_d. This simple approach, although not exact, was found to yield results with less than 3% error in practice, as shown in Section 4. This is due to the fact that
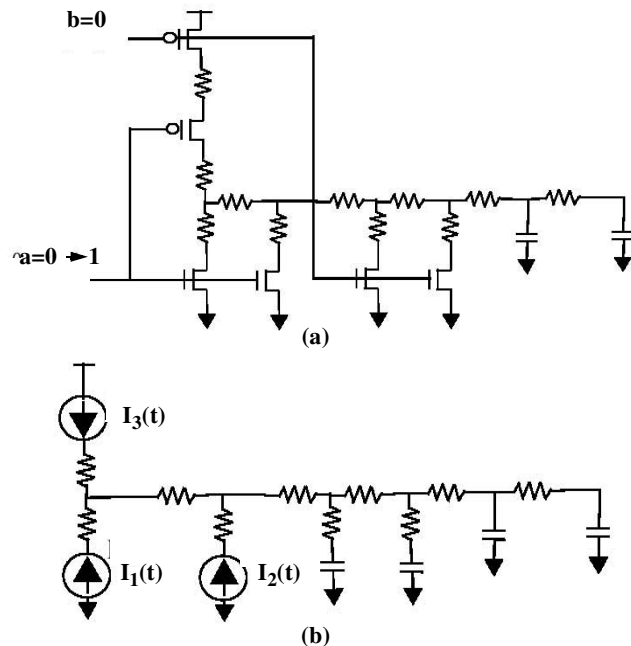

(a)

(b)

Figure 3. Linear model of interconnect driven by a gate.

the simultaneous switching drivers are, most often, different fingers of a folded device that have identical structure and inputs.

3. Average, RMS and Peak Current

In the previous Section we presented an approach to efficiently compute the charge transfer through a wire segment in response to a rising or falling transition. In this section, we show how to use the charge transfer computation to determine the worst-case average, RMS, and peak currents for a metal segment. In order to guarantee a repeatable transition pattern, we base our worst-case current calculation on the maximum charge transfer during two clock periods where the first period contains a rising or charging transition of the interconnect and the second period contains a falling or discharging transition. Two problems need to be addressed: First, given a particular charging and discharging driver pair we need to compute I_{dc}, I_{rms}, and I_{peak} from the charge transfers. Second, among all possible charging and discharging driver combinations, we need to determine the worst-case pair for each type of current in a metal segment.

In order to efficiently approach this problem, we separately record the charge transfer for rising and falling transitions through an interconnect. The drivers connected to the interconnect are divided into clusters of simultaneously switching drivers, where each cluster is assumed to be independently controllable. Each cluster is simulated in turn for both rising and falling transitions, while recording the minimum and maximum charge transfer in each direction through an interconnect element. The procedure is shown below:

Procedure 2:
1. For all wire segments define a reference direction.
2. For (all driver clusters) {
3.   For (each driver d in a driver cluster) compute *charging* driver charge transfer Q_d.
4.   Compute charge transfer through each wire segment using Procedure 1.
5.   For (all wire segments i)
6.   If (charge transfer is in reference direction) update *max $Q^f_{i,charge}$* and *$minQ^f_{i,charge}$*
7.   else update *$maxQ^r_{i,charge}$* and *$minQ^r_{i,charge}$*
8.   Repeat for discharging transition and update *$maxQ^f_{i,discharge}$*, *$minQ^f_{i,discharge}$* or *$maxQ^r_{i,discharge}$*, *$minQ^r_{i,discharge}$*
9. }

Note that these charge transfers are unsigned quantities and equal to zero if no transfer exists in the specified direction. Also, each charge transfer quantity can be associated with a different driver. Since we simulate each drive only twice (once for the rising transition and once for the falling transition of the net), the run time complexity is linear with the number of drivers. Based on the maximum and minimum charge transfer in each direction through a wire segment for both rising and falling transitions, we now calculate the average, RMS, and peak currents, as shown below:

1) Average current:

The average current is defined in equation (2): $I_{dc} = \frac{s}{T}\int_0^T i(t)dt$, where s is the switching factor and T is the clock period. Typically, the switching factor is obtained from simulations with a cycle based simulator, or through propagation of switching probabilities in the circuit. We evaluate I_{dc} over two clock

periods - one with a rising, and one with a falling transition. If there is non-zero charge transfer in a particular direction for both the rising and the falling transitions, the worst-case charge transfer is the sum of both these maximum charge transfers. If there is a zero charge transfer for either rising or falling transition in this direction, the worst-case charge transfer is the maximum charge transfer in that direction subtracted with the minimum charge transfer in the opposite direction. We divide the worst-case charge transfer by 2 to account for the two transition periods and account for the clock period T as follows:

Procedure 3:
1. if ($maxQ^f_{i,charge} > 0$ && $maxQ^f_{i,discharge} > 0$)
   $$maxQ^f_i = maxQ^f_{i,charge} + maxQ^f_{i,discharge}$$
2. else $maxQ^f_i$ = Max (($maxQ^f_{i,charge} - minQ^r_{i,discharge}$), ($maxQ^f_{i,discharge} - minQ^r_{i,charge}$))
3. if ($maxQ^r_{i,charge} > 0$ && $maxQ^r_{i,discharge} > 0$)
   $$maxQ^r_i = maxQ^r_{i,charge} + maxQ^r_{i,discharge}$$
4. else $maxQ^r_i$ = Max (($maxQ^r_{i,charge} - minQ^f_{i,discharge}$), ($maxQ^r_{i,discharge} - minQ^f_{i,charge}$))
5. $maxQ_i = $ Max($maxQ^f_i$, $maxQ^r_i$)
6. $I_{i,dc} = s/(2T)\ maxQ_i$

2) RMS and Peak current:

The RMS current of a wire segment is defined with the integral

(3): $I_{RMS} = \sqrt{\frac{1}{T}\int_0^T i^2(t)dt}$, and hence requires information about

the waveform shape of the time varying current $i(t)$ and not only the total charge transfer. In our approach, we analytically estimate the RMS current by approximating the waveform $i(t)$ with a triangular waveform with identical rise and fall times. The charge transfer $maxQ_{charge}$ is defined as the maximum rising/falling charge transfer in either direction: $maxQ_{charge} = $ Max ($maxQ^f_{charge}$, $maxQ^r_{charge}$) and $maxQ_{discharge} = $ Max ($maxQ^f_{discharge}$, $maxQ^r_{discharge}$). The transition time Tr is the duration of the current pulse for the transition and corresponds to the transition time of the signal. Without a transient simulation of the entire interconnect, we can not obtain the exact width of the triangular current waveform Tr at each resistor. In our approach, we use the transition time at the output of the driver as an approximation of the transition time at all the wire segments. Since the transition time at the wire segments will be larger than that at the driver output, our estimation of peak and RMS current will tend to err on the side of pessimism. The transition time at the driver output can be obtained from a static timing analyzer or through non-linear simulation of the driver gate using a pi-load model. Given Tr, we calculate the peak and RMS current under the triangular current waveform assumption analytically as follows:

$$I_{rms,charge} = \sqrt{\frac{s}{T}\cdot 2\int_0^{\frac{Tr}{2}} (4maxQ_{charge}/Tr^2)tdt} =$$

$$\sqrt{\frac{4s(maxQ_{charge})^2}{3T_rT}}$$

$$I_{peak,charge} = \frac{2maxQ_{charge}}{T_r}$$

For the falling transition, the peak and RMS currents $I_{peak,discharge,}$

and $I_{rms,discharge}$ are calculated separately using *maxQdischarge*. The total peak and RMS currents are computed as follows:

$$I_{peak} = Max[I_{peak,charge}, I_{peak,discharge}]$$

$$I_{rms} = \sqrt{\frac{1}{2}(I^2_{rms,charge} + I^2_{rms,discharge})}$$

After the average, RMS and peak currents for all wire segments are computed, the electromigration analysis is performed using either simple current limit checks, or using statistical electromigration budgeting [5].

4. Result

The proposed electromigration analysis approach was implemented in an industrial electromigration checker and was applied on a number of industry circuit designs. A commercial extraction tool was used to extract parasitic RC data including the metal width and layer information and the electromigration analysis tool is applied on this data without performing reduction on the RC data.

Table 1 shows the accuracy of our current calculation by compar-

Element	Spice (mA)			Proposed Static Approach (mA)		
	I_{dc}	I_{rms}	I_{peak}	I_{dc} (%error)	I_{rms} (%error)	I_{peak} (%error)
R1	0.19	0.50	1.38	0.19 (0.0%)	0.43 (-14.0%)	1.46 (8.7%)
R2	0.06	0.15	0.41	0.06 (0.0%)	0.13 (-13.3%)	0.44 (2.4%)
R3	0.17	0.44	1.23	0.17 (0.0%)	0.39 (-2.3%)	1.32 (7.3%)
R4	0.08	0.20	0.56	0.08 (0.0%)	0.17 (-15.0%)	0.59 (5.6%)
R5	9.15	23.24	68.38	9.34 (2.1%)	21.29 (-8.4%)	72.78 (6.4%)
R6	5.30	13.52	39.80	5.44 (2.6%)	12.38 (-8.4%)	42.34 (6.4%)
R7	1.53	3.89	11.40	1.56 (1.9%)	3.56 (-8.5%)	12.20 (7.0%)
R8	3.94	9.99	19.43	4.01 (1.8%)	9.16 (-8.3%)	31.31 (6.1%)
R9	0.35	0.90	2.58	0.34 (-2.9%)	0.79 (-12.2%)	2.69 (4.3%)
R10	0.05	0.12	0.35	0.05 (0.0%)	0.10 (-16.7%)	0.35 (0.0%)

Table 1. Comparison of proposed approach with Spice simulation for wire segments of industrial interconnects

ing it to the result obtained from explicit transient simulations of the interconnect and driver gates using Spice for several large industrial signal net. Our approach estimates average current with a maximum error of 2.9%. Since the formulation for charge transfer is exact, the observed deviation is due to error in the modeling of the gate loads with linear capacitors and the distribution of charge transfer between the driver gates. Our approach for RMS and peak current has a maximum error of 16.7% and 8.7% respectively. This error is primarily due to the fact that the actual current waveform is not precisely triangular. However, the observed error is well within the required accuracy for an industrial electromigation analysis tool.

Table 2 shows statistics from our analysis on several circuit designs. Due to the number of nets, the number of R/C elements, and the number of possible drivers, it would be impractical to apply simulation based approaches. The proposed approach successfully analyzed these circuits with very modest run time. Note that in order to demonstrate the efficiency of the proposed approach, a detailed analysis is performed on all the nets in the design and no nets were filtered from the analysis.

5. Conclusion

In this paper, we have proposed a static electromigration analysis approach. We showed that the charge transfer through wire segments of a net can be calculated directly by solving a linear system,

circuit	#nets	Total #RC elem.	Largest net		max # drivers	run time (min)
			#R	#C		
Arith	622	73K	347	1,820	38	1.8
Add1	1,923	268K	10,014	29,840	1,088	8.5
Dp1	2,104	319K	10.287	19,624	799	5.0
Add2	4,172	606K	22,294	67,710	2,384	14.8
Dp2	4,598	636K	18,245	46,795	1,509	20.0
uPcore	295K	21.3M	3,766	6,629	511	21.7h

Table 2. Run time statistics on example circuits.

derived from the nodal formulation of the circuit. We avoid the need for time consuming time domain simulation. We showed how average, RMS, and peak current values for each wire segment can be obtained using the computed charge transfer. We also account for the different possible switching scenarios that give rise to unidirectional or bi-directional current by separating the charge transfer from the rising and falling transitions. We implemented the proposed static analysis approach in an industrial electromigration analysis tool that was used on a number of industrial circuits, including a large processor core. Experimental results were presented to demonstrate the accuracy and efficiency of the approach.

REFERENCES

[1] J. R. Black, "Mass transport of aluminum by momentum exchange with conduction electrons," Proc. IEEE International Reliability Physics Symposium, pp. 148-159, 1967

[2] L. Ting, J. May, W. Hunter, and J. McPherson, "AC electromigration characterization and modeling of multilayered interconnects," Proc. IEEE Int. Reliability Physics Symposium, 1993.

[3] J. M. Towner, E. P. van de Ven, "Aluminum electromigration under pulsed dc conditions," Proceedings IEEE International Reliability Physics Symposium, pp. 36-39, 1983

[4] J. A. Maiz, "Characterization of electromigration under bidirectional and pulsed unidirectional currents", in Proc. IEEE Int. Reliability Physics Symposium, 1988, pp. 220-228.

[5] J. Kitchin, "Statistical electromigration budgeting for reliable design and verification in a 300-MHz Microprocessor," Proceedings Symposium on VLSI Circuits, pp. 115-116, 1995.

[6] S. Rochel, G. Steele, J. Lloyd, S. Hussain, and D. Overhauser, "Full-Chip reliability analysis," Proceeding IEEE International Reliability Physics Symposium, pp. 356-362, 1998

[7] J. J. Clement, S. P. Riege, R. Cvijetic, C. V. Thompson, "Methodology for electromigration critical threshold design rule evaluation," IEEE Trans on CAD, Vol 18, May, pp. 576-581, 1999

[8] C. C. Teng, Y.-K. Cheng, E. Rosenbaum, S.-M. Kang, "iTEM: A temperature-dependent electromigration reliability diagnosis tool," IEEE Trans. on CAD, Vol. 16, pp. 882-893, Aug. 1997

[9] J. E. Hall, D. E. Hocevar, P. Yang, and M. J. McGraw, "SPIDER – A CAD system for modeling VLSI metallization patterns," IEEE Trans. on CAD, pp. 1023-1031, Nov, 1978

[10] R. H. Tu, E. Rosenbaum, W. Y. Chan, C. C. Li, E. Miami, K. Quader, P. K. Ko, and C. Hu, "Berkeley reliability tools – BERT," IEEE Trans on CAD, pp. 1524-1534, Oct 1993.

[11] D. Frost and K. F. Poole, "RELIANT: A reliability analysis tool for VLSI interconnects," IEEE J. Solid-State Circuits, 1989.

[12] J. Qian, S. Pullela and L. T. Pillage, "Modeling the effective capacitance for the RC interconnect of CMOS gates," IEEE Trans. Computer-Aided Design, pp. 1526-1555, 1994.

COMPUTER SOCIETY