Efficient Crosstalk Noise Modeling Using Aggressor and Tree Reductions *

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ABSTRACT

This paper describes a fast method to estimate crosstalk noise in the presence of multiple aggressor nets for use in physical design automation tools. Since noise estimation is often part of the inner-loop of optimization algorithms, very efficient closed-form solutions are needed. Previous approaches have typically used simple lumped 3-4 node circuit templates. One aggressor net is modeled at a time assuming that the coupling capacitances to all quiet aggressor nets are grounded. They also model the load from interconnect branches as a lumped capacitor and use a dominant pole approximation to solve the template circuit. While these approximations allow for very fast analysis, they result in significant underestimation of the noise. In this paper, we propose a new and more comprehensive fast noise estimation model. We use a 6 node template circuit and propose a novel reduction technique for modeling quiet aggressor nets based on the concept of coupling point admittance. We also propose a reduction method to replace tree branches with effective capacitors which models the effect of resistive shielding. Finally, we propose a new double pole approach to solve the template circuit. We tested the proposed method on noise-prone interconnects from an industrial high performance processor. Our results show a worst-case error of 7.8% and an average error of 2.7%, while allowing for very fast analysis.

1. INTRODUCTION

Crosstalk noise between signal wires has become a major source of failures in modern high-performance VLSI systems [1]-[2]. Due to the aggressive interconnect scaling in the lateral dimensions with relatively unchanged vertical dimensions, the coupling capacitance among adjacent wires can be significantly larger than wire ground capacitance. In such strongly coupled systems, the state of a wire strongly depends on the states of its neighboring wires. The switching of a first net, referred to as the aggressor net, may affect the state of a second nearby net, referred to as the victim net.

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The coupling among adjacent wires has made it necessary to analyze a victim net together with all its coupled aggressor nets. However, efficient and accurate analysis of the coupling noise is difficult because, 1) the number of coupling nets is typically large and, 2) the aggressor and victim nets may have a large number of branches. Crosstalk noise modeling approaches in literature can be loosely classified into two categories based on their trade-off between accuracy and efficiency. The first class of methods aims to achieve maximum modeling accuracy while gaining substantial speedup over standard SPICE simulation. A number of methods use linear model order reduction techniques [3]-[5] to reduce the original large but sparse matrix to a much smaller and denser matrix which is then used as a macromodel for crosstalk simulation. These methods are useful for post-layout verification where high accuracy is a key requirement and they enable the analysis of large industrial designs in a matter of hours [6], [7].

However, in deep submicron VLSI chip designs, there is often the need to assess and avoid crosstalk noise in the early stages of the chip design flow. Therefore, the second class of crosstalk noise modeling methods aims to further improve the efficiency of noise analysis, such that they can be used in the inner-loop of physical design automation tools. These methods [8]-[10] reduce the interconnect topology into a very simple template circuit with a known and fixed topology. The simple template circuit is then analytically modeled leading to an analysis efficiency that is another several orders of magnitude faster than model order reduction based methods. The approaches proposed in this paper address this second class of crosstalk noise modeling methods.

Since the number of aggressor nets to a victim net is potentially large, it is very difficult to properly align the switching times in order to generate the worst-case noise [11], [12]. A common approach uses the superposition law to estimate crosstalk noises. To compute the worst-case crosstalk noise of an N-aggressor system, it is necessary to calculate the crosstalk noise of an N+1-net system N times. Most previous approaches have further assumed that coupling capacitances from the victim net to non-switching or quiet aggressor nets are grounded during superposition. This reduces the network from N+1 nets to only two nets, and hence, the maximum crosstalk noise can be calculated in linear time with respect to the number of aggressors N. However, during superposition, the quiet aggressor nets follow the victim net waveform to a certain extent and their effective load capacitance is always less than the coupling capacitance value. By using grounded coupling capacitance, these methods have therefore improved the efficiency of the analysis while potentially underestimating the crosstalk noise.

Similarly, the techniques used in literature for fast crosstalk noise estimation do not consider the effect of resistive shielding of long interconnects. They typically lump the total wire and load capac-

itances of a branch at the branching point to simplify the circuit. This results in an underestimation of crosstalk noise. Finally, previous methods use 3-4 node template circuits which are solved using a dominant pole approximation. We will show that the inability of the template circuit to model the resistance of the switching aggressor and the dominant pole approximation further compromise the accuracy of the existing fast noise analysis methods.

In this paper, we present an efficient crosstalk noise estimation framework which maintains the efficiency of past approaches, but significantly improves on their accuracy. We propose novel quiet aggressor net and tree branch reduction technique which models them with effective load capacitances. Formulas are derived to calculate the values of these effective capacitances using coupling-point and branching-point admittance together with approximate waveforms at the coupling and branching points. In order to model the resistance of the switching aggressor net, we use a 6 node template circuit, which significantly enhances the accuracy of the noise estimation. To solve this more complex template circuit, we propose a new double pole method and confirm its accuracy compared with SPICE simulation. Experimental results on industrial nets demonstrate that the proposed methods significantly enhance the accuracy of the noise estimation and eliminates the tendency of prior methods to underestimate the noise level. At the same time, the proposed method maintains the efficiency of previous methods and is linear in run time with the number of aggressor nets.

The rest of the paper is organized as follows. Section 2 explains the overall framework of the proposed noise estimation methodology. In Section 3, we introduce quiet aggressor net reduction and tree branch reduction techniques based on point admittance matching. The reduced circuit is then analyzed in Section 4, where we proposed the double pole model for efficient yet accurate noise calculation. And in Section 5, we present results of proposed methodology on industrial circuits.

2. METHODOLOGY

The basic idea of the proposed method is first to reduce a large crosstalk network into a simple template circuit. The template circuit is then solved analytically. The flowchart of the reduction scheme is illustrated in Figure 1. First, we apply the tree reduction operation on each aggressor net. Second, we apply quiet aggressor net reduction operation on each of the N-1 non-switching aggressors. Third, the branches in the victim net are reduced in a similar manner as those aggressor net branches. At the end of this step, we obtain a simple circuit with only two main wires each corresponding to the victim net and the active aggressor net. Finally, resistance and capacitance values of the reduced template circuit, shown in Figure 2 are extracted.

The template circuit for crosstalk noise modeling shown in Figure 2 is an extension to the 2-π model proposed in [10], where the victim net is modeled using the 2-π (3-node) circuit while the aggressor net is simplified as a saturated ramp input at node *1* in Figure 2. In this paper, we model both victim net and aggressor net as 2-π circuits so that the location of the capacitive coupling can be correctly modeled and overall modeling accuracy is much improved. We have proposed a simple yet accurate double pole model to solve the crosstalk noise estimation problem in the reduced template circuit. Note that this template circuit, however, is only suitable for short to medium interconnects because it uses only one lumped coupling capacitor. More complex template circuits with larger number of coupling capacitors should be employed for very long wires. Nevertheless, the reduction methods proposed in this paper are generic, and they are not restricted to the specific circuit topology shown in Figure 2.

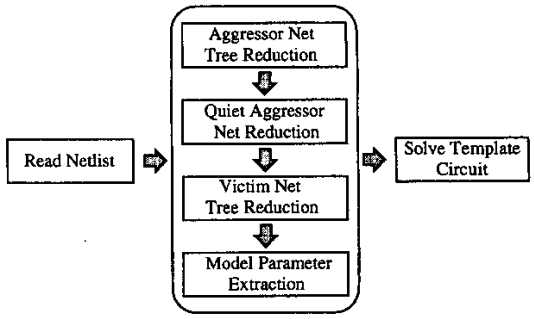

Figure 1: Flowchart of tree and quite aggressor net reduction.

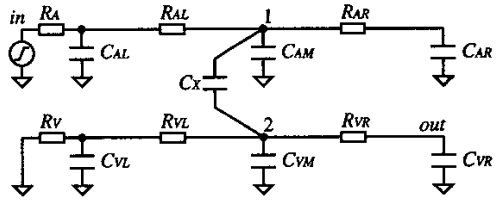

Figure 2: Single aggressor crosstalk noise model.

3. REDUCTION TECHNIQUES

Each reduction technique described in this section consists of two phases in sequence. In the first phase, a quiet aggressor net or tree branch is modeled using simple reduced circuits by matching the lower order Taylor series expansion coefficients of the admittance $Y(s)$ at the coupling point or branching point of the circuit. In the second phase, an effective capacitance is derived to replace those reduced circuits to further improve the efficiency.

3.1 Overview of point admittance

Let $Y(s)$ denotes the point admittance of a general circuit. It can be approximated by the sum of lower order Taylor series expansion terms

$$Y(s) = y_0 + y_1 s + y_2 s^2 + y_3 s^3 + O(s^4). \quad (1)$$

where y_n ($n = 0, 1, 2, 3$) is the n-th expansion coefficient. Note that the first term y_0 is zero when there is no dc conducting path from the observing point to the ground.

The *coupling-point admittance* or *branching-point admittance* is computed starting from the leaf nodes of a RC tree then going back to the coupling or branching point. This is similar to the approaches used in solving the driving-point admittance problem for gate delay calculation [13]. Three basic rules are used in the algorithm to calculate the lower order coefficients. Those rules are presented in (2)-(4) and are illustrated in Figure 3.

Rule 1: serial resistance:

$$\begin{aligned} y_0^* &= p y_0 \\ y_1^* &= p^2 y_1 \\ y_2^* &= p^2 y_2 - p^3 r y_1^2 \\ y_3^* &= p^2 y_3 - 2p^3 r y_1 y_2 + p^4 r^2 y_1^3, \end{aligned} \quad (2)$$

where the parameter p is defined as $p = 1/(1 + r y_0)$.

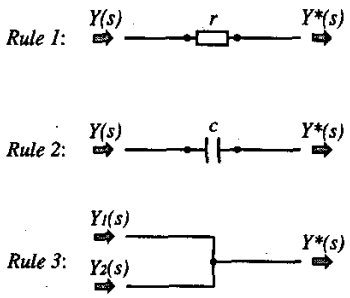

Figure 3: Rules for point admittance expansion coefficients.

Rule 2: serial capacitance:

$$\begin{aligned} y_0^* &= 0 \\ y_1^* &= c \\ y_2^* &= -c^2/y_0 \\ y_3^* &= c^2(y_1+c)/y_0^2. \end{aligned} \tag{3}$$

Rule 3: branch join:

$$\begin{aligned} y_0^* &= y_{1,0}+y_{2,0} \\ y_1^* &= y_{1,1}+y_{2,1} \\ y_2^* &= y_{1,2}+y_{2,2} \\ y_3^* &= y_{1,3}+y_{2,3}, \end{aligned} \tag{4}$$

where $y_{i,0}, y_{i,1}, y_{i,2}$ and $y_{i,3}$ are the first four Taylor series expansion coefficients of the i-th branch ($i = 1, 2$), respectively. Note that *Rule 3* can be applied for multiple times when there are more than two joining branches.

It is easy to observe that 1) the first four terms of the admittance y_0, y_1, y_2, and y_3 are preserved by repeated application of above rules, and 2) the time complexity to reduce a subtree using this reduction technique is linear with respect to the number of RC elements in the netlist.

3.2 Quiet aggressor net reduction

Consider the equivalent quiet aggressor net shown in Figure 4(a). We first reduce the aggressor net to a single resistor R_A^* and a single capacitor C_A^* as shown in Figure 4(b) by matching the first two Taylor series expansion coefficients y_0 and y_1 of the aggressor net at node A. Since only y_0 and y_1 appear at the right side of (3), we can hence neglect higher order Taylor coefficients at node A to achieve third order accuracy at node V. By applying both *Rule 1* and *Rule 3*, it is straightforward to obtain the admittance at node A as

$$Y_A(s) = \frac{1}{R_A+R_{AL}} + \left(\frac{R_A^2}{(R_A+R_{AL})^2}C_{AL}+C_{AM}+C_{AR}\right)s + O(s^2). \tag{5}$$

Therefore, the devices in the simplified circuit shown in Figure 4(b) have the following values

$$R_A^* = R_A+R_{AL}, \tag{6}$$

$$C_A^* = \frac{R_A^2}{(R_A+R_{AL})^2}C_{AL}+C_{AM}+C_{AR}. \tag{7}$$

Next, we derive the formula to estimate the effective coupling capacitance C_{eff} of a quiet aggressor net, based on the simplified circuit shown in Figure 4(b). To introduce some intuition, we first

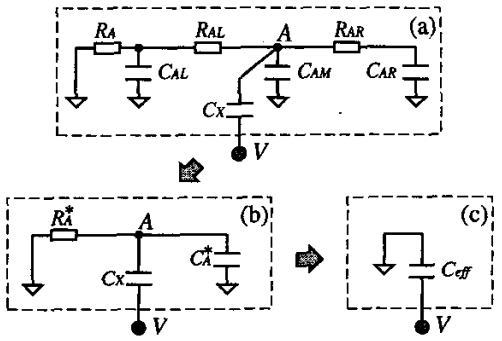

Figure 4: Quiet aggressor net reduction for crosstalk estimation. (a) Equivalent circuit for the quiet aggressor net. (b) Reduced circuit by matching first two Taylor expansion terms. (c) Effective capacitance for the aggressor.

study the upper and lower bounds of C_{eff}. When the effective resistance R_A^* of the quiet aggressor net approaches zero, we can consider node A as being grounded. Therefore, the effective coupling capacitance is the actual coupling capacitance $C_{eff}^{max} = C_X$. On the other hand, as R_A^* approaches infinity, node A floats and the coupling point V is connected to the ground through two series capacitors C_X and C_A^*. Therefore, the effective coupling capacitance approaches $C_{eff}^{min} = C_A^*C_X/(C_A^*+C_X)$. For a realistic R_A^* value, the C_{eff} is somewhere between these two bounds.

We find the value of the effective capacitance by matching the current drawn by the circuit in Figure 4(b) with that taken by the effective capacitor, i.e., our task is to find a constant C_{eff} such that

$$C_{eff}\frac{dV_V(t)}{dt} \simeq C_X\left(\frac{dV_V(t)}{dt} - \frac{dV_A(t)}{dt}\right). \tag{8}$$

Assume the voltage waveform of the victim net is a normalized ramp input $V_V(t) = t/t_r$, $0 \le t \le t_r$. We have obtained the following formula for the effective capacitance

$$C_{eff} = \left(1 - \frac{R_A^*C_X}{t_r}\left(1 - e^{-t_r/(R_A^*(C_A^*+C_X))}\right)\right)C_X. \tag{9}$$

It can be easily verified that C_{eff} approaches C_X when $R_A^* \to 0$ and that C_{eff} approaches $C_A^*C_X/(C_A^*+C_X)$ as $R_A^* \to \infty$. Experiments on a large number of ramdon circuits have shown that using the proposed effective capacitance results to less than 5% error in most cases while using either C_{eff}^{max} or C_{eff}^{min} as the effective capacitance may have over 20% error.

3.3 Tree branch reduction

In general, a net has a tree structure instead of being a simple wire. Previous works use a simple method for tree branch reduction, where the total capacitances including wire capacitances and load capacitances of a branch are lumped at the branching point. However, with scaling of VLSI technology, the effect of interconnect resistive shielding can no longer be neglected. When interconnect resistance of a branch is considered, the actual capacitance seen at the branching point is always less than the total capacitance of the branch. Therefore, using total capacitance will result in an underestimation of the crosstalk noise. In this section, we derive a formula to find the value of the effective branching capacitance.

The problem we have here is very similar to the driving point admittance problem for gate delay calculation. However, the tree we

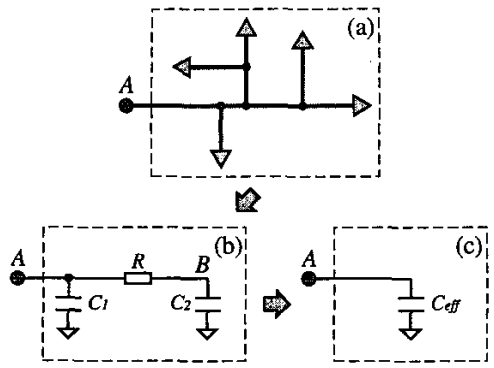

Figure 5: Tree reduction for crosstalk estimation. (a) General RC tree branch. (b) Reduced-order π-model for the tree. (c) Tree effective capacitance.

consider here are actually branches that connected to the 'main' wires of the aggressor nets or the victim net. We model those branches employing similar approaches as those used in [13] and [14]. First a general RC tree structure is reduced to a simple π-model as shown in Figure 5(b) by matching the first three moments of the tree. The resulting model is then further reduced to an effective capacitance, shown in Figure 5(c), for a given signal switching slope at the node A.

The difference between the proposed method and the techniques for effective driving point capacitance lies in the interfacing of the π-type circuit with external waveforms. For delay calculation, the effective capacitance tries to match the average capacitance for the period from start to the time when the voltage reaches 50% of the supply voltage. For crosstalk noise estimation, however, we try to match the average capacitance of the branch during the entire signal switching period.

Since there is no direct dc path to the ground in circuit branches, we always have $y_0 = 0$. Once the first three moments of a general RC tree are obtained by repeatedly applying *Rule 1*, we can construct a reduced π-type circuit which matches those three moments. The values of the capacitors and the resistor in the figure are calculated as

$$C_1 = y_1 - \frac{y_2^2}{y_3}, \quad C_2 = \frac{y_2^2}{y_3}, \quad R = -\frac{y_3^2}{y_2^3}. \tag{10}$$

Note that for a RC tree, y_2 is always a negative value. Therefore, the resistance R is positive. Similarly, C_1 and C_2 are always positive for realistic circuits and the sum of C_1 and C_2 is the total capacitance of the RC tree.

The π-type circuit derived is still not simple enough for our purpose because each branch on the two 'main' wires will add one additional node (node B) to the final reduced circuit and the number of such branches can potentially be very large. So the next step is to find an effective capacitance for a given input waveform at node A such that this single effective capacitor can approximate the load condition of the π circuit.

Similar to the approach used in the previous subsection, we try to find a constant C_{eff} such that

$$C_{eff}\frac{dV_A(t)}{dt} \simeq C_1\frac{dV_A(t)}{dt} + C_2\frac{dV_B(t)}{dt}. \tag{11}$$

Assuming a normalized saturated ramp input at the victim node with a rise time of t_r, the effective capacitance can be derived as

$$C_{eff} = C_1 + \left(1 - \frac{RC_2}{t_r}(1 - e^{-t_r/RC_2})\right)C_2. \tag{12}$$

4. TEMPLATE CIRCUIT ANALYSIS

Using tree reduction and quiet aggressor net reduction techniques described in previous sections, the crosstalk noise estimation problem is transformed to a much simpler one of solving the 6-node reduced circuit as shown in Figure 2. In this section, we derive the analytical expression to calculate the crosstalk noise waveform of the reduced circuit.

For template circuits with fixed topology, we can always find all poles and their respective residues. Exact waveform can therefore be derived based on those pole/residue pairs. This approach, however, requires to numerically solve a 6-th order equation. Furthermore, it does not give a clear physical picture on the waveform of the noise glitch, nor does it offer an analytical way to calculate the maximum noise height and the noise width.

The desire to have simple analytical expressions for the noise voltage waveform and the maximum noise voltage has led to models based on the dominant pole approximation [9], [10], which has been shown capable of estimating the maximum noise voltage with an acceptable accuracy for certain template circuits. However, for our template circuit shown in Figure 2, which is more complex than the template circuits used in previous works, the dominant pole approximation is no longer a good approximation.

It is our goal to derive a simple yet efficient formula that overcomes the shortcomings of the aforementioned problems. It is clear that the single pole approximation is not adequate for the proposed 6-node template circuit. We will, therefore, use a double-pole approximation approach where the first pole mainly models the victim net and the second pole models the aggressor net.

First, we decouple the victim net from the aggressor net using a similar approach as that we used to reduce quiet aggressor net. The Elmore delay from the input to the coupling node at the aggressor net is estimated as

$$t_{A,0} = C_{AL}R_A + (C_{AM} + C_X + C_{AR})(R_A + R_{AL}). \tag{13}$$

The approximate rise time at the aggressor coupling node is

$$t_{r,0} = t_r + t_{A,0}/(1 - e^{-1}). \tag{14}$$

The effective capacitances for the victim net and for the right segment of the aggressor net can be calculated as

$$C^v_{eff} = \left(1 - \frac{t_X}{t_{r,0}}(1 - e^{-t_{r,0}/t_V})\right)C_X, \tag{15}$$

$$C^r_{eff} = \left(1 - \frac{R_{AR}C_{AR}}{t_{r,0}}(1 - e^{-t_{r,0}/R_{AR}C_{AR}})\right)C_{AR}. \tag{16}$$

where

$$t_X = C_X(R_V + R_{VL}) \tag{17}$$

$$t_V = C_{VL}R_V + (C_{VM}+C_X)(R_V+R_{VL}) + C_{VR}(R_V+R_{VL}+R_{VR}). \tag{18}$$

The approximate time constant corresponding to the dominant pole at the aggressor net is therefore calculated as

$$t_A = C_{AL}R_A + (C_{AM} + C^v_{eff} + C^r_{eff})(R_A + R_{AL}). \tag{19}$$

And the aggressor time-domain voltage waveform is obtained as

$$V_A(t) = \begin{cases} \frac{t}{t_r} - \frac{t_A}{t_r}\left(1 - e^{-t/t_A}\right) & t \le t_r \\ 1 - \frac{t_A}{t_r}\left(1 - e^{-t_r/t_A}\right)e^{-(t-t_r)/t_A} & t > t_r \end{cases}. \tag{20}$$

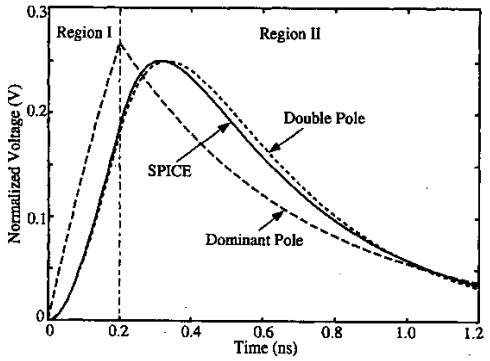

Figure 6: Comparison of noise waveforms.

Now, instead of using a simple ramp function at node 1 as the aggressor net waveform, we use the above more accurate form. Using dominant pole approximation on the victim net, we have obtained the time-domain noise voltage output, which can be divided into the following two regions:

1) Region I ($0 \le t \le t_r$):

$$V_{out}^{I}(t) = \frac{t_X}{t_r}\left(1 + \alpha e^{-t/t_A} - \beta e^{-t/t_V}\right), \tag{21}$$

2) Region II ($t > t_r$):

$$V_{out}^{II}(t) = \frac{t_X}{t_r}\left(\alpha\left(e^{-t/t_A} - e^{-(t-t_r)/t_A}\right) - \beta\left(e^{-t/t_V} - e^{-(t-t_r)/t_V}\right)\right), \tag{22}$$

where $\alpha = t_A/(t_V - t_A)$ and $\beta = t_V/(t_V - t_A)$.

It can be easily observed that the noise voltage increases monotonically in Region I and it increases, then decreases in Region II. Therefore, the maximum noise voltage always occurs in Region II. By solving the equation $dV_{out}^{II}(t)/dt = 0$, we obtain the time noise voltage reaches the peak

$$t_{peak} = t_r + \frac{t_V t_A}{t_V - t_A}\ln\left(\frac{1 - e^{-t_r/t_A}}{1 - e^{-t_r/t_V}}\right). \tag{23}$$

We compare the noise waveforms generated by the dominant pole and the double pole models with that obtained using SPICE simulation in Figure 6. The following circuit parameters are assumed. The driving resistances of the aggressor and the victim are 500 Ω and 1000 Ω, respectively; the wire resistances are 100 Ω each; the ground capacitances are 50 fF each and the coupling capacitance is 150 fF; and the rising slope of the input signal is 200 ps. Clearly, the waveform obtained using the double pole approximation is more accurate than that obtained by the dominant pole approximation. First, the noise peak time is very close to the correct value. Second, the derivative of the voltage waveform is continuous throughout the entire range, which is important for many optimization engines. And third, the noise voltage matches the simulated result well over the entire waveform.

Peak noise voltage is a metric to determine whether the noise on a signal wire exceeds the static noise margin of the receivers. However, the duration that the signal is higher than receiver static noise margin should also be considered to measure the effect of the noise on the receiver output. In literature, this is accomplished by using the noise width metric. In the presence of multiple aggressor nets, however, the noise width of the glitches generated by each single aggressor cannot be simply combined as we can do with the peak noise voltage. Therefore, in this paper, we use the noise area metric. Similar to noise height, noise area produced by each aggressor can be simply added to derive the total noise area generated when all aggressors are switching simultaneously.

Table 1: Experimental results on noise area.

Circuit	NA/NS	#RC	Len	SPICE	Model (Err%)
1	2/2	97	1.49	0.535	0.541 (1.3)
2	9/9	215	2.80	0.610	0.596 (2.2)
3	4/4	132	2.62	0.634	0.644 (1.7)
4	5/5	128	2.80	0.535	0.522 (2.6)
5	9/9	167	2.79	0.599	0.600 (0.2)
6	9/9	201	2.61	0.518	0.520 (0.3)
7	4/4	112	1.47	0.396	0.393 (0.7)
8	7/6	144	0.71	0.706	0.706 (0.0)
9	7/5	121	2.07	1.223	1.220 (0.2)
10	2/2	88	2.82	0.483	0.477 (1.2)
11	7/7	174	2.70	0.449	0.459 (2.4)
12	3/3	116	1.69	0.409	0.404 (1.3)
13	3/3	117	1.69	0.407	0.404 (0.7)
14	10/10	191	2.58	0.388	0.397 (2.1)
15	3/3	106	1.47	0.324	0.329 (1.5)
16	2/2	106	1.71	0.410	0.409 (0.4)
17	7/4	171	2.82	8.965	8.969 (0.0)
18	3/3	112	1.68	0.402	0.407 (1.1)
19	2/2	94	1.49	0.272	0.269 (1.2)
20	3/3	118	1.70	0.407	0.406 (0.1)
21	2/2	98	1.65	0.392	0.397 (1.1)
22	7/7	181	2.73	0.647	0.651 (0.6)
23	5/3	136	2.72	8.870	8.860 (0.1)
24	2/2	95	1.48	0.246	0.250 (1.5)
25	3/3	116	1.70	0.404	0.401 (0.7)
26	5/5	114	2.41	0.337	0.352 (4.3)
27	10/9	247	2.75	0.380	0.385 (1.2)
28	5/5	138	2.71	0.389	0.406 (4.5)
29	2/2	95	1.47	0.275	0.282 (2.5)
30	9/9	187	2.12	0.226	0.224 (1.0)
Ave	**5.0/4.7**	**128**	**2.1**	-	**1.3%**

The area under the noise voltage waveform can be calculated by integrating the noise voltage equations, which turns out to be a very simple equation

$$Area = C_X(R_V + R_{VL}). \tag{24}$$

Note that the above expression is normalized to the supply voltage V_{DD}. The noise area equation holds for both dominant-pole and double-pole based formulas.

5. EXPERIMENTS

We have applied the proposed method to industrial circuits to further verify its correctness. The set of circuits available to us is 30 noise-prone nets from a high-performance processor designed in a 0.15 micron process technology. In those nets, the drivers of the circuits were replaced by linear resistors using the technique described in [7]. Logic correlations and overlapping of timing windows were also considered.

Some information of the circuits and comparison of the model results with SPICE simulation results on noise area are shown in Table 1. The second column shows the number of total aggressor

Table 2: Experimental results on peak noise voltage.

Circuit	SPICE (V)	Simple (Err%)	Proposed (Err%)
1	0.839	0.772 (8.0)	0.900 (7.4)
2	0.793	0.672 (15.3)	0.782 (1.4)
3	0.790	0.670 (15.3)	0.812 (2.7)
4	0.786	0.650 (17.3)	0.796 (1.3)
5	0.765	0.659 (13.9)	0.765 (0.0)
6	0.772	0.658 (14.7)	0.731 (5.4)
7	0.764	0.704 (7.9)	0.772 (1.0)
8	0.716	0.727 (1.7)	0.761 (6.3)
9	0.713	0.675 (5.2)	0.727 (2.1)
10	0.710	0.559 (21.3)	0.654 (7.8)
11	0.704	0.589 (16.3)	0.717 (1.8)
12	0.695	0.609 (12.4)	0.682 (1.9)
13	0.693	0.609 (12.0)	0.682 (1.5)
14	0.682	0.576 (15.5)	0.658 (3.5)
15	0.686	0.632 (7.9)	0.702 (2.3)
16	0.690	0.612 (11.3)	0.683 (1.1)
17	0.686	0.634 (7.6)	0.693 (1.0)
18	0.688	0.615 (10.6)	0.687 (0.1)
19	0.685	0.597 (12.9)	0.684 (0.2)
20	0.685	0.606 (11.5)	0.676 (1.3)
21	0.684	0.610 (10.9)	0.682 (0.4)
22	0.663	0.559 (15.7)	0.658 (0.7)
23	0.662	0.600 (9.4)	0.714 (7.7)
24	0.656	0.577 (12.0)	0.657 (0.2)
25	0.656	0.581 (11.4)	0.640 (2.5)
26	0.632	0.580 (8.2)	0.616 (2.5)
27	0.632	0.548 (13.3)	0.585 (7.4)
28	0.626	0.562 (10.2)	0.625 (0.1)
29	0.626	0.561 (10.4)	0.639 (2.0)
30	0.622	0.561 (9.8)	0.585 (5.9)
Ave/Max	-	**11.7% / 21.3%**	**2.7% / 7.8%**

nets and number of switching aggressor nets. The third column is the total number of RC elements in a given circuit. The average number of all the nets is 128. The lengths of the victim nets in millimeters are shown in the fourth column, and varies from less than 1 mm up to about 3 mm, with an average victim net length of 2.1 mm.

Noise area calculated using the proposed model is compared with those obtained using SPICE simulation in the last two columns of Table 1. Both are in the unit of $ns \cdot V$. According to Eq. (24), the noise area is a function of only three variables: C_X, R_V and R_{VL}, none of which is affected by the reduction techniques described in previous sections. Therefore, both the proposed approach and the simple approach which does not use effective capacitances, generate the same results in terms of noise area. Also, in agreement with the fact that Eq. (24) is exact, we observe the model errors are very small with an average value of 1.3%.

In Table 2, we compare the peak noise voltage values of the simple approach and the proposed approach with SPICE simulation results. In the simple approach, the quiet aggressor nets are grounded during superposition and the resistive shielding effect in the branches is not considered. The proposed approach has an average peak noise error of 2.7% and the maximum error is 7.8%. The majority of the circuits (23 out of 30) have an error less than 5%. In comparison, the simple method has an average error of 11.7% and a maximum error of 21.3%. It underestimates the crosstalk noises by more than 10% in 21 out of 30 circuits.

6. CONCLUSION

We have proposed an efficient crosstalk noise estimation framework that maintains the efficiency of prior works and has much improved accuracy. Novel reduction techniques were proposed for quiet aggressor net reduction, which models the effect that the quiet aggressor nets are affected by the victim waveform, and for tree branch reduction, which considers the effect of resistive shielding of branch interconnects. A double-pole based formula is derived for analytical model of the reduced 6-node template circuit. Experimental results on industrial circuits is promising.

The proposed crosstalk noise estimation methodology is very efficient, therefore is suitable as a noise estimation engine for various physical design tools such that coupling noise, together with circuit area, speed and power consumption, can be used as a metric for design optimization.

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