Circuit and System Designs of Ultra-Low Power Sensor Nodes With Illustration in a Miniaturized GNSS Logger for Position Tracking: Part I—Analog Circuit Techniques

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***Abstract*— This paper, split into Parts I and II, reviews recent innovations in circuit design that have accelerated the miniaturization of sensor nodes. Design techniques for key building blocks, such as sensor interfaces, timing reference, data communication, energy harvesting, and power management are reviewed. In particular, Part I introduces analog circuit techniques and sensor interfaces for miniaturized sensor nodes. The energy budget of such system is highly restricted due to the small battery volume. Therefore, ultra-low power design techniques are critical enablers and are reviewed. Design techniques for compact monolithic integration are also discussed.**

***Index Terms*— Internet of Things, IoT, sensor node, ultra-low power, wireless sensor node, GNSS.**

I. Introduction

MINIATURIZATION and interactive communication are the two main topics that dominate the recent research in the internet-of-things (IoT) [1]–[11]. The high demand for continuous monitoring of environmental and bio-medical information has accelerated sensor technologies as well as circuit innovations. Simultaneously, the advances in communication methods and the wide spread use of cellular and local data links enable the networking of sensor nodes. This potential improvement in machine service for humans could trigger the commercial development of a sensor node with platforms that collect, process and transmit widely spread environmental and bio-medical data.

In the history of computing platforms, from mainframes in the 1950s to workstations in the 1960s, personal computers in the 1980s, laptops in the 1990s and now the current smart phones, one of the most evident trends is the increasing convenience and frequency of access by humans who utilize the computing platform. Miniaturization of the computer is an important factor in this trend, lowering cost, reducing the required space and providing mobility. However, the need for physical access with an interfacing component like a screen, buttons or a touch surface limits its form factor and therefore inhibits further miniaturization.

On the other hand, the next generation of computing platforms, which is the IoT, increases proximity to the source of the information rather than to humans, allowing much more aggressive miniaturization.

The key technology of miniaturization has been process scaling, which has reduced the silicon area, increased computational capability and lowered power consumption. However, leakage current of a device has continuously increased with the process scaling so that the latest deep-submicron technologies do not fit well on the mm-scale computing platforms that demand nano-watt levels of sleeping power. Therefore, advances in *circuit level techniques* are critical to realize networks of mm-scale IoT computing platforms.

Furthermore, a miniaturized form factor incurs a severely restricted energy budget [12], [13]. For instance the 0.92-mm^3 Li thin-film battery introduced in [14] provides nearly $1/10^6$th the energy capacity of an alkaline AA battery. Therefore, the transition of the circuit design regime from milli-watt to nano-watt level is critical.

This paper, split into Parts I and II [1], reviews recent advances in circuit techniques in the implementation of the key building blocks for miniaturized sensor nodes. Part I of this work includes design challenges associated with sensor front-end circuits. In section II, circuit techniques for analog references and amplifiers are introduced. Section III includes system level discussions on capacitive sensor interfaces and bio-medical applications. As one of the key elements for saving sleep power of a miniaturized sensor node, ultra-low power timing references are reviewed in section IV. Part II of this work includes design challenges in data transceiver, energy harvester, power management unit and digital logic gates. Finally, Part II proposes a miniaturized (2.7 cm^3) global

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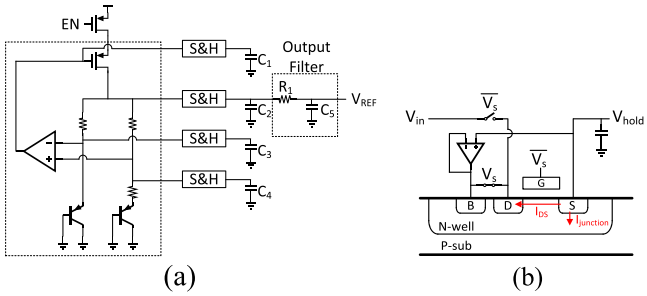


Fig. 1. (a) A sample-and-hold bandgap circuit proposed in [18]. (b) Schematic of a sample-and-hold switch.

navigation satellite system (GNSS) logger as a proto-type design example.

II. Analog Circuit Techniques

Due to the inherent energy constraints of wireless sensor nodes, reducing the power consumption of the main building blocks that make up such systems is critical. Efficient power management circuits, low-power energy harvesting circuits and communication protocols that minimize energy consumption are emphasized.

The energy budget of a sensor interface is highly limited due to the battery size, and most of the major building blocks need to consume sub-nano to micro watt amounts of power [2]–[4], [9], [15]–[17]. Thus innovative circuit techniques are required to reduce the power consumption of these mW-circuit designs by more than 10^6times. In this section, useful circuit design techniques aimed at improving voltage reference, current reference and amplifier DC biasing are reviewed.

A. Voltage Reference

An accurate voltage reference that is insensitive to process, voltage and temperature (PVT) variations is required in many analog and mixed-mode circuits, such as those found in an amplifier or an analog-to-digital converter (ADC). However, conventional band-gap based voltage references consume more than 100 nW, making integration into an ultra-low power sensor node system difficult.

The sample-and-hold bandgap proposed in [18] can be a good solution to such problems. As shown in Fig. 1(a), the voltages of the bandgap reference are simply sampled at C_1–C_5 and maintained by occasionally enabling the bandgap. The bandgap is heavily duty-cycled so that the on-time of the bandgap is only 0.003% of the off-time. The major factor that determines the minimum duty-cycle is the leakage in the sample-and-hold circuits. The leakage of a sample–and-hold switch consists of the diode leakage of the source-to-body junction and the transistor off-leakage from the source to the drain. These two leakages are minimized by adopting a low power amplifier that biases the drain and body voltages to the source voltage when the sampling transistor is off as shown in Fig. 1(b). The proposed work consumes 2.98 nW, which is approximately a 250x reduction, while maintaining the accuracy of the output voltage under temperature and supply variations.

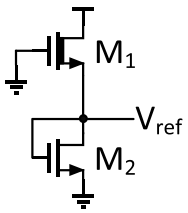


Fig. 2. A CMOS based voltage reference proposed in [19].

A CMOS-based voltage reference consuming less than 30 pW is proposed in [19]. This work uses two transistors of different sizes, M_1 and M_2, with the sizes shown in Fig. 2. The output voltage can be calculated by equalizing the current of the two transistors. The subthreshold current of a MOSFET can be calculated using the following equation:

$$I_{sub} = \mu C_{ox} \frac{W}{L} (m-1) V_T^2 e^{\frac{V_{gs}-V_{th}}{mV_T}} \left(1 - e^{\frac{-V_{ds}}{V_T}}\right) \quad (1)$$

where μ, C_{OX}, W, L, V_T, V_{gs}, V_{ds} and V_{th} are the mobility, unit oxide capacitance, width of the transistor, length of the transistor, thermal voltage, gate-to-source voltage, drain-to-source voltage and threshold voltage, respectively. The subthreshold slope factor, m, is expressed as $1+C_d/C_{ox}$ where C_d is the unit depletion capacitance. There exist other sources of static current, such as the drain-induced barrier-lowering (DIBL) current of M_1 and source-to-body junction leakage currents. However, they are typically negligible compared with the subthreshold current. Therefore, in this paper, they are ignored to simplify the solution and provide an intuitive understanding of the operation of the voltage reference. Assuming that V_{ds} is sufficiently greater than V_T so that $\exp(-V_{ds}/V_T)$ can be neglected, the currents though M_1 (I_1) and M_2 (I_2) are as follows:

$$I_1 = \mu_1 C_{ox1} \frac{W_1}{L_1} (m_1 - 1) V_T^2 e^{\frac{-V_{th1}-V_{ref}}{m_1 V_T}} \quad (2)$$

$$I_2 = \mu_2 C_{ox2} \frac{W_2}{L_2} (m_2 - 1) V_T^2 e^{\frac{V_{ref}-V_{th2}}{m_2 V_T}} \quad (3)$$

Equating (2) and (3) provides V_{ref} as a function of the process parameters as described by the following equation:

$$\begin{aligned}
&\mu_1 C_{ox1} \frac{W_1}{L_1} (m_1 - 1) V_T^2 e^{\frac{-V_{th1}-V_{ref}}{m_1 V_T}} \\
&\quad = \mu_2 C_{ox2} \frac{W_2}{L_2} (m_2 - 1) V_T^2 e^{\frac{V_{ref}-V_{th2}}{m_2 V_T}} \\
&\ln\left(\mu_1 C_{ox1} \frac{W_1}{L_1} (m_1 - 1)\right) + \frac{-V_{th1} - V_{ref}}{m_1 V_T} \\
&\quad = \ln\left(\mu_2 C_{ox2} \frac{W_2}{L_2} (m_2 - 1)\right) + \frac{V_{ref} - V_{th2}}{m_2 V_T} \\
&V_{ref} = \frac{m_1 V_{th2} - m_2 V_{th2}}{m_1 + m_2} + \frac{m_1 m_2}{m_1 + m_2} V_T \\
&\quad \times \ln\left(\frac{\mu_1 C_{ox1} \frac{W_1}{L_1} (m_1 - 1)}{\mu_2 C_{ox2} \frac{W_2}{L_2} (m_2 - 1)}\right) \quad (4)
\end{aligned}$$

Note that the output voltage, V_{ref}, is dependent on the difference between the two threshold voltages and the ratio of the device parameters, making it insensitive to process variation.

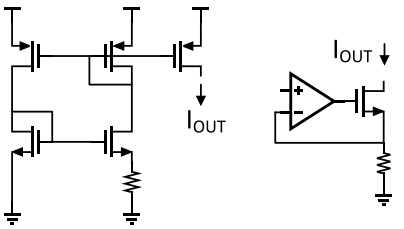


Fig. 3. Conventional current references (a) constant-g_m (b) resistor regulation.

The optimal device size for minimizing the temperature coefficient (TC) can be determined using the following equation:

$$\frac{dV_{ref}}{dT} = 0 \rightarrow \left(\frac{W_1}{W_2}\right)_{opt} = \frac{\mu_2 C_{ox2}\,(m_2-1)\,/L_2}{\mu_1 C_{ox1}\,(m_1-1)\,/L_1} e^{\frac{k}{q}\left(\frac{1}{m_2}\frac{dV_{th2}}{dT}-\frac{1}{m_1}\frac{dV_{th1}}{dT}\right)} \quad (5)$$

Note that (4) and (5) are slightly different and corrected versions of equations (3) and (4) in [19].

B. Current Reference

The bias current of an amplifier determines its bandwidth. If the bias current is lower than its target, the signal bandwidth is reduced, causing gain attenuation at high frequency. On the other hand, if the current is too large, the noise integration range of the signal is increased unless an accurate filter insensitive to PVT variation is added before the sampling. If the amplifier noise is the dominant noise source, the thermal noise reduction and the noise bandwidth increase cancel each other out; thus, the output noise rarely depends on the bias current. However, if the major noise source is the input of the amplifier, an increase in the noise integration range causes a lower signal-to-noise ratio at the output. Energy waste due to the high bias current is another side effect of high bias current. In addition, changing the pole locations can impair the feedback stability of the amplifiers. Therefore, stable bias current generation, insensitive to environmental change, is required.

A current reference is usually implemented using a resistor. Fig. 3 shows conventional methods used to generate a current reference for a constant-g_m and a current reference using the combination of a voltage reference and a resistor. The challenge of such an implementation in ultra-low power sensor nodes is the size of the resistor. Due to power limitations, sensor nodes demand a sub-nA current reference. Thus >100 MΩ is required in order to implement such low current using conventional approaches, which is highly impractical because of the size of the resistor.

Reference [20] proposes a 20-pA resistor-less current reference circuit using a threshold voltage cancellation scheme. A complementary to absolute temperature (CTAT) voltage generator using a diode stack of transistors produces a gate voltage of a subthreshold transistor and compensates for the temperature dependence of the threshold voltage as shown in Fig. 4. The supply voltage of the CTAT circuit is generated

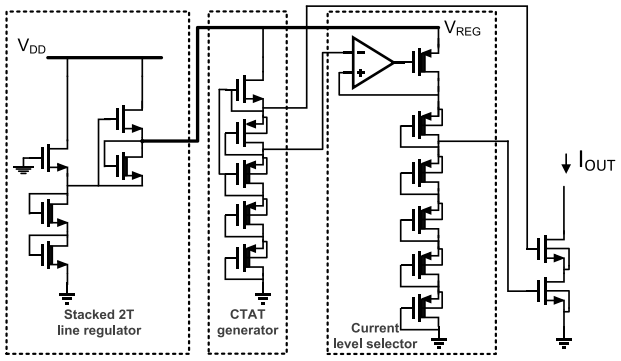


Fig. 4. A resistor-less current reference proposed in [20].

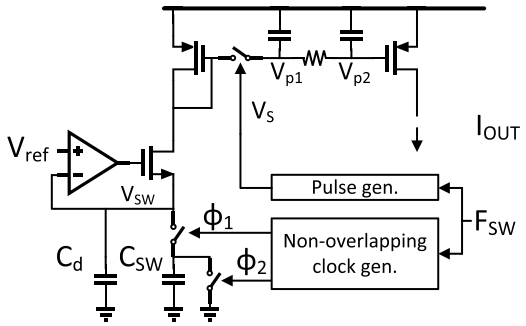


Fig. 5. A switched capacitor based current reference generation.

with a 2T voltage [19], and its supply dependence is minimized. The output stage is designed with a stack of NMOS transistors to improve the load sensitivity of the output current. The quiescent power consumption of this current reference is 23 pW, which is suitable for low power applications.

Nevertheless, the aforementioned technique relies on precise coefficient matching between the CTAT generator and the NMOS threshold voltage, which is difficult to achieve without multi-temperature trimming. An ultra-low power current reference replacing a resistor with a switched capacitor is introduced in [21]. A voltage reference can be implemented in sub-nW power consumption conditions [19]. If stable frequency is available in the sensor node, a stable current reference can be generated by regulating a switched capacitor with a reference voltage as shown in Fig. 5; its output current is $C_{sw}V_{ref}F_{sw}$. Note that the area occupied by the capacitor is proportional to the output current, making it advantageous for the generation a sub-nW current reference. The voltage ripple generated by the switching operation of the capacitor can be attenuated by the parallel capacitance, C_d, and is further reduced by sampling the mirroring voltage, V_p, with the switching clock or with R-C filtering using a pseudo-resistor. Typically C_d needs to be at least 10 times larger than C_{sw} to sufficiently lower the voltage ripple caused by the switching operation [21].

C. Resistance Boosting

Often a sensor node measures slowly varying signals, such as voice, pressure or neural signals. Its analog front-end demands time constants of a filter or amplifier that are an order of magnitude larger than the signal changing rate in such cases. A pseudo-resistor, introduced in [22], has been widely adopted

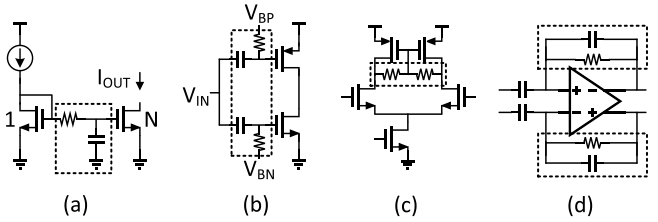


Fig. 6. Use of pseudo-resistor in (a) noise filtering (b) ac coupling (c) common mode feedback and (d) amplifier servo loop.

to generate very low frequency poles and zeros for low pass filtering, ac coupling, common mode feedback and amplifier biasing as shown in Fig. 6 [17], [23]–[26]. A pseudo-resistor can provide a very large resistance with a series of turned-off transistors that occupies only a few micro meter squares. Despite the efficient use of area, the resistance is highly dependent on environmental changes such as temperature and process variations, which makes widespread use of this approach difficult. For instance, in the amplifier biasing circuit shown in Fig. 6(d), the small resistance of the pseudo-resistor at high temperature increases the low cut-off frequency, which may even reach the signal bandwidth thereby causing signal attenuation. Furthermore, the current through the resistor is not negligible in such cases, resulting in signal distortion convoluted by the non-linearity of the pseudo-resistor. High resistance also causes side effects such as an increased settling time defined as the time constant of the pseudo-resistance and the parallel capacitance. Sometimes, the resistance is comparable to or even greater than the equivalent resistance of gate and metal-insulator-metal (MIM) capacitors caused by the leakage current due to tunneling, resulting in a shift of the DC operating point.

Adaptive biasing on the gate voltages of the pseudo-resistance has been proposed to improve the robustness of the pseudo-resistance [26]–[28]. The gate voltages of the pseudo-resistances are generated by a bias current combined with a replica transistor to define the impedance of the pseudo-resistor. In such approaches, however, the V_{gs} of the turn-off transistor in the pseudo-resistor varies according to the output voltage, and therefore the linearity becomes worse.

The duty-cycled resistor introduced in [29]–[31] is a viable option for achieving an accurate and linear resistance. Assuming that the switching frequency of a resistor is faster than the frequency of interest, a resistance, usually implemented with poly-silicon or N-well, is boosted by the factor of the duty cycle. Reference [31] and [30] implemented stable 256 MΩ and 20 GΩ for bias current generation and amplifier biasing, respectively, using on-chip poly-resistors.

A switched capacitor can also provide a large impedance with a small area [32], [33]. The resistance of a switched capacitor is $1/C_{SW}F_{SW}$, as discussed in Section II-B. Therefore, a smaller capacitance and switching frequency, which are advantageous to implement with a smaller area and low power, offer greater resistance. Reference [33] demonstrates a series-parallel charge-sharing technique during the capacitance switching operation that further boosts the equivalence resistance.

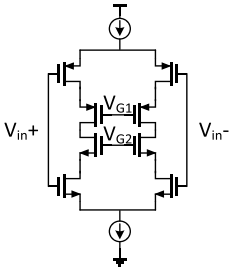


Fig. 7. A differential current reuse amplifier proposed in [44].

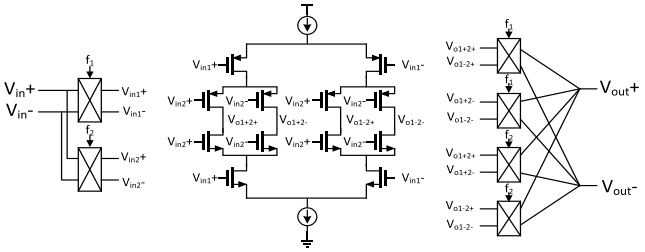


Fig. 8. A multi-chopper amplifier proposed in [25].

D. Amplifier

The minimum power consumption of an instrumentation amplifier is limited either by the input referred noise or the signal bandwidth, depending on the amplifier specification. Most of the sensor node applications, such as monitoring pressure [34], temperature [2], humidity [35], acceleration [36] or bio signals [17], [22]–[24], [32], [37]–[41], involve slowly varying signals of up to a few kHz; thus, the power consumption is determined by the noise specification rather than the bandwidth. Therefore, it is important to optimize the noise efficiency factor (NEF) of the amplifier, which can be expressed using the following equation [42]:

$$NEF = V_{rms,in}\sqrt{\frac{2I_{tot}}{\pi \cdot V_T \cdot 4kT \cdot BW}} \tag{6}$$

where $V_{rms,in}$, I_{tot}, V_T, k, T and BW are the root-mean-square of input referred noise voltage, total amplifier current, thermal voltage, Boltzmann's constant, temperature and noise integration bandwidth, respectively. NEF indicates the amount of current dissipation required to accomplish an input-referred noise specification. As the noise spectral density at the input of the transistor can be calculated by $4\,kT\gamma/g_m$, the maximization of the transconductance is critical. In this respect, an amplifier using transistors in subthreshold mode is advantageous. The transconductance, g_m, of a transistor is dependent on V_{gs} in strong inversion

$$Strong\ inversion\text{: } gm = \frac{2I_{DS}}{V_{gs} - V_{th}} \tag{7}$$

and is maximized when a transistor is in weak inversion [43]

$$Weak\ inversion\text{: } gm = \frac{I_{DS}}{mV_T} \tag{8}$$

Where m is $1 + C_d/C_{ox}$ and C_d and C_{ox} are depletion and oxide capacitances, respectively.

A current reuse scheme that further improves the transconductance is proposed in [44], and a differential version [45] is shown in Fig. 7. In this scheme, the input voltages are connected to both nmos and pmos differential pairs whose

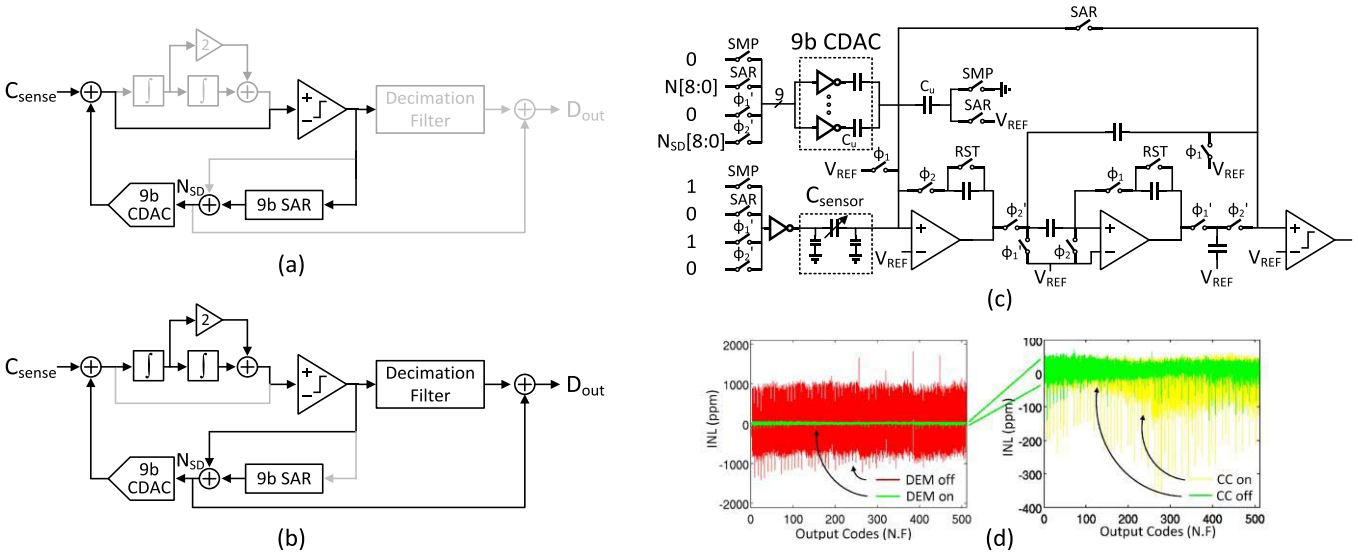


Fig. 9. An incremental $\Sigma\Delta$ CDC proposed in [49]. (a) SAR mode (b) $\Sigma\Delta$ mode (c) detailed schematic (d) INL measurement with dynamic element matching and common-centroid indexing.

current is shared, so that the devices are connected in parallel from an input signal's perspective. Since the transconductance is increased to $g_{mn} + g_{mp}$ while the current remains constant, the input referred voltage noise can be reduced compared to the single-input-pair implementation. This architecture has been widely adopted in instrumentation amplifiers targeting low NEF.

Reference [25] proposes a multi-chopper amplifier that utilizes the excessive bandwidth to reduce the NEF. As noted in the previous paragraph, the current of the amplifier is sufficiently large to reduce the input referred noise, causing excessive bandwidth at the output. This work mixes the input signal to the unused bandwidth using f_1 and f_2 and then reconstructs the signal at the output as shown in Fig. 8. This work achieved the lowest NEF of 1.38.

III. Sensor Interfaces

A. Capacitive Sensor Interface

To implement an ultra-low power sensor node, it is important to reduce the power consumption of the sensor itself. Capacitive sensors are suitable in this respect because the capacitive sensors do not consume static current [34]. Many papers have been published utilizing low power capacitive sensors to monitor parameters such as pressure [16], humidity [35], acceleration [36] and displacement [46].

One of the key challenges of such capacitive sensors is the dynamic range of the signal [35], [46]–[50]. The sensors provide up to tens of pF of base capacitance but require aF accuracy to precisely read out the information. Therefore, the delta-sigma modulation method is advantageous for high accuracy applications [35], [46]. However such an approach requires relatively high power consumption. Fig. 9 shows a recently published incremental $\Sigma\Delta$ CDC with zoom-in 9 bit asynchronous successive approximation (SAR) [49]. The energy efficiency of the CDC is improved by lowering the oversampling ratio (OSR) through the pre-calibration of the capacitance range using 9 bit SAR operating with a capacitive digital-to-analog converter (CDAC). Initially, the integrators are disabled, and the CDAC voltage is directly connected to the comparator to perform a SAR search of CDAC, as shown in Fig. 9(a). After the SAR phase, $\Sigma\Delta$ CDC is activated and generates a bit stream of the capacitor comparison result, as shown in Fig. 9(b). The detailed schematic of the CDC is shown in Fig. 9(c) and consists of two OTAs, one comparator, a 9-bit CDAC and switched capacitor circuits. This work includes the energy efficient dynamic element matching (DEM) method to improve the linearity of the 9-bit CDAC, and the common centroid layout of the capacitor further improves the linearity, as shown in Fig. 9(d). The performance of this work and the state-of-the art CDCs are summarized in Table. I.

B. Bio-Signal Monitoring

Bio-signal monitoring SoCs represent one of the most prominent areas of circuit applications in the last decade. The development of bio-signal sensors for use in personal healthcare is expected to greatly improve the quality of human life and help with early detection of disease. For instance, real-time monitoring of electrocardiography (ECG) is an effective method for the diagnosis and study of heart disorders such as arrhythmia [17]. Neural signal monitoring from various regions of the brain enables the detection of neurological disorders such as epilepsy, schizophrenia, Alzheimer's disease, Parkinson's disease and autism [51].

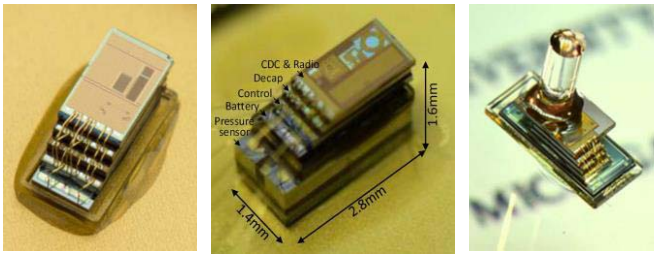
Reference [52] proposed a non-invasive multi-sensor acquisition system with simultaneous ECG, bio-impedance (BIO-Z), galvanic skin response (GSR) and photoplethysmogram (PPG) monitoring. The multi-parameter recording provides a more accurate and reliable health assessment in a comfortable wearable device.

There has been high demand for technologies to enable simultaneous monitoring of a large number of neurons, and multi electrode neural recoding is becoming standard practice [22], [33], [37], [40], [41], [53]–[61]. In this way, it is

TABLE I
PERFORMANCE SUMMARY OF STATE-OF-THE-ART CDCS

	[48] Y. He ISSCC 2015	[48] Ha, ISSCC 2014	[49] Oh, VLSI 2014	[16] Oh, ESSCIRC 2014	[35] Tan, JSSC 2013	[46] Xia, ISSCC 2012	[50] Nizza, TCAS-I 2013
Method	PM	SAR	IΣΔ	Dual Slope	ΣΔ	ΣΔ	PM
Power (μW)	14	0.16	33.7	0.11	10.3	14900	84
Input Range (pF)	0 – 8	2.5-75.3[2]	8.4-11.6	5.3-30.7	0.54-1.06	8.4-11.6	0.5-0.76
Meas. Time (ms)	0.21	4	0.23	6.4	0.8	20	0.033
Resolution (Crms, aF)	1443	6000	156	-	70	65	800
SNR (dB) [1]	65.57	60.6	94.7	44.2	68.4	84.83	40.9
FoM (pJ/step)	1.87	0.54-1.3[3]	0.18	5.3[3]	3.8	21	0.52
Area (mm^2)	0.05	0.49	0.456	0.105	0.28	2.6	98
Technology	0.16μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.16μm CMOS	0.35μm CMOS	0.32μm CMOS

[1] $\text{SNR} = 6.02 \times \text{ENOB} + 1.76$
[2] Composed of 8 subranges
[3] FoM with one subrange



(a) (b) (c)

Fig. 10. Examples of mm-scale sensor nodes for (a) temperature, (b) pressure, and (c) image sensing.

possible to gather enough information from a specific part of the brain related to motor planning and control, enabling direct control of a robotic manipulator by cortical neurons.

The read-out circuits must be designed to consume ultra-low power in order to avoid tissue damage caused by heat. Area is another challenge of the read-out circuits. The read-out circuit needs to provide sufficient immunity to the environmental noise caused by the electrochemical behavior of its surroundings, requiring a high power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR). The input referred noise specification is also challenging. The peak spike voltage of the action potential (AP) of a neuron is 50-500 μV in the 0.1-700 kHz frequency range [62]. Therefore, 2-3 μV_{rms} input referred noise is demanded for neural recoding read-out circuits. The amplitude of the local field potential (LFP) can be as high as 5 mV [63], but its ultra-low frequency near sub-Hz makes it difficult to meet the noise specification due to the large device flicker noise. Pseudo-resistors (section II-C) are widely used to implement large time constants, and the current reuse technique (section II-D) is useful for minimizing power consumption while meeting a low noise specification. Performance summary of the recently published neural recording front-end circuits is presented in Table II.

C. Modular Design

Ultra-low power sensor nodes can be used in a wide variety of applications, but the basic operation mechanisms are similar, requiring common building blocks such as a wake-up

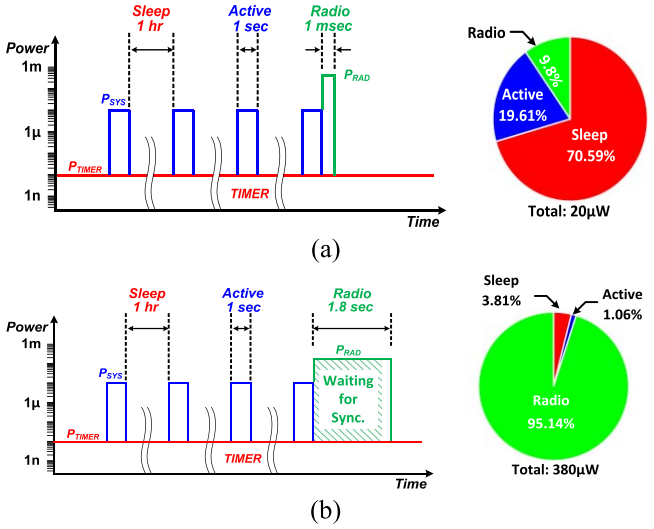


Fig. 11. Timing diagrams of a wireless sensor node (a) without timing uncertainty (b) with timing uncertainty.

timer, RF or optical communication, an energy harvester and a power management unit. Therefore, the modular design of each functional block can reduce the development time, verification overhead and manufacturing cost. Fig. 10 shows millimeter-scale wireless sensor node designs for temperature monitoring [2], pressure monitoring [16] and imaging [4] developed based on a generic sensing platform [3].

IV. TIMING REFERENCE

The reduction of sleep power is critical to make a system sustainable with limited harvested energy. Wake-up timers are a key always-on building block that can dominate the sleep power. Therefore, a wake-up timer must be designed with a stringent power budget [21], [64]–[69]. A highly accurate timing reference is also important if the sensor node is required to maintain synchronization for peer-to-peer or asymmetric communications. As an example, Fig. 11(a) shows a timing diagram of two wireless sensor nodes that need to communicate with each other. Each sensor node sleeps for an hour and then wakes up for 100 ms to collect and process data. The data

TABLE II
PERFORMANCE SUMMARY OF ANALOG FRONT-END CIRCUITS FOR NEURAL RECORDING APPLICATION

	[56] Muller, ISSCC 2014	[30] ChandraKumar, ISSCC 2016	[57] Ng, ISSCC 2015	[58] Lopez, ISSCC 2013	[59] Walker, VLSI 2011	[60] Majidzadeh, TBCAS 2011	[61] Abdelhalim, JSSC 2013
Power (μW/ch)	2.3	2	2.8	10.48	68	7.192	10
Supply (V)	-	1.2	1	1.8	1.2	1.8	1.2
Recoding Signal	ECoG	AP + LFP	AP	AP+LFP	AP+LFP	AP	AP+LFP
Bandwidth (Hz)	500[1]	1-5000	1-8200	0.5-6000	280-10000	10-7200	1-5000
Max Input Offset (mV)	100	40	220	-	15	5.7	-
Input referred Noise (μV)	1.3[1]	2[2] - 7[3]	4.2	3.2[4] – 5.8[5]	2.2	3.5	5.1
Input Impedance (MΩ)	28	300	-	-	-	-	-
NEF	4.76	7[2] – 4.9[3]	2.93	2.72	4.5	3.35	4.4
PSRR (dB)	67	-	78	76	-	63.8	-
CMRR (dB)	88	-	80	60	-	70.1	78
THD (dB)	-	-74	1 (%)	1 (%)	-	1 (%)	-50
Area (mm^2)	-	0.071	0.042	-	0.26	0.0625	-
Technology	0.065μm	0.04μm	0.065μm	0.18μm	0.13μm	0.18μm	0.13μm

[1] Calculated from Fig. 24.1.4
[2] Measured in LFP mode (1-200Hz)
[3] Measured in AP mode (200-5000Hz)
[4] Measured in AP mode (300-6000Hz)
[5] Measured in LFP mode (0.5-200Hz)

is transmitted every 4 hours. The power consumptions during sleep, active and radio modes are 10 nW, 10 uW and 2 mW, respectively. In this case study, the energy consumption in the sleep mode is the dominant factor, emphasizing the need for an ultra-low power wake-up timer. In contrast, the energy loss due to timing uncertainty is more pronounced with the presence of timing mismatch, as shown in Fig. 11(b). When the temperature coefficient is 50 ppm/°, and the temperature difference is 10°, the timing uncertainty is 500 ppm, which corresponds to 1.8 sec. This timing uncertainty causes significant energy loss for a sensor node that has to keep transmitting data until its peer responds.

A crystal oscillator is a viable option to achieve such aggressive power and accuracy specifications. Recently, a pulsed driver technique published for 32-kHz crystal oscillators reduced power consumption drastically, allowing crystal oscillators to provide an accurate frequency of less than 100 ppm across wide PVT variations while consuming only a few nano watts [70], [71]. However, crystal oscillators require an off-chip component, which is difficult to integrate in a millimeter-scale sensor node [64].

On-chip clock generation techniques are useful when the system may allow frequency uncertainty higher than 500 ppm. Fig. 12 shows the power consumption of recently published on-chip oscillators and their temperature coefficients. Gate leakage-based oscillators offer sub-nW power consumption. However, their oscillation frequencies can be as low as a few hertz, and the frequency uncertainty is very high (>10,000 ppm). Relaxation oscillators using an R-C time constant generally offer moderate temperature coefficients of tens of ppm/° with nano watt to micro watt power consumption.

In this section, we will discuss recent developments in crystal and on-chip oscillators and discuss their advantages with respect to use in millimeter-scale wireless sensor nodes.

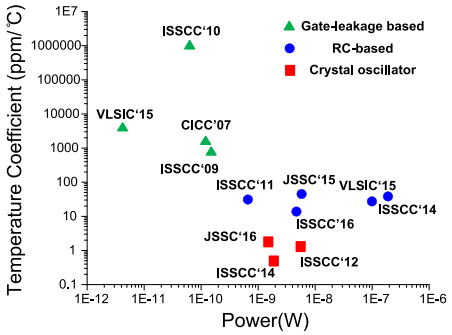


Fig. 12. Summary of temperature coefficients and the power consumption of the recently published on-chip oscillators.

A. Crystal Oscillator

Conventionally, a crystal resonator is driven by an inverter-based amplifier in series with a resistor. However, there are many sources of energy waste in such architectures. Most notably, the inverter consumes static power due to the sinusoidal input voltage. The series resistance also dissipates a significant amount of power due to the large voltage imposed on it. A current-starved driver is proposed to minimize the static power and eliminate the series resistor [72]. The limited oscillation amplitude achieved using the current-starved driver reduces the power consumption drastically, but power consumption remains higher than 27 nW [72], [73], which is too large for integration into recent millimeter-scale wireless sensor nodes consuming less than 10 nW during sleep mode [3], [74].

A pulsed driver for an ultra-low power crystal is proposed in [70] and [75]. Fig. 13 shows a simplified circuit diagram of the crystal driver. One of the crystal voltages, OSC_{IN}, is amplified and delivered to a delay-locked loop (DLL). The DLL generates two narrow pulses that are located at the peaks

TABLE III
PERFORMANCE SUMMARY OF ON-CHIP OSCILLATORS

	[21] Jang, ISSCC 2016	[64] Jeong, JSSC 2015	[65] Paidimarri, ISSCC 2013	[66] Griffith, ISSCC 2014	[67] Choi, VLSI 2015	[68] Tokairin, VLSI 2012	[69] Lee, ISSCC 2011
Frequency (Hz)	3,000	11	18,500	33,000	70,400	100,000	0.37
TC (ppm/°C)[1]	13.8	45	38.5	38.2	27.4	104.6	375(31[2])
Temperature Range	-25-85	-10-90	-40-90	-20-90	-40-80	-40-90	-20-60
Line Sensitivity (%/V)	0.48	1	1	0.09	0.5	9.4	490
Power (nW)	4.7	5.8	120	190	99.4	280	0.66
Energy/Cycle (pJ/Cycle)	1.6	527.27	6.49	5.76	1.41	2.8	1,738.8
Area (mm^2)	0.5	0.24	0.032	0.015	0.26	0.12	0.015
Technology	0.18 µm	0.18 µm	0.065 µm	0.065 µm	0.18 µm	0.09 µm	0.13 µm

[1] Calculated by $(f_{max}-f_{min})/f_{avg}\times 100$
[2] With 10 point calibration using temperature sensor.

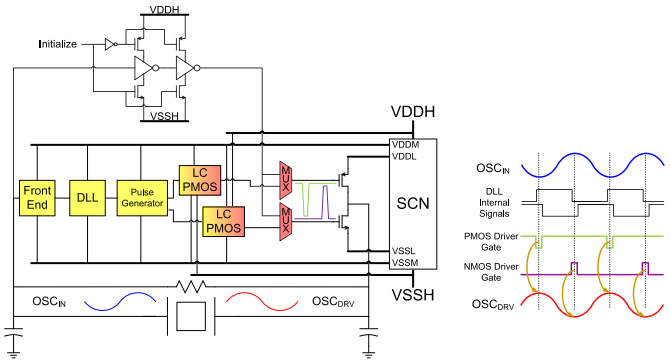


Fig. 13. Block diagram of a pulse injection based crystal driver proposed in [70].

of the crystal voltages, OSC_{IN} and OSC_{DRV}. Then, a level converter shifts those pulses to a higher magnitude, and M_{P1} and M_{N1} are driven by the pulses. There are several advantages provided by this architecture in terms of power consumption. First, the crystal amplitude is restricted to 180 mV, which reduces the power consumption of the crystal series resistance. Second, the static power consumption of the driver switches is very low because the transistors receive rectangular pulses, and only one of M_{N1} and M_{P1} is enabled so that the leakage current though each transistor is very small. Third, the driver switch is only enabled when OSC_{DRV} reaches its peak voltage. Therefore, the voltage across the driver switches is small, and most of the energy derived from the supply, E_{VDD}, is delivered to the crystal to regenerate the waveform. According to eq. (19) and Fig. 12 in [70], when the drivers are properly sized, approximately 90% of the energy is used to regenerate the waveform of the crystal, and only 10% is dissipated by the driver circuit. With the supplementary circuits of a DLL, amplifier, pulse generators and level converters, this work achieved 5.58 nW power consumption, which is a 4.8× reduction compared with prior works.

B. On-Chip Oscillator

Conventionally, on-chip oscillators are developed using a time constant provided by a monolithic resistance and capacitance pair as shown in Fig. 14(a). The frequency of the oscillator is dominated by the R-C time constant but still

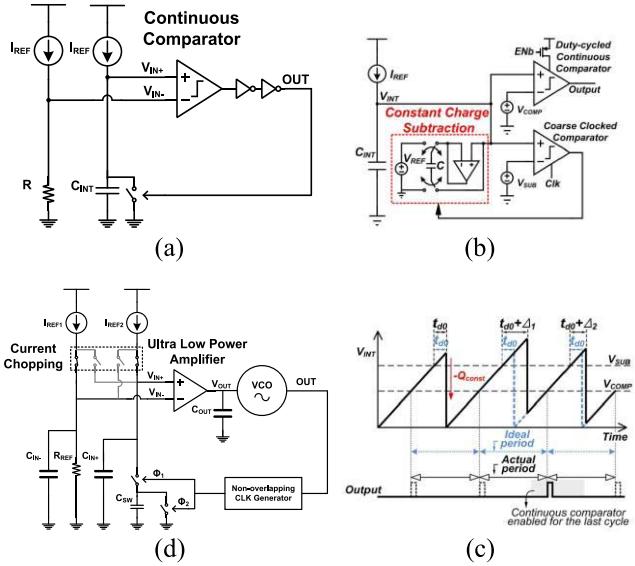


Fig. 14. (a) Conventional on-chip oscillators (b) An R-C oscillator using constant charge subtraction proposed in [63] (c) A timing diagram of the oscillator [64] (d) A resistive frequency-locking scheme proposed in [67].

affected by the comparator, buffer and reset switch delay, all of which are known to be temperature-dependent. Therefore, the delay caused by the supplementary components needs to be negligible compared with the R-C delay, which consumes a substantial amount of power.

Reference [65] introduces a constant charge subtraction method to eliminate the frequency dependency stemming from the comparator delay as shown in Fig. 14(b). A constant current, I_{REF}, generated by a temperature-compensated resistor is provided to an integration capacitor, C_{INT}. Instead of the conventional approach of fully discharging the capacitor, a constant amount of charge, $V_{REF}\times C$, is subtracted from C_{INT} when V_{INT} exceeds V_{SUB}. Therefore, the voltage drop by the charge subtraction operation is always $V_{REF}\times C/C_{INT}$, and thus the time moment that V_{INT} crosses V_{COMP} is independent of the comparator delay. The output frequency is generated using a duty-cycled continuous time comparator.

Reference [64] introduces a resistive frequency-locking method that eliminates the comparator as shown in Fig. 14(d).

In this architecture the impedance of a switched capacitor is equalized to a temperature-compensated resistor by using a frequency-locked loop implemented with an ultra-low power amplifier. A wake-up timer that further reduces the power consumption using a frequency-locked loop and a duty-cycled resistor is proposed in [21].

The performances of recently published low power on-chip oscillators are summarized in Table-III.

C. Frequency Synthesis

A simple ring oscillator used as a frequency generator is acceptable in a processor despite the wide frequency variations observed in response to environmental changes. This observation is true because the throughput of a sensor node is determined by the sensor interface circuits rather than the processor speed. However, the change in the processor frequency results in increased energy consumed by the processor core because the active time is usually determined not by the workload of the processor core but by the sensor signal acquisition time. Therefore, the core frequency needs to be stabilized by locking it to an accurate wake-up timer.

A phase-locked loop (PLL) using a frequency reference generated by either a crystal or wake-up oscillator is a viable option to reduce the power overhead caused by excessive frequency. A charge-pump PLL, which is the most generic architecture for SoC clock generation, is not well suited for this purpose for several reasons. First, the VCO frequency tuning range is limited due to the low supply voltage. Many wireless sensor nodes operate with a supply voltage close to the MOS threshold voltage to reduce power consumption [76]. Under these conditions, the control voltage range is very limited because of the small charge pump output range resulting from the low supply voltage. Furthermore, the delay cells in the VCO operate in a subthreshold region in order to generate low frequencies, resulting in wide frequency variations depending on the temperature and process changes, thereby requiring an even larger control voltage range to compensate for the frequency change. Second, the size of the loop filter consumes a substantial amount of space. A sensor node wake-up timer typically generates only a few kHz to minimize its energy overhead during the sleep period. The loop bandwidth of a PLL should be smaller than one-tenth of the reference frequency [77] and result in either a very small charge pump current or a very large loop filter capacitance. On the other hand, a digital PLL scales well to the lower loop bandwidth as its loop filter coefficients are represented as digital values. For example, a digital loop filter of an all-digital PLL receiving 32kHz reference clock [78] is implemented with 14-bit words and its area occupation is 7-to-56x smaller compared to the analog implementation mostly due to the absence of the analog loop filter ([78], Table-V). Also, the DCO frequency tuning range is less affected by the low supply voltage. In addition, the frequency tuning code of a digital PLL can be easily stored in memory and can be directly used when the system wakes up from sleep mode, reducing the lock time. Therefore, a digital PLL is better suited for the frequency synthesizers in miniaturized systems.

V. Conclusion

Miniaturized sensor nodes have applications in fields such as medicine, environmental monitoring and surveillance. Ultra-low power circuit techniques have emerged as critical tools to accelerate the miniaturization of sensor nodes due to the limited energy and power budget resulting from the small battery size and the harvester capability. In Part I of this two-part paper, we described key front-end circuits, including analog references, amplifiers and clock generators, of sensor nodes and their design challenges. Further, recently proposed ultra-low power circuit schemes to overcome such challenges and realize miniaturized sensor nodes are reviewed.

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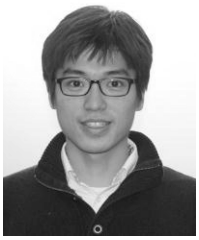

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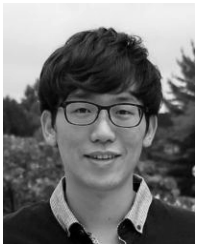

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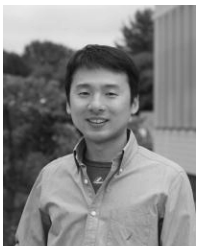

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