Battery Voltage Supervisors for Miniature IoT Systems

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***Abstract*— As battery size decreases due to system size constraints in miniature Internet-of-things systems, the internal resistance of the battery increases, resulting in a large IR drop on the battery voltage, complicating battery supervising functions. In this paper, we discuss low-power battery voltage supervisors (BVSs) that are capable of handling this increased IR drop. Battery voltage, battery internal resistance, required threshold voltages, and power-on-reset delay are discussed. As examples, two low-power BVSs fabricated in a 180 nm CMOS process are described.**

***Index Terms*— Battery internal resistance, battery voltage supervisor (BVS), brown out detector, energy harvester, Internet of things (IoT), low power, power on reset, wireless sensor node.**

I. Introduction

RAPID advances in miniature Internet-of-things (IoT) systems have prompted studies investigating their potential use in new embedded application areas, including medical, security, and resource exploration [1]–[5]. IoT systems often include an energy harvester that derives energy from a source (e.g., a solar cell) and transfers it to a battery, as shown in Fig. 1. The battery voltage (V_{BAT}) varies over time depending on the amount of harvested energy versus the system energy consumption.

To avoid unpredictable circuit behavior and permanent damage to a battery, a battery voltage supervisor (BVS) monitors V_{BAT} and only enables the system when V_{BAT} exceeds a threshold (V_{ON}), as shown in Fig. 2. To prevent oscillation due to circuit noise and error, conventional BVSs employ two fixed threshold voltages with a voltage difference of 1–10 mV [6]–[10]. The lower threshold voltage (V_{OFF}) sets the lowest V_{BAT} at which circuits operate properly and do not damage the battery. The higher threshold voltage (V_{ON}) provides hysteresis ($V_{HYST} = V_{ON} - V_{OFF}$) to prevent the system from oscillating between the operation and reset modes. A voltage regulator cannot be an alternative of BVS since it does not prevent the battery from being discharged below the voltage that causes permanent damage to a battery.

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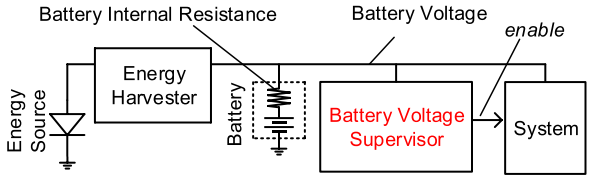


Fig. 1. IoT system with BVS.

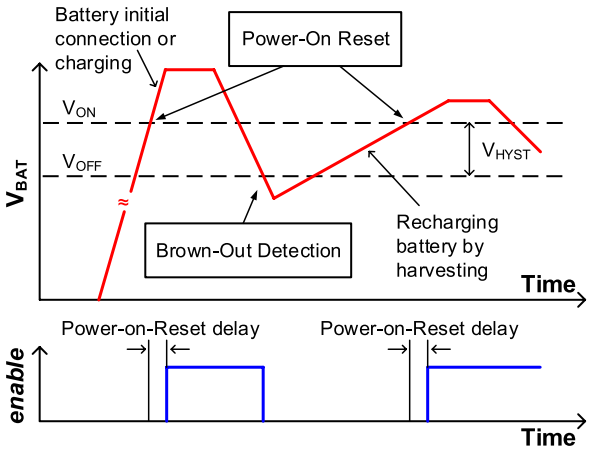


Fig. 2. Conceptual BVS operation according to V_{BAT}.

The constant small V_{HYST} in conventional BVSs cannot handle the V_{BAT} of advanced miniature IoT systems, where the instant current consumption in the operation mode can be significantly larger than in the reset mode. In operation mode, a large instant power is necessary for transmitting data through a wireless radio link. In reset mode, only a small amount of power is required for an energy harvester to charge a battery above V_{ON} even in a low-energy environment. For example, the system introduced in [11] consumes 10 μA as the maximum in operation mode and less than 2 nA in reset mode. This significant current difference results in a considerable *IR* drop on V_{BAT}. If the *IR* drop is larger than V_{HYST}, the system becomes unstable and oscillates between ON and OFF as shown in Fig. 3. This is because V_{BAT} drops from voltage higher than V_{ON} to voltage lower than V_{OFF} in the operation mode after the BVS turns ON the system, thus turning the system OFF again.

The impact of the *IR* drop becomes more noticeable as the system size decreases since the battery internal resistance (R_{BAT}) increases as battery size decreases, as shown

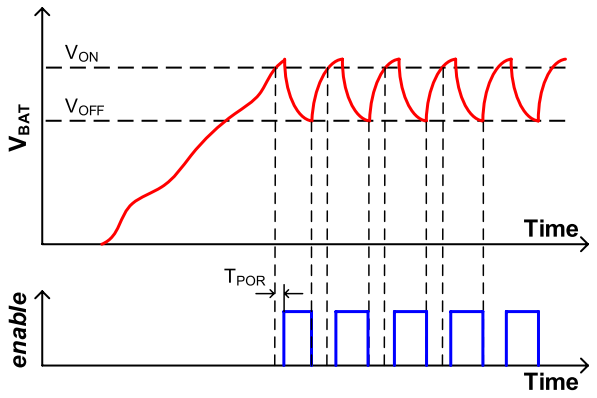


Fig. 3. System oscillation due to *IR* drop on V_{BAT} higher than V_{HYST}.

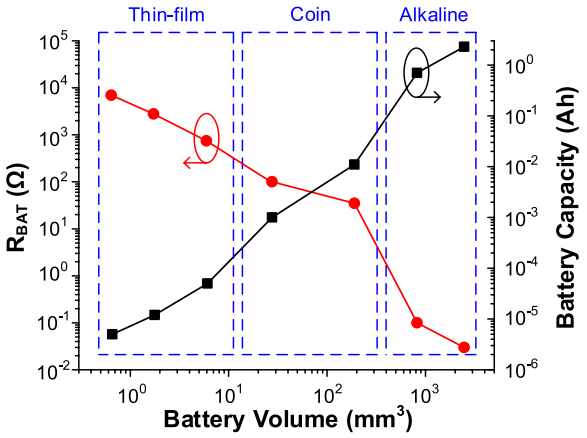


Fig. 4. R_{BAT} and battery capacity across battery volumes.

in Fig. 4 [12]–[17]. In addition, R_{BAT} increases as a battery ages over charge/discharge cycles. The increase in R_{BAT} results from solid-electrolyte interphase growth in the carbon anodes, a reduced surface area for reactions due to the loss of active material, and electrolyte degradation. Hence, R_{BAT} has been used as an indicator of battery health [18]–[20].

The *IR* drop problem has been an issue for high-power applications as well due to their large currents. To prevent system failure, uninterruptible power systems and battery management systems detect increased R_{BAT} and signal a need to replace the battery [21]–[26]. In miniature IoT systems, however, replacing batteries can be difficult due to the sheer number of IoT nodes or difficulty of access (e.g., medical implantable device). Thus, it is more important to effectively use the battery and maximize the system functional time without incurring system oscillation.

In this paper, low-power BVSs are explored that are able to handle the increased *IR* drop on V_{BAT}. A discussion of V_{BAT}, R_{BAT}, required V_{HYST}, and power-on-reset delay (T_{POR}) is included. Also, design techniques and calibration methods for V_{HYST} are discussed. As examples, two low-power BVSs fabricated in a 180 nm CMOS process are presented.

The first BVS, referred to as large-constant-hysteresis BVS (LCHBVS), is designed for a large and constant R_{BAT} [27]. With a predetermined large V_{HYST}, it solves the

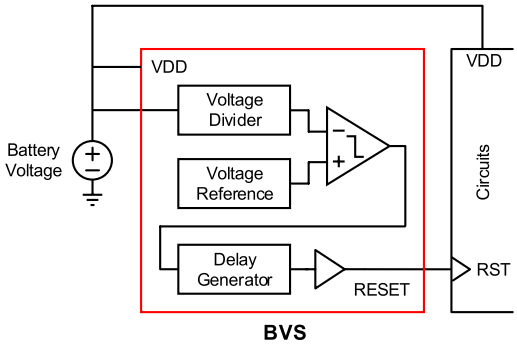


Fig. 5. Conventional BVS.

oscillation problem associated with conventional BVSs. This design can handle an R_{BAT} of up to 17 kΩ with 635 pW power consumption. The second BVS, referred to as adaptive-hysteresis BVS (AHBVS), is an extension that updates V_{HYST} according to the R_{BAT} measurement results [28]. It can tolerate large and varying R_{BAT} up to 63 kΩ with a 3.6 nW power consumption. In the target systems, R_{BAT} changes from 11 to 60 kΩ after 1000 battery charge/discharge cycles in the worst case [12]. LCHBVS is designed for the system that requires less than five battery charge/discharge cycles. The change in R_{BAT} is negligible in such limited cycles, and 17 kΩ is sufficient as the maximum R_{BAT} coverage. AHBVS is chosen for systems that seek to maximize the lifetime. With a maximum R_{BAT} coverage of 63 kΩ, the system can run for ∼1000 battery charge/discharge cycles.

LCHBVS is a simpler, lower power design than AHBVS, and thus it can be a good choice for applications that experience only a small R_{BAT} change. However, LCHBVS can be inefficient for systems with large and varying R_{BAT} since the system must wait to be charged to a high V_{ON}, reducing the system functional time. Also, it causes the system to operate at a higher V_{BAT}, which can accelerate battery health degradation. AHBVS overcomes these problems by using the adaptive V_{HYST} technique at the cost of additional circuits (i.e., R_{BAT} monitor) and 5.7× higher power.

The remainder of this paper is organized as follows. Section II provides an overview of the BVS design. Section III discusses the threshold voltages design. Section IV shows the measured results, Section V discusses calibration, and Section VI concludes this paper.

II. Overview of BVS Design

Conventional BVSs typically include a supply voltage divider, voltage reference, comparator, and T_{POR} generator [6]–[10] as shown in Fig. 5. The divided supply voltage is compared with a predetermined threshold voltage from a voltage reference by a comparator. The comparator output either immediately resets the sensor system or enables it after T_{POR}, which provides stabilization time to the circuits.

In addition to the threshold voltages (V_{ON} and V_{OFF}) discussed earlier, T_{POR} is also an important parameter for a BVS design. In an IoT system, during T_{POR}, various power voltage regulators, references, and clock generators that begin their operation regardless of BVS operation are stabilized before the

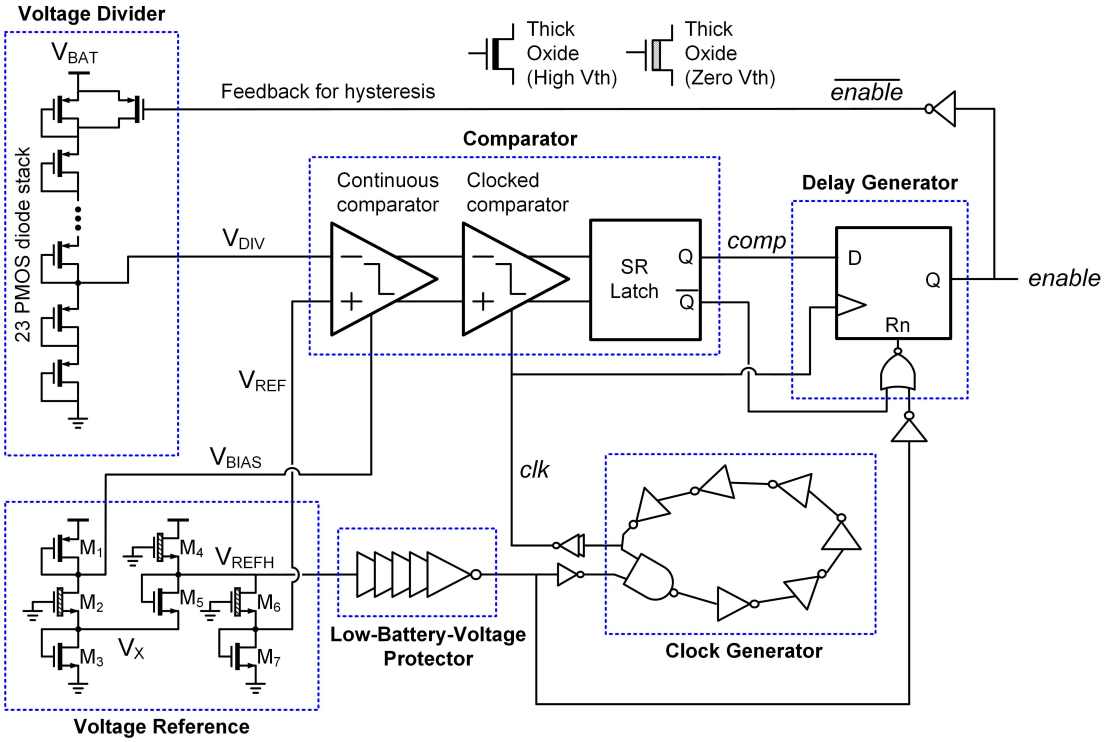


Fig. 6. Circuit diagram of LCHBVS.

BVS turns ON the system. Thus, T_{POR} should be determined by considering the time required for the circuits to stabilize.

For a shorter T_{POR}, faster delay needs to be generated and more power is required. Longer T_{POR} can reduce power and provide sufficient stabilization time to the system, at the expense of latency. For example, to meet the low system power budget, LCHBVS has 7.2× longer T_{POR} with 331× lower power compared with the conventional BVS design. Compared with using a frequency divider and a fast-frequency clock generator, generating a slow pulse is more energy efficient. Typically, a delay cell generates a slowly increasing/decreasing voltage curve with large resistance or capacitance, and it is connected to a digital logic buffer for a logic-level output and strong driving ability. However, the slowly increasing/decreasing voltage at the output of the delay cell causes large short-circuit current at an output digital buffer since it does not fully turn OFF PMOS or NMOS transistor(s) of the buffer. Instead, a ring oscillator with delay cells in [29] is used in LCHBVS to avoid the short-circuit current issue.

However, AHBVS maintains T_{POR} at a similar level as that reported for conventional BVS designs with 58× lower power. Low standby power is maintained with a power gating technique after pulse generation.

Power consumption is also critical. A BVS is one of the few components in a sensing system that continually consumes power from a battery and therefore should be accounted for in the system standby power budget. Furthermore, it should consume less energy than the energy harvested from the minimum energy environment in order to charge the battery. For instance, the 8.25 mm^2 harvester can provide 300 nW at 100 lx [30]. The harvester can charge a battery at 100 lx in the IoT system using LCHBVS or AHBVS due to their nanowatt power consumption. However, with the conventional BVS designs, charging a battery may be impossible or may take at least 2× longer than with LCHBVS or AHBVS due to higher power consumption.

III. Threshold Voltages (V_{ON}, V_{OFF}, and V_{HYST}) Design

A. Low-Power Constant V_{HYST} Generation

LCHBVS is designed for a millimeter-scale implantable pressure sensor that requires less than five battery charge/discharge cycles to remotely study the mouse behavior for approximately 2 weeks. During these few charge/discharge cycles, the change in R_{BAT} is negligible although the absolute value is high (∼10 kΩ). However, the conventional BVSs with 1–10 mV V_{HYST} cannot tolerate the *IR* drop of ∼100 mV. Thus, LCHBVS is proposed with a higher V_{HYST}.

Fig. 6 shows the circuit diagram of LCHBVS, which consumes 635 pW and is integrated in the system with 2 nA standby power [11]. In this design, the threshold voltages are implemented by adjusting the V_{BAT} divider with the output signal (*enable*). For a low-power implementation, a 23-transistor PMOS diode stack is used instead of resistors. PMOS is chosen instead of NMOS to avoid the body effect on the threshold voltage by connecting its body to the source. NMOS can also be used with the deep n-well to remove the body effect.

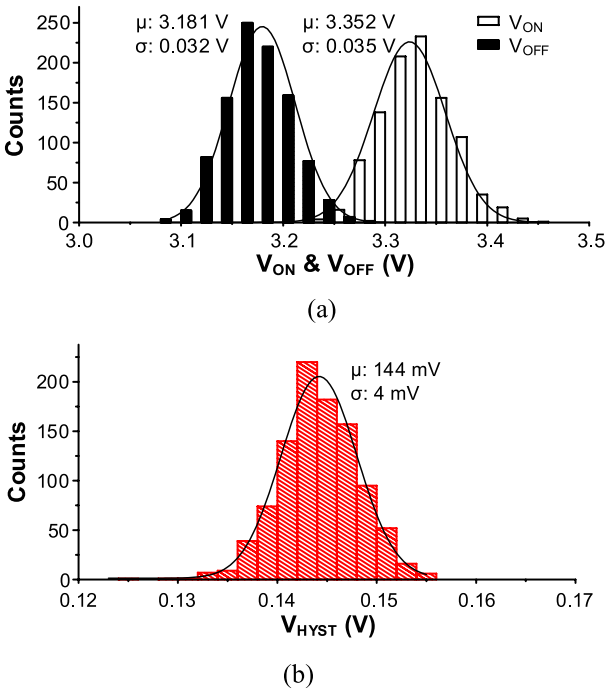


Fig. 7. Simulated impact of process variation and device mismatch on reset threshold voltages. (a) V_{ON} and V_{OFF}. (b) V_{HYST} ($=V_{ON} - V_{OFF}$).

To avoid damaging the battery, V_{BAT} needs to remain above 3.0 V after the initial charging. As shown in Fig. 7(a), V_{OFF} is chosen as 3.18 V with a 0.18 V margin considering process variation and device mismatch, and V_{ON} is set to 3.35 V with a hysteresis voltage of 0.17 V to avoid system oscillation between the operation ($enable = 1$) and reset modes ($enable = 0$). This design handles an R_{BAT} of up to 17 kΩ with a maximum current draw from the system (I_{MAX}) of 10 μA.

In Fig. 7(a), the distributions of V_{ON} and V_{OFF} overlap, but this does not imply that V_{HYST} can be negative, a situation that would lead to an unstable system. Instead, positive hysteresis is guaranteed by the structure of the V_{BAT} divider, which uses a diode stack and a switch to physically change the number of transistors connected in series [31]. As shown in Fig. 7(b), V_{HYST} is always positive even when considering device mismatch.

The transistor sizes of the diode stack are chosen by limiting the worst case power condition to less than 10% of the total LCHBVS power. With the selected sizes, V_{DIV} reaches 0.29 V in 5 ms in simulation. Thus, V_{REF} should stabilize within 5 ms to properly generate *enable*. A leakage-based voltage reference topology is used for its low power consumption [32]. However, its original implementation employs a large capacitor to ground for decoupling and noise purposes, leading to a large settling time of 7.3 ms (with 1 pF decoupling capacitor), which is slower than that observed with the V_{BAT} divider. This introduces the risk that with a fast rising V_{BAT}, V_{DIV} will temporarily exceed V_{REF} while V_{REF} is stabilizing, causing a false reset release that could be fatal to the system operation (Fig. 8).

Hence, a two-stage reference structure is proposed without the large capacitor to ground. The first stage reference

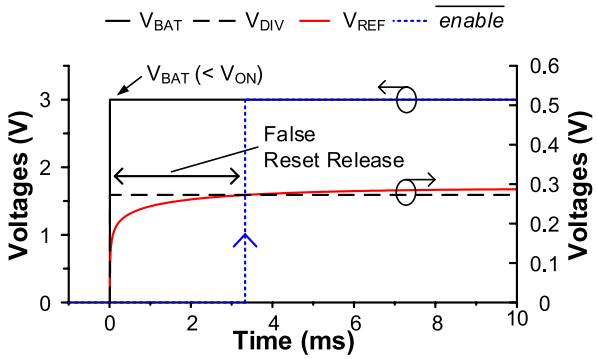


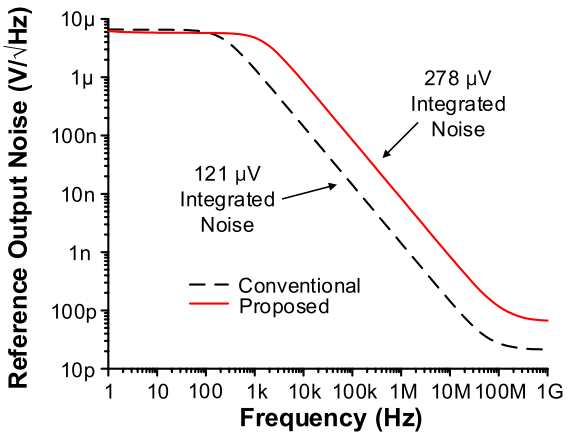
Fig. 8. False reset release using decoupling capacitor to ground in the conventional voltage reference.

(M_1–M_5 in Fig. 6) provides a reference voltage (V_{REFH}) of approximately 0.6 V by stacking the leakage-based voltage references. This acts as a voltage preconditioner and generates a supply voltage for the second reference stage (M_6, M_7), as shown in Fig. 6. This decouples the reference from V_{BAT}, which when combined with the 4× reduced gate length ensures fast stabilization (0.44 ms), with a total reference power of 58.6 pW (simulation at 4.2 V).

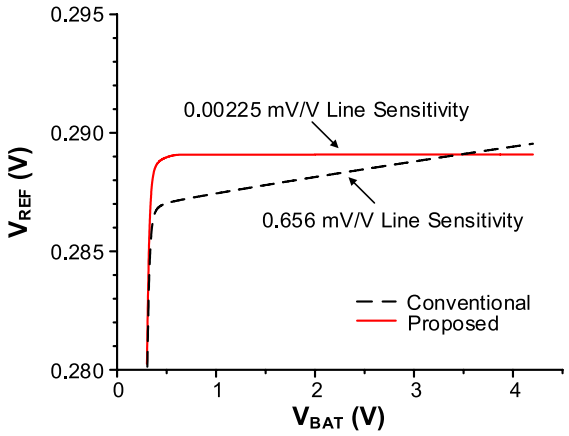
The settling time of the conventional voltage reference can be reduced by removing the decoupling capacitor. Without a 1 pF capacitor at the output, the settling time is decreased to 2.3 ms, which is 5.2× slower than the proposed reference but satisfies the requirement from the voltage divider (5 ms). The conventional approach consumes 44.4% less power (32.6 pW) than the proposed reference (58.6 pW) since it has only one current branch. As shown in Fig. 9(a), the integrated output noise is also 2.3× smaller in the conventional approach (121 μV) than the proposed approach (278 μV). In both the references, the highest and second highest noise contributors are the thermal noises from the top zero-Vth transistor (∼60%) and the bottom high-Vth transistor (∼40%), respectively. Both are in the final stage in the proposed case. The proposed reference has more integrated noise due to a 4× reduced gate length, which decreases output resistance and capacitance and thus increases the bandwidth.

However, the proposed reference improves the line sensitivity, as shown in Fig. 9(b). In the two-stage structure, the first stage dramatically reduces the effect of supply variation. As V_{BAT} changes from 1 to 4.2 V, the first stage output (V_{REFH}) has a line sensitivity of 1.914 mV/V and changes from 577.8 to 583.9 mV. Although this is worse than the conventional reference (0.656 mV/V), the supply voltage of the second stage in the proposed reference only changes by 6.1 mV, giving 292× less line sensitivity in the final output. Therefore, the proposed two-stage reference is chosen for LCHBVS despite the 2.3× noise degradation since it offers a more stable reference voltage due to its low line sensitivity.

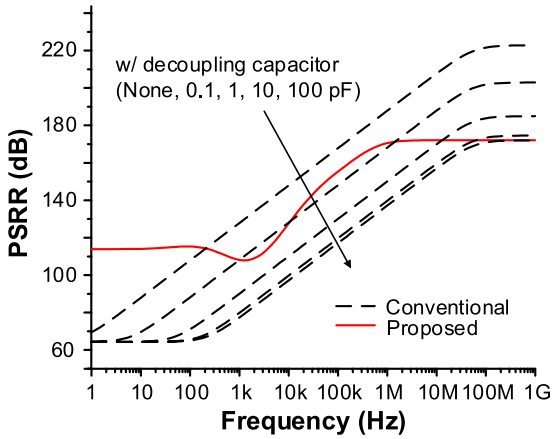
Furthermore, the proposed reference provides better power supply rejection ratio (PSRR) performance than the conventional approach, as shown in Fig. 9(c). The conventional reference has a PSRR of 64 dB at low frequency, and its decoupling capacitance at the output decides the cutoff frequency. In the



(a)



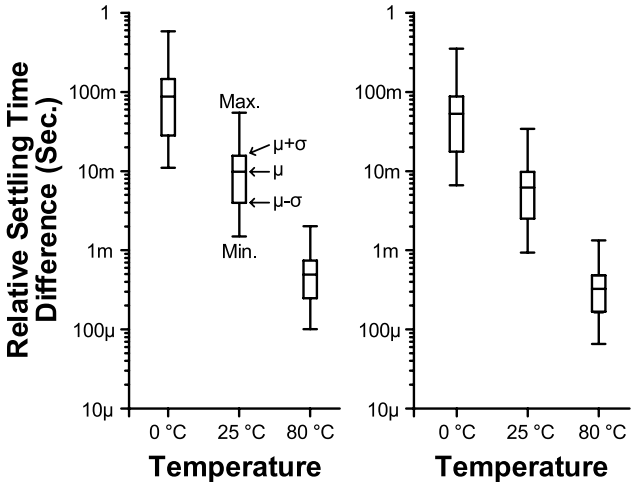
(b)



(c)

Fig. 9. Simulated conventional and proposed voltage reference. (a) Output noise. (b) Line sensitivity. (c) PSRR.

proposed reference, the fluctuation of the supply voltage is rejected twice through the two-stage structure, and the PSRR becomes 113 dB at low frequency. The proposed reference shows a 6 dB lower PSRR between 300 Hz and 10 kHz than at lower frequency since the path through C_{gd} of M_4 affects V_X (Fig. 6). However, the overall PSRR performance is compatible with the conventional design using a decoupling capacitor of 10 pF up to 1 MHz.



(a) (b)

Fig. 10. Simulated relative settling time difference (settling time of V_{DIV}–settling time of V_{REF}). (a) 3.8 V. (b) 4.2 V.

The relative settling time difference between V_{DIV} and V_{REF} is critical since the race condition of the two signals can cause an incorrect reset operation. As shown in Fig. 10, V_{REF} always stabilizes faster than V_{DIV} under simulations of all temperatures, voltages, and process and mismatch conditions. The minimum margin in the worst case condition (80 °C and 4.2 V) is 65 μs and demonstrates that the design can work properly when the system starts up.

B. Adaptive V_{HYST} Generation

For general applications that require more charge/discharge cycles and experience large and varying R_{BAT}, LCHBVS using a constant V_{HYST} is not efficient, as discussed earlier. AHBVS overcomes the issues in LCHBVS for the condition by keeping V_{HYST} low when R_{BAT} is low and increasing it when R_{BAT} is high to avoid oscillation. Fig. 11(a) shows the circuit diagram of AHBVS, which updates V_{ON} and thus V_{HYST} by measuring R_{BAT}.

In AHBVS, a diode stack is used to increase the offset of V_{HYST} (212 mV), similar to LCHBVS for the condition in which the harvested energy is less than the energy consumption of the system. For fine modification of V_{HYST} (64 values with 11 mV step), a multiple-output voltage reference with an analog multiplexer is used. Here, we will focus on how R_{BAT} is measured to control the voltage reference and adjust V_{HYST}.

As shown in Fig. 11(b), the R_{BAT} monitor consists of a test current generator, an RC response calculator, and a system isolation block. The R_{BAT} monitor creates an RC curve to measure R_{BAT} [Fig. 11(c)]. The test current generator consists of eight test capacitors (C_{T1}–C_{T8}, the same capacitance of C_T) and switches as shown in Fig. 12. Under normal conditions when R_{BAT} is not measured, the test capacitors are connected between V_{BAT} and ground in parallel and act as decoupling capacitors as default. To discharge the test capacitors in preparation for an RC curve generation, the proposed circuit stacks the test capacitors, which will be explained later.

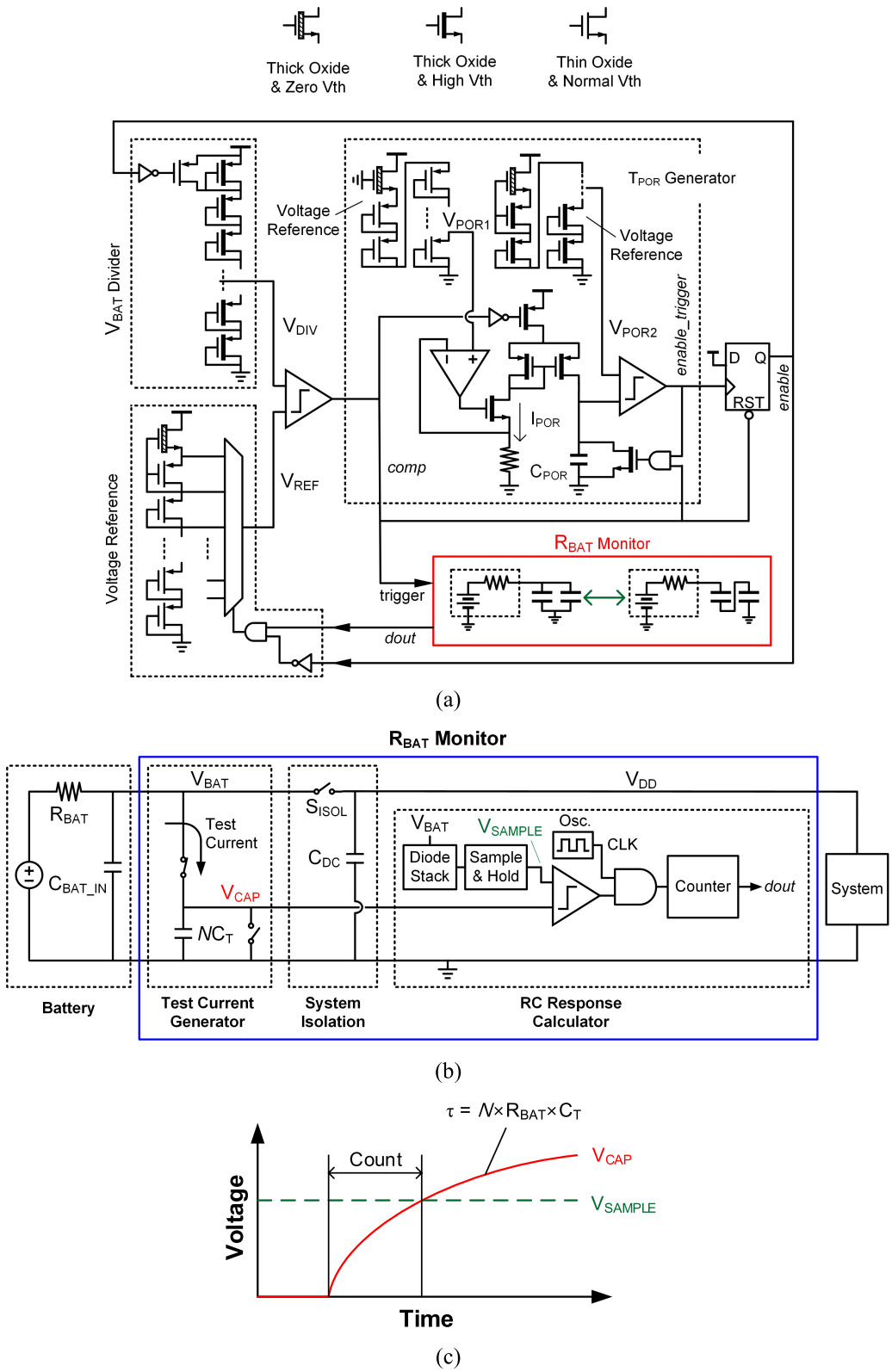


Fig. 11. Circuit diagram of AHBVS. (a) BVS. (b) R_{BAT} monitor. (c) Conceptual operation of R_{BAT} monitor.

After the discharge process, to generate an *RC* curve, all the test capacitors are connected to the battery and ground at once.

By drawing the test current from the battery, V_{CAP} generates an *RC* curve, which is used to calculate R_{BAT}, as shown in Fig. 11(c). The *RC* curve on V_{CAP} is sent to the *RC*-response calculator [Fig. 11(b)]. It consists of a diode stack and a sample and hold circuit to set the reference voltage (V_{SAMPLE}), a comparator to compare *RC* response to the reference voltage,

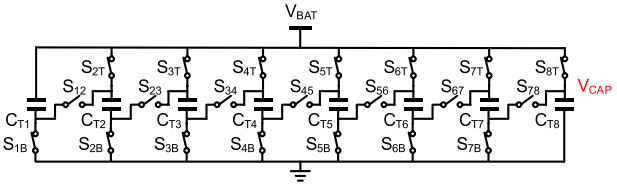


Fig. 12. Circuit diagram of test current generator.

and an oscillator and a counter to record RC delay. First, the sample and hold circuit closes a sampling switch such that the divided V_{BAT} is tracked on a capacitor as V_{SAMPLE}. Before the RC curve generation, the sampling switch is open in order to hold the divided V_{BAT} before V_{BAT} drops suddenly low. Once V_{CAP} generates the RC curve, the counter number is incremented by the clock of the oscillator until V_{CAP} crosses V_{SAMPLE}. Then, the digital output of the counter represents R_{BAT}.

The advantage of using divided V_{BAT} as a reference is that the measured R_{BAT} becomes insensitive to the absolute V_{BAT}. The RC curve on V_{CAP} and V_{SAMPLE} can be expressed as follows:

$$\begin{aligned} V_{CAP}(t) &= V_{CAP0} + (V_{BAT} - V_{CAP0})(1 - e^{-\frac{t}{NR_{BAT}C_T}}) \\ V_{SAMPLE} &= kV_{BAT} \\ T_{SAMPLE} &= -NR_{BAT}C_T \ln\left(1 - \frac{V_{SAMPLE} - V_{CAP0}}{V_{BAT} - V_{CAP0}}\right). \end{aligned} \quad (1)$$

Here, V_{CAP0} is the initial voltage of V_{CAP}, N is the number of test capacitors, k is the division factor of V_{SAMPLE}, and T_{SAMPLE} is the time taken for V_{CAP} to reach V_{SAMPLE}. In this design, V_{SAMPLE} and V_{CAP0} are fixed fractions (k and $1/N$) of V_{BAT} by the diode stack and the discharge process, respectively. Thus, T_{SAMPLE} (thus R_{BAT} measured) is independent of the absolute V_{BAT}.

During RC curve generation, V_{BAT} can drop too low to support the circuits. Hence, a system isolation block is added. Usually, the isolation switch is closed, and the battery supports the system circuits. However, during RC curve generation, the isolation switch is open, and the system operates from the decoupling capacitor for a short duration. In the system where AHBVS is applied, for a 10% system supply voltage drop, 7 nF decoupling capacitance (measured) is required.

In the discharge process of the test capacitors, the proposed circuit shown in Fig. 12 gradually stacks the test capacitors to avoid a large overshoot on V_{BAT}, as shown in Fig. 13. By disconnecting S_{1B} and S_{2T} and connecting S_{12}, the voltage across the capacitors and the charges on the capacitor are reduced by half. As more test capacitors are stacked, V_{CAP} is decreased. Once all the capacitors are connected in series, the discharge process is complete.

Rather than directly discharging the capacitor to ground, this approach sends the extracted charge to the battery for recycling. Initially, each test capacitor contains $C_T V_{BAT}$. After the capacitor stacking process, only $(1/8)C_T V_{BAT}$ remains in the capacitor for reuse.

Instead of generating a rising RC curve, a falling curve from V_{BAT} to $(1/8)V_{BAT}$ can be used without the discharging process by stacking all of the capacitors at once. However,

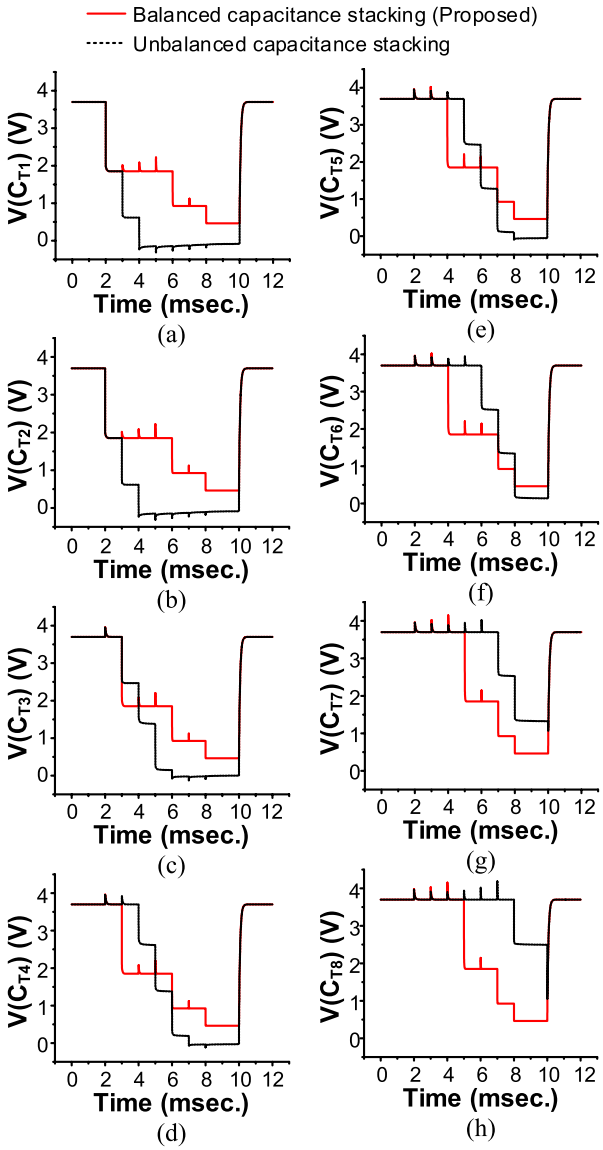


Fig. 13. Voltage across each test capacitor with two different discharging processes. (a) C_{T1}. (b) C_{T2}. (c) C_{T3}. (d) C_{T4}. (e) C_{T5}. (f) C_{T6}. (g) C_{T7}. (h) C_{T8}.

its time constant is 64× shorter than the proposed approach due to the total capacitance difference [$(1/8)C_T$ versus $8C_T$], which makes R_{BAT} measurement more difficult. Also, the instant capacitor stacking causes overshoot on V_{BAT} as shown in Fig. 14, which can damage the battery and system circuits. The overshoot depends on battery input capacitance (C_{BAT_IN}), R_{BAT}, and resistance of the switches (R_{SW}). C_{BAT_IN} is the capacitance between V_{BAT} and ground [Fig. 11(b)]. C_{BAT_IN} and R_{SW} reduce the overshoot voltage by charge sharing and energy loss, respectively. R_{BAT} weakens control of the battery on V_{BAT} and increases the voltage spike. For example, the overshoot can be 46.8% of V_{BAT} with 63 kΩ R_{BAT} and 10 pF C_{BAT_IN} in this design if all of the testing capacitors are stacked concurrently. The overshoot problem can also occur if instant stacking is used for the discharging process.

The overshoot depends on the stacking sequence. Fig. 13 shows two different ways to discharge the test capacitors gradually. In the balanced capacitance stacking, the test current

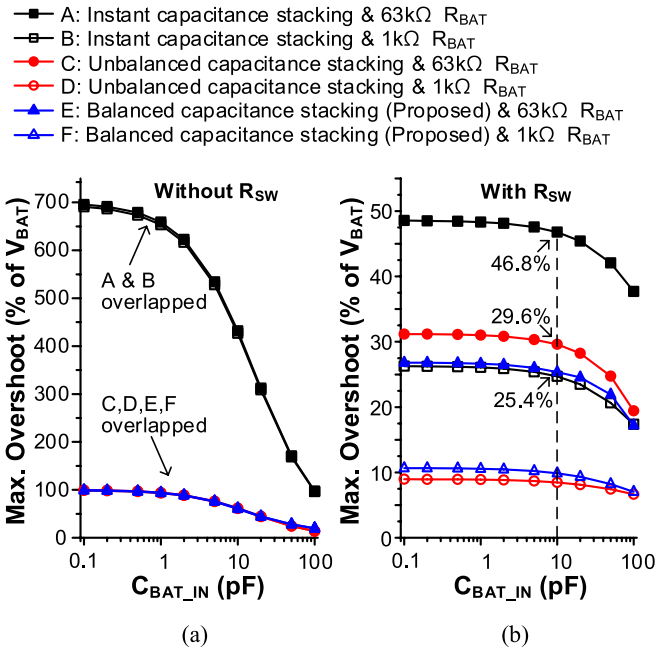


Fig. 14. Simulated overshoot on V_{BAT} (a) without R_{SW} and (b) with R_{SW}.

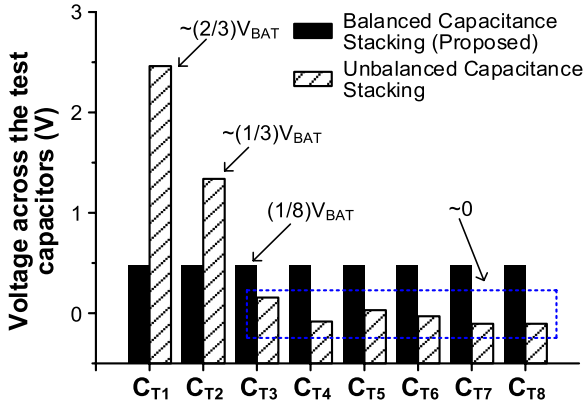


Fig. 15. Simulated voltages across test capacitors after discharging processes.

generator always connects two groups of capacitors, each with the same number of capacitors. In the unbalanced capacitance stacking, however, it adds one capacitor to a stack. To find the voltage across the capacitors, consider two capacitors with capacitances C_1 and C_2. They are initially charged to V_A and connected in series, and V_A is imposed on the stack. The charge movement in each capacitor can be expressed as follows:

$$C_1V_A - \Delta Q = C_1(V_A - V_B), \quad C_2V_A - \Delta Q = C_2V_B. \tag{2}$$

Here, ΔQ is the extracted charge from each capacitor, and V_B is the node voltage between the two capacitors. From (2), $\Delta Q = C_1V_B$ and $V_B = (C_2/(C_1 + C_2))V_A$. Thus, the voltage across the capacitors depends on the capacitance of the two capacitors.

In the balanced capacitance stacking, two capacitors with matched capacitance are stacked, resulting in constant voltages, as shown in Fig. 15. In contrast, the unbalanced capacitance stacking stacks capacitors with different capacitance, and the voltages vary. When three capacitors are stacked, C_{T6}, C_{T7}, and C_{T8} have $(2/3)V_{\mathrm{BAT}}$, $(1/6)V_{\mathrm{BAT}}$, and $(1/6)V_{\mathrm{BAT}}$, respectively. By connecting C_{T5} on top of them, the voltage across C_{T7} and C_{T8} becomes $(-1/6)V_{\mathrm{BAT}}$ according to (1), but the body of NMOS transistors in the switches prevents a negative voltage. Thus, C_{T5} and C_{T6} have $(2/3)V_{\mathrm{BAT}}$ and $(1/3)V_{\mathrm{BAT}}$, respectively, while the other capacitors have approximately zero voltage across them. Next, a new capacitor with V_{BAT} is stacked, and all the voltages are reduced by $(1/3)V_{\mathrm{BAT}}$. Again, two capacitors have $(2/3)V_{\mathrm{BAT}}$ and $(1/3)V_{\mathrm{BAT}}$, while the other capacitors have approximately zero voltage. In the final step, as shown in Fig. 15, C_{T1} and C_{T2} have $\sim(2/3)V_{\mathrm{BAT}}$ and $\sim(1/3)V_{\mathrm{BAT}}$, and the other capacitors have approximately zero voltage.

The proposed balanced capacitance stacking is chosen in AHBVS since it reduces the overshoot compared with the unbalanced capacitance stacking as shown in Fig. 14. For example, the overshoot is decreased by 45.7% and 14.2% compared with the instant and unbalanced capacitance stacking, respectively, with 63 kΩ R_{BAT} and 10 pF $C_{\mathrm{BAT\_IN}}$. The balanced and unbalanced capacitance stacking methods have the maximum overshoot on V_{BAT} at the final stacking step since a decoupling capacitor no longer exists. However, the proposed approach has less ΔQ ($(1/8)C_TV_{\mathrm{BAT}}$ versus $(1/3)C_TV_{\mathrm{BAT}}$), and the battery suppresses the overshoot faster.

After the discharging process, the energy stored in the eight test capacitors is reduced from $4C_TV_{\mathrm{BAT}}^2$ to $(1/14)C_TV_{\mathrm{BAT}}^2$ (98% energy loss). However, as shown in Fig. 16, the energy loss can be reduced by 41%–44% in the proposed gradual discharging process compared with a method discharging a single large capacitor without stacking. The proposed technique sends the charge to the battery when two, four, and eight test capacitors are connected in series. The overshoot on V_{BAT} results in energy loss through R_{BAT}. Thus, the energy saved by the charge recycling depends on the stacking method, $C_{\mathrm{BAT\_IN}}$, and R_{BAT}. This savings can offset the increased design complexity and power consumption required to manipulate more capacitors. The technique helps send more energy to the battery and can save the total energy consumption from the battery, but it does not increase energy stored in the capacitors.

The number of capacitors (N) and their capacitance (C_T) are decided considering the voltage across the discharged capacitors, $C_{\mathrm{BAT\_IN}}$, discharge process time, and switching complexity. The voltages over the capacitors are lowered to V_{BAT}/N. A lower capacitor voltage increases the voltage range of the RC curve and helps the comparison with the reference voltage. $C_{\mathrm{BAT\_IN}}$ is not discharged in the discharge process as the test capacitors are and maintains a voltage of V_{BAT}. This reduces the voltage range of the RC curve. In this design, the total capacitance is limited by the silicon area, and N and C_T are chosen to be 8 and 130 pF, respectively. With 80 pF $C_{\mathrm{BAT\_IN}}$ (from the used battery), 93.3% of the ideal voltage range is achieved, as shown in Fig. 17. N is limited to eight considering design complexity with switches and control.

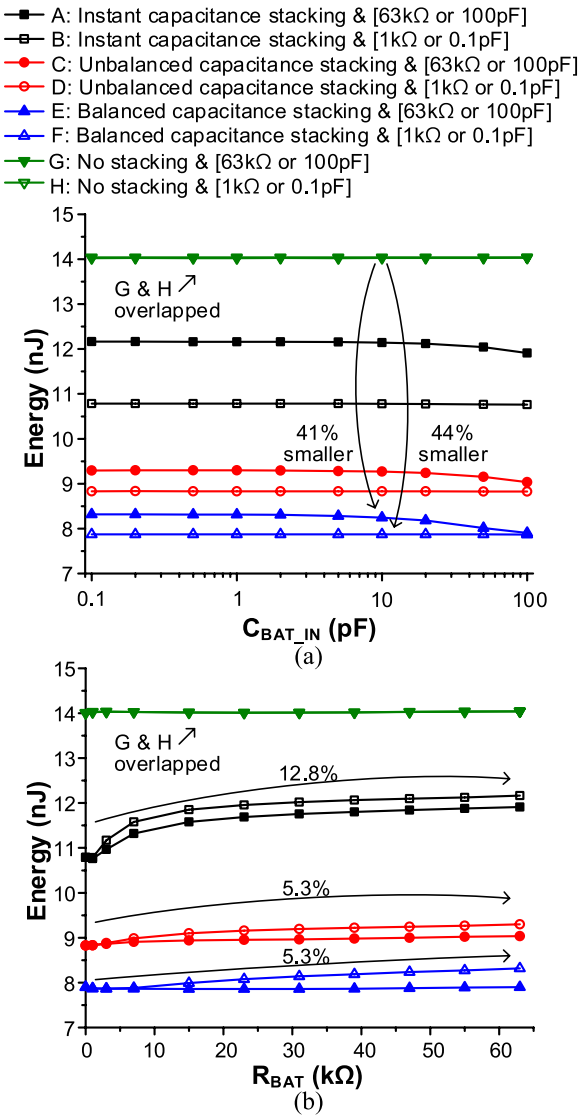


Fig. 16. Simulated energy consumption for *RC* curve generation. (a) $C_{\text{BAT\_IN}}$ dependency. (b) R_{BAT} dependency.

In addition, if C_T is too small due to a large N, the *RC* curve can be disrupted by the capacitance of the switches and the comparator.

Battery management systems have used R_{BAT} to estimate the battery state of health or charge [20]–[26], [33]–[37]. Electrochemical impedance spectroscopy measures battery impedance over a range of frequencies and provides the most complete battery parameters [33], [34] but requires unnecessarily complex hardware only for R_{BAT} measurement.

Instead, R_{BAT} can be calculated from measuring the load current and the voltage difference between the unloaded V_{BAT} and the loaded V_{BAT} [20]. The load current is typically measured using a shunt resistor with low resistance connected to the battery in series [35]–[37]. However, it requires a high-resolution ADC to resolve the small voltage across the shunt resistor.

R_{BAT} can be also measured by connecting the predetermined fixed resistance between the battery and ground and measuring the voltage ratio between the unloaded V_{BAT} and the loaded V_{BAT} [20]. However, the dynamic range of V_{BAT} is limited by the power consumption of the added resistance. Compared with the proposed *RC* time constant method, these techniques dissipate power without any ameliorating charge reuse and also require a division process to compute R_{BAT}.

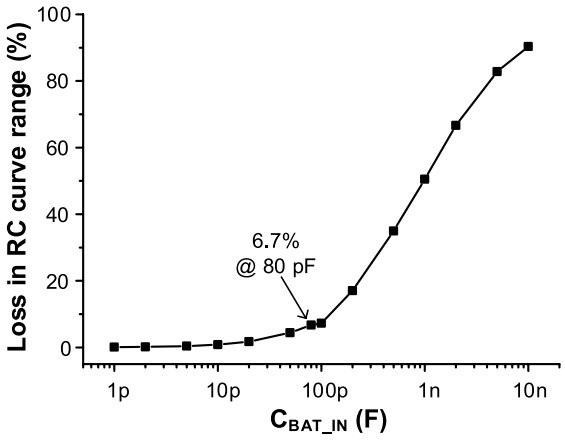


Fig. 17. Simulated loss in the *RC* curve range across $C_{\text{BAT\_IN}}$.

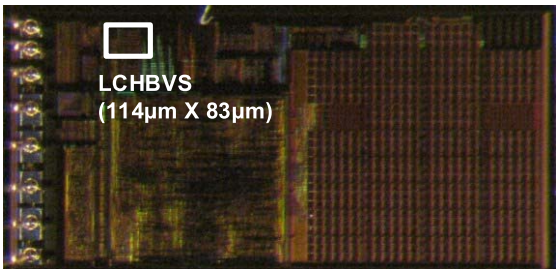


Fig. 18. Die photo of LCHBVS.

AHBVS generates V_{HYST} according to the measured R_{BAT} and the predetermined I_{MAX} taken from design time analysis. Thus, $V_{\text{ON}} = V_{\text{OFF}} + R_{\text{BAT}} \times I_{\text{MAX}}$. AHBVS should turn ON the system when the open-circuit voltage of V_{BAT} equals V_{ON}. Instead, it uses V_{BAT} in reset mode to detect V_{ON} due to the small *IR* drop in reset mode (~0.1 mV). The voltage drop is negligible since the load current in operation mode is at least 100× larger than that in reset mode.

The predetermined I_{MAX} can include a large margin when the maximum value of I_{LOAD} is actually much smaller than I_{MAX}. Also, V_{HYST} can be insufficient when I_{LOAD} is larger than I_{MAX}. If I_{LOAD} is predictable due to periodic operations, I_{LOAD} can be monitored during a few operation cycles and I_{MAX} chosen based on the current consumption profile. However, this runtime approach requires additional power and complexity for battery current monitoring (e.g., a shunt resistor and a high-resolution ADC).

IV. Experimental Results

Fig. 18 shows LCHBVS fabricated in a 180 nm CMOS process. It consumes 635 pW at a 3.6 V supply voltage as measured by a Keithley 6514 Electrometer and averaged over 15 dies.

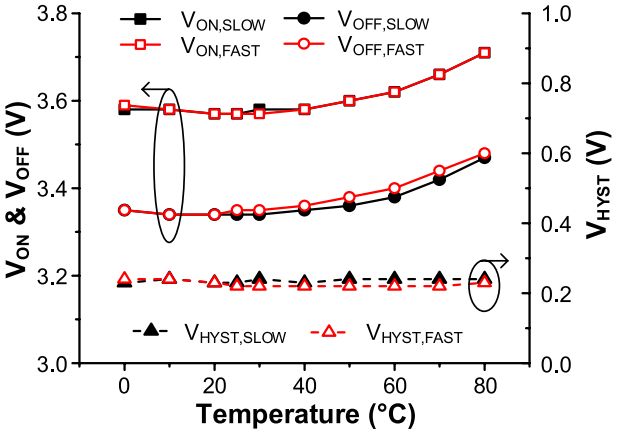


Fig. 19. V_{ON}, V_{OFF}, and V_{HYST} across temperatures with different V_{BAT} transition speeds (0.25 mV/s and 0.8 V/μs).

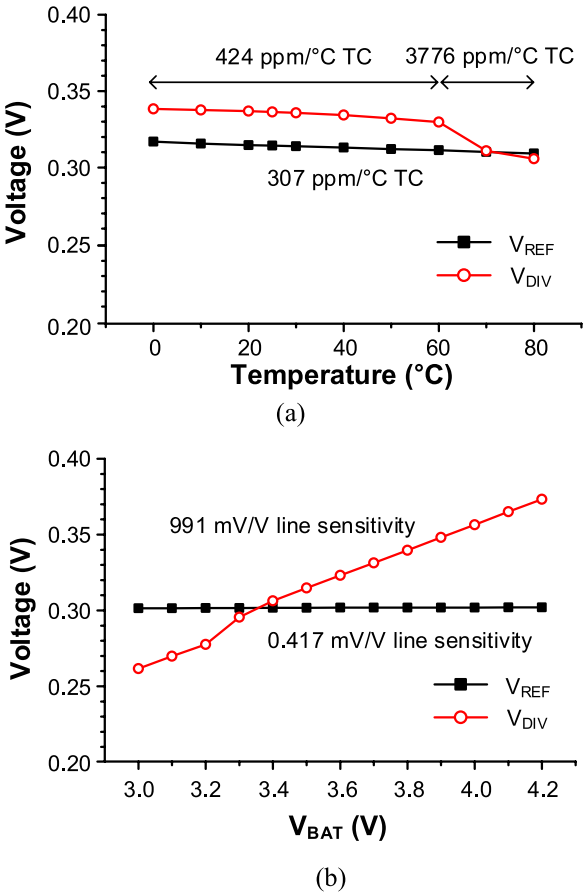


Fig. 20. Measured V_{REF} and V_{DIV}. (a) Temperature dependency. (b) V_{BAT} dependency.

Fig. 19 shows the measured V_{ON}, V_{OFF}, and V_{HYST} across temperatures for two different V_{BAT} transition speeds (0.25 mV/s and 0.8 V/μs). Both V_{ON} and V_{OFF} increase by 3.6% as the temperature increases from 0 °C to 80 °C. However, V_{HYST} is maintained at ~230 mV, which prevents system oscillation due to *IR* drop at V_{BAT}. Fig. 20 shows the measured V_{REF} and V_{DIV} across temperatures and a range of V_{BAT} values. The proposed two-stage voltage reference provides a stable V_{REF} over temperature and V_{BAT} variation (307 ppm/°C temperature coefficient (TC) and 0.42 mV/V line sensitivity).

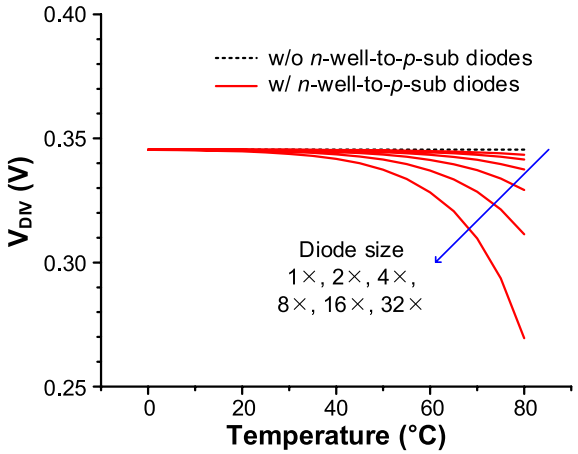


Fig. 21. Simulated effect of leakage current through n-well to *p*-subdiodes on V_{DIV} across temperatures.

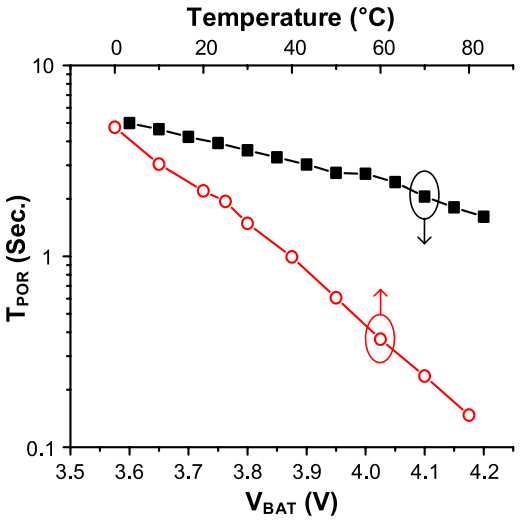


Fig. 22. Measured T_{POR} of LCHBVS across temperatures and V_{BAT}.

V_{DIV} shows a rapid drop as the temperature drops from 70 °C, but it scales well with V_{BAT}. The TC of V_{BAT} is 424 ppm/°C between 0 °C and 60 °C, but it increases to 3776 ppm/°C in the 60 °C–80 °C temperature range due to an increased leakage current between the n-well to the *p*-substrate over the diode stack. Fig. 21 shows the effect of the diode leakage current across temperatures. At higher temperatures, more leakage current pulls down the internal nodes in the diode stack, resulting in a lower V_{DIV}. As shown in Fig. 19, V_{DIV} shifts V_{ON} from 3.58 to 3.71 V and V_{OFF} from 3.35 to 3.47 V. Here, V_{HYST} is maintained although V_{ON} and V_{OFF} are increased. Thus, the higher TC of V_{DIV} at high temperatures does not cause a critical issue. Fig. 22 shows the measured T_{POR} in LCHBVS as a function of the final V_{BAT} and temperature. It is mainly determined by the oscillator period, and the profile of T_{POR} is similar to the inverse of the clock frequency shown in Fig. 23.

Fig. 24 shows a die photo of AHBVS fabricated in a 180 nm CMOS process. It consumes 1 nA standby current with power breakdown as shown in Fig. 25. One-half of the power is consumed in the continuous comparator in order to rapidly respond to the updated V_{ON}.

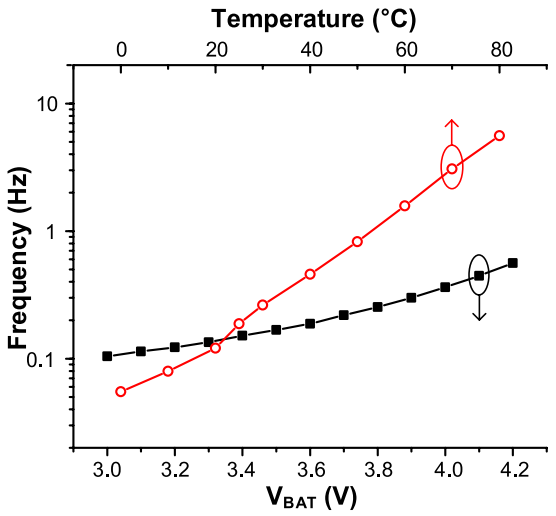


Fig. 23. Measured oscillator frequency across temperatures and V_{BAT}.

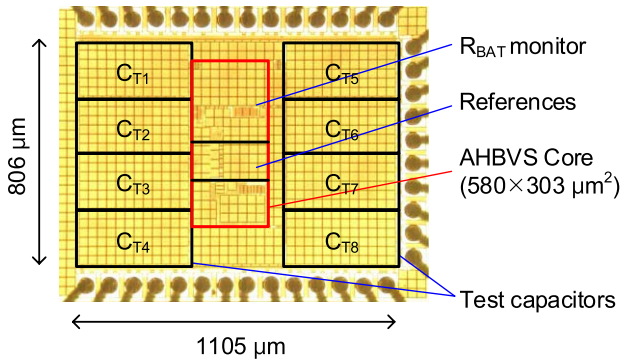


Fig. 24. Die photo of AHBVS.

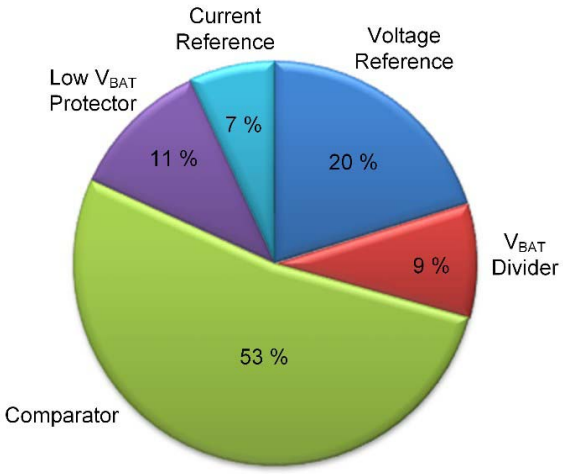


Fig. 25. Power breakdown of AHBVS.

AHBVS is tested with an actual millimeter-size thin-film battery. Fig. 26(a) shows the desirable V_{ON} calculated from the measured R_{BAT} (Keithley 2400 Sourcemeter) and the measured V_{ON} from AHBVS. R_{BAT} increases from 16 to 55 kΩ over 500 charge/discharge cycles. At approximately the

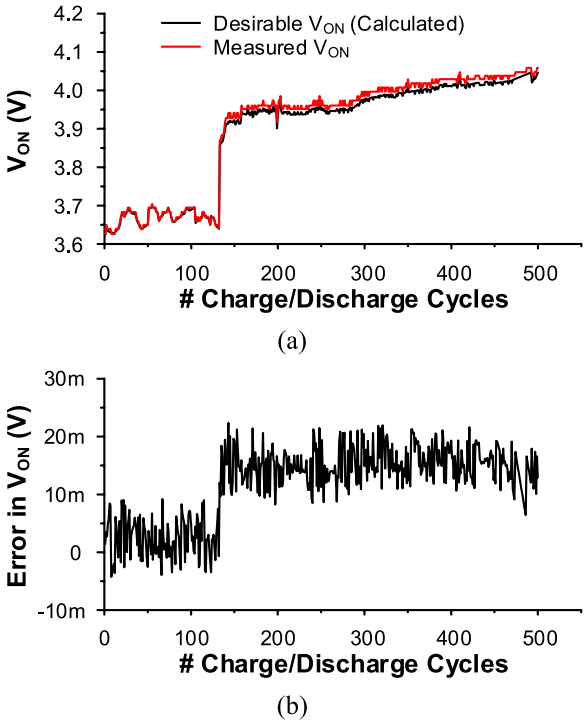


Fig. 26. Measured AHBVS across charge/discharge cycles. (a) Desirable and measured V_{ON}. (b) Error in V_{ON}.

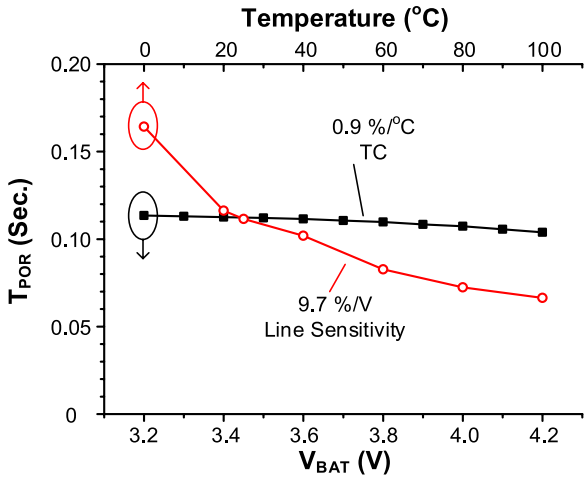


Fig. 27. Measured T_{POR} of AHBVS across temperatures and V_{BAT}.

140th cycle, the monitoring equipment shorts the battery to ground. It degrades the battery performance and changes the R_{BAT} considerably. However, AHBVS correctly updates V_{ON} and covers the increased R_{BAT}. Fig. 26(b) shows the maximum error of 27 mV. The adaptive V_{HYST} enables 2.1× the lower V_{HYST} in the first cycles (416 versus 867 mV), allowing more system functional time and a lower operating V_{BAT}.

Fig. 27 shows the T_{POR} of AHBVS across temperatures and V_{BAT}, revealing 0.9%/°C TC and 9.7%/V line sensitivity. Compared with that observed in LCHBVS, the TC is decreased 24.6-fold (0 °C–80 °C) and line sensitivity is reduced 28.5-fold (3.6–4.2 V) in AHBVS. This improvement is enabled by

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER WORKS

	This Work		[6]	[7]	[8]	[9]	[10]	[31]	[38]
	LCHBVS	AHBVS							
Process (nm)	180	180	N/A	N/A	N/A	N/A	N/A	90	180
Supply Voltage (V)	3.6	3.6	3.0	0.9	1.8	1.2	3.6	1.0	1.8
Power (W)	635p	3.6n	1.5μ	135n	225n	210n	1.8μ	540n	3.6μ
POR Delay (Sec.)	1.94	50m	185m	200m	14.2m	270m	15m	150n	100m
V_{HYST} (mV) (% of Supply)	220 (6.1)	212–1,000 (5.8–27.8)	6.3 (2.1)	11 (1.2)	7.88 (0.4)	31.6 (2.6)	20 (0.6)	432 (43.2)	N/A
Area (mm^2)	0.01	0.89 (0.18)†	N/A	N/A	N/A	N/A	N/A	0.09	0.01

† BVS core only without capacitors for test current generation

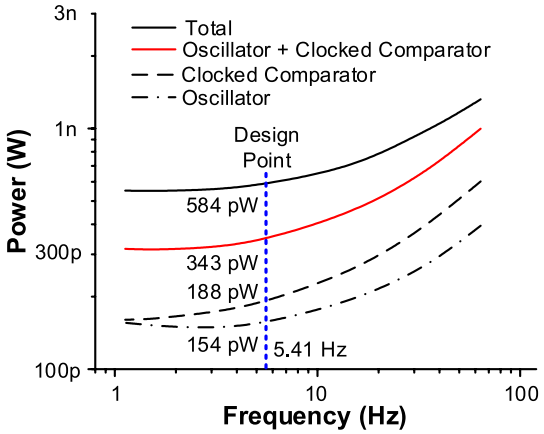


Fig. 28. Simulated LCHBVS power consumption breakdown across operating frequencies.

a stable current generation using a resistor instead of sub-threshold transistors while keeping the standby power low by power gating.

Compared with the other works listed in Table I, LCHBVS and AHBVS demonstrate lower nanoampere current consumption, enabling their use in miniaturized battery-operated and harvesting-capable nodes with aggressive power budgets. The T_{POR} of LCHBVS is 7.2× longer than that of the others; the longer T_{POR} is dictated by the limited power budget, as shown in Fig. 28. This long T_{POR} is acceptable in the target sensing system since they are implanted or permanently deployed in physical spaces and therefore the power-ON event does not occur frequently (e.g., > once per week). For general applications, in AHBVS, a resistor is used to reduce T_{POR} to a similar level as that reported for the other works with higher levels of power consumption. However, a low standby power is maintained with a power gating technique.

AHBVS shows an adaptive V_{HYST}, which can change from 0.21 to 1.0 V and handle up to 63 kΩ R_{BAT} with the same I_{MAX}. The high default V_{HYST} of 0.21 V is designed for conditions where the harvested energy is smaller than the system energy consumption. The other works do not require this default V_{HYST} since they are designed for systems where power comes from power suppliers, and energy harvesting is not considered. Without the default value, V_{HYST} can be reduced to 27 mV based on the experimental results, and the relative V_{HYST} in supply voltage (0.75%) is low compared with that of the other works.

V. CALIBRATION

There can be variation in the capacitance in the R_{BAT} monitor of AHBVS due to process variation. To measure the correct R_{BAT}, oscillator clock frequency [Fig. 11(b)] can be adjusted with a resistor before using a battery. The R_{BAT} monitor can be connected to a power supply with or without the off-chip 63 kΩ resistor (the maximum value) to measure their RC time constant. The clock frequency needs to be high enough to obtain desirable resolution. The measured R_{BAT} with or without the resistor can be used as the maximum and minimum values, respectively.

For online calibration, adaptive and reprogramming methods can be used. AHBVS updates V_{HYST} according to R_{BAT}, which changes over charge/discharge cycles and environmental conditions as mentioned previously. Instead of online R_{BAT} measurement, a BVS in general can be reprogrammed depending on a previous battery study, but errors can occur between the study result and the characteristics of the used battery.

For the T_{POR} change at one temperature due to process variation (e.g., resistance), T_{POR} can be adjusted by shorting/opening the segmented resistors, by connecting/disconnecting the segmented capacitors connected in parallel C_{POR} [Fig. 11(a)], or by changing the current mirroring ratio from I_{POR} to charging current of C_{POR}. For T_{POR} change across temperatures, TC of V_{POR1} and V_{POR2} can be tuned in the similar technique used in [32] to reduce the temperature dependency of T_{POR}.

VI. CONCLUSION

In this paper, battery voltage supervisors (BVSs) are explored as a means of handling a large battery internal

resistance. A discussion of battery voltage, battery internal resistance, required hysteresis, power-on-reset delay for different applications, and the respective impact of each specification on BVS design is included. Two low-power BVSs fabricated in a 180 nm CMOS process are described as examples.

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