Variability Analysis of a Digitally Trimmable Ultra-Low Power Voltage Reference

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***Abstract*— A digitally trimmable voltage reference is proposed, achieving a tight distribution of temperature coefficient and output voltage, along with pA-range current consumption for V_{dd}=0.5-3.0V. Using 2 temperature point digital trimming, the temperature coefficient and nominal output voltage are within 5.3-47.4ppm/°C and 175.2-176.5mV across 25 dies in 0.13µm CMOS. Non-trimmable versions are also implemented in 0.13µm and 0.18µm technologies to study process variations across multiple runs and technology portability of the design.**

I. INTRODUCTION

Recent progress in ultra-low power (ULP) circuit design has been made due to significant interest in environmental and biomedical sensor applications [1,2]. These systems often include analog and mixed-signal modules such as linear regulators, A/D converters, and RF communication blocks for self-contained functionality.

Voltage references (VR) are key building blocks for these modules. In particular, linear regulators require a VR to supply a constant voltage level to the entire system. Also, amplifiers in A/D converters employ several bias voltages. Therefore, it is often necessary to incorporate multiple VR circuits in a system.

VRs are integrated in wireless sensing systems with tight power budgets, which are often less than hundreds of nW due to very limited energy sources. Hence, it is vital that VRs consume very little power. On the other hand, VRs should be able to operate across a wide V_{dd} range, in particular near or below 1V, since some power sources, such as energy scavenging units, provide low output voltages [12].

As a result, there is a growing need for ULP VRs today. We recently proposed a 2-Transistor (2T) VR [4], shown in Figure 1(a), which consumes as little as 2.2pW at V_{dd}=0.5V and 25°C. This VR offers improved power efficiency by ~4 orders of magnitude compared to previous state-of-the-art designs [6-10]. The design uses subthreshold-biased devices with distinct V_{th} levels (one regular and one native device) to achieve a stable output voltage.

Since process variations widen the spread in temperature coefficient (TC) and output voltage we demonstrate a digitally trimmable version of the 2T VR design. To quantify the need for this version we first collect statistical results from the 2T VRs in two different fabrication processes and three different runs. In addition to new data collected from the 0.13µm run in [4], we report new measured data from a separate 0.13µm run with identically designed VRs, as well as a 0.18µm version of the 2T VR. Measurement results indicate that 2T VRs exhibit considerable spread in TC and output voltage due to die-to-die and run-to-run process variations.

Process sensitivity is a common problem for most VRs and is typically addressed through trimming. However, trimming is often a time/cost intensive process, particularly if it involves laser trimming of resistors in the case of bandgap VRs [3,5]. Therefore, we propose a digitally trimmable version of the 2T VR design to improve TC and output voltage accuracy across dies while reducing trimming time and cost. Measurements from the prototype chip in 0.13µm show that trimming enables tighter distributions of TC and nominal output voltage across 25 dies. The TCs lie between 5.3ppm/°C and 47.4ppm/°C while the nominal output varies by ±0.4% from the mean value. The VR consumes 29.5pW at 0.5V and 25°C.

II. CIRCUIT DESIGN

To investigate the impact of run-to-run and die-to-die process variations on TC and output voltage, we fabricate 2T VRs as shown in Figure 1(a) using the same 0.13µm process as in [4]. Figure 2 shows the measurement results of the VRs from the first [4] and second runs. As shown in Figure 2(a), the average output voltage changes by a small amount (0.3%) between the two runs. However, both runs show considerable spread in TC and output voltage from die-to-die variations, as shown in Figure 2.

To minimize the TC and output voltage spread, we design a VR with digital trimming, as seen in Figure 1(b). The ratio of top-to-bottom device widths is critical to TC and output voltage [4]. However, the optimal width ratio at design time may not be ideal for each chip due to process variations. Therefore, it is beneficial to be able to change the width ratio post-silicon. This VR design can selectively turn on and off the four top and four bottom devices using associated switches. Bottom devices are sized as powers of 2 for range and granularity, while top devices are sized up gradually from the minimum width of native devices (3µm). By applying control signals *bmod* and *tmod* to the switches, the top-to-bottom width ratio varies from 0.52 to 3.75 with 256 different settings. Control signals swing from 0 to V_{dd}, requiring no extra supply voltage. One-Time-Programmable memories such

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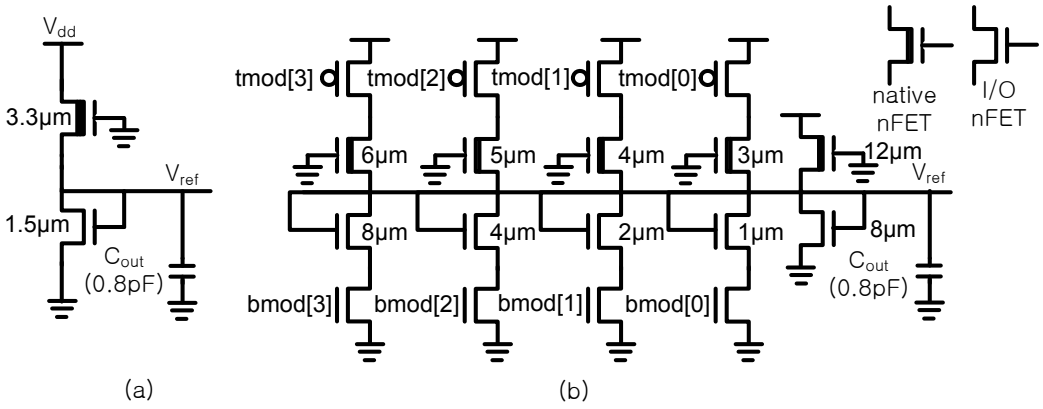

Figure.1. (a) 2T voltage reference (b) trimmable voltage reference.

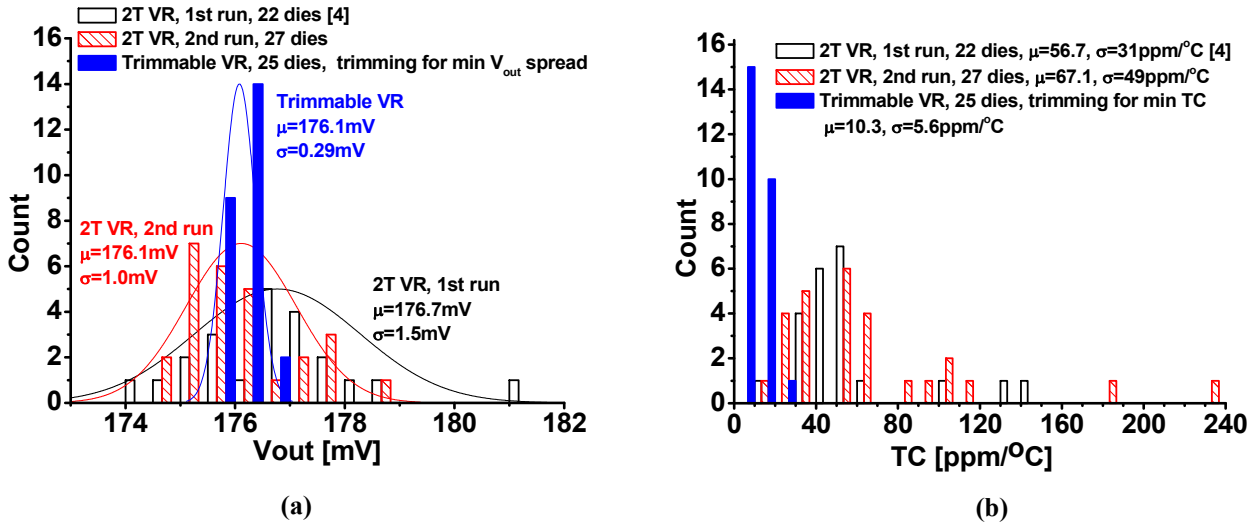

Figure 2. Measured (a) output voltage and (b) TC distribution.

as fuses can be used to provide the signals with minimal power overhead [11]. Once the switches are turned off, any top and bottom devices connected to them have negligible effect on the output voltage, acting as a dangling capacitor. Finally, a 0.8pF output capacitor is added to suppress the effect of noise on output voltage.

III. MEASUREMENT RESULTS

The trimmable VR can be used to achieve consistently small TC and/or very tight output voltage ranges. In Figure 2(a) the 3σ output voltage spread is reduced by ~3.5× from the untrimmed version while Figure 2(b) shows a reduction in worst-case TC of nearly 8×.

More likely the design goal will be to meet a specified TC constraint with minimum deviation from the desired output voltage. Figure 3 illustrates the TC and output voltage design spaces for different settings in the trimmable VR. Figure 3(a) shows that for a given total width of top devices, for example 22µm, setting the bottom device total width to 10µm minimizes TC. A clear trend is observed where a specific width ratio leads to minimum TC, forming a diagonal line in the matrix. Likewise, output voltage changes at different settings, and depends directly on the width ratio. This is again confirmed by the diagonal line in Figure 3(b).

We develop a trimming procedure for the proposed VR that balances minimal trimming time with optimal performance. To reduce testing time, we limit the number of trim settings and temperatures during the trimming process. At two temperature points (-20 and 80°C), output voltages are measured by sweeping across 16 settings using two top device and eight bottom device widths. Then, an optimal setting for each die is chosen for given design objective. Our objective is to minimize output voltage spread subject to TC being less than 50ppm/°C. After choosing the appropriate setting, we test each VR at a finer temperature granularity and observe that the TC constraint remains met, as shown in Figure 4.

Figure 4 shows that trimming reduces the spread of TC and output voltage by 9.6× and 9.8× compared to pre-trim

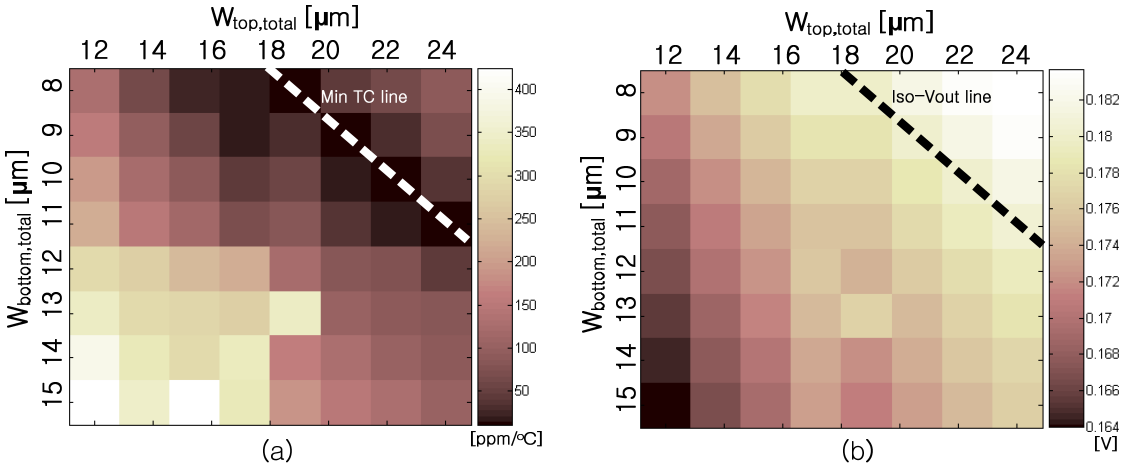

Figure 3. Measured (a) TC and (b) V_{out} change with trim settings.

results for the 25 dies. Only eight different settings are used out of the 256 possible.

PSRR, LS, and power consumption are also measured for the trimmable VRs. Figure 5 shows that PSRR is measured as -51 to -64dB, which tracks simulation results. Typical power consumption is 29.5pW at 0.5V, 25°C and 2.5nW at 3V, 80°C.

Output referred noise is investigated with SPICE simulations, as shown in Figure 6. Together with output capacitors, the trimmable VR effectively suppresses noise, showing 20nV/Hz$^{1/2}$ with 1nF output capacitor at 100Hz. As a reference point, [8] exhibits 152nV/Hz$^{1/2}$ with 100nF output capacitor at the same frequency.

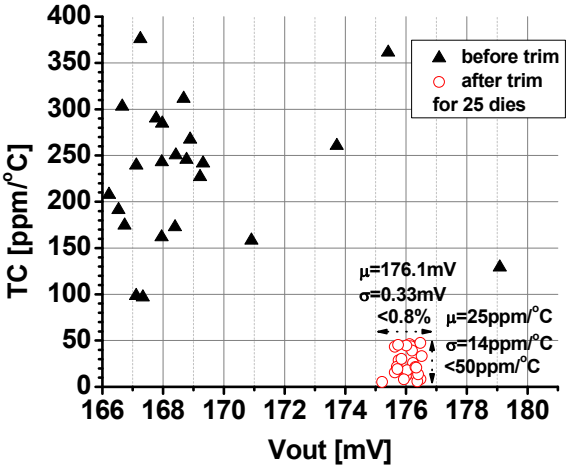

Figure. 4. Measured reductions of V_{out} and TC spreads after trimming.

To demonstrate the portability of the VR design we also implement 2T VRs (Figure 1(a)) in a 0.18µm CMOS technology. Given the simple topology, porting the design only involves sizing of the two transistors. Measurements from all 14 dies show comparable results to the 0.13µm process. Area increases only slightly despite the older technology since very long (60µm) devices are employed in the 0.13µm version for low power.

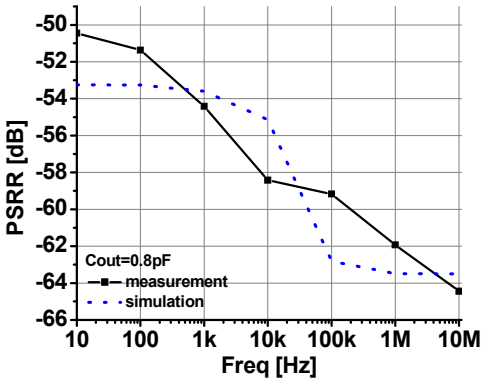

Figure. 5. Measured PSRR in trimmable VR.

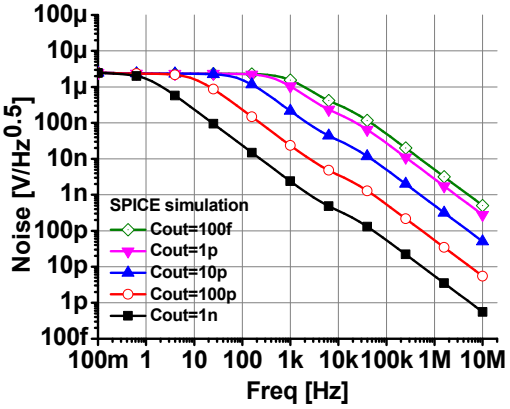

Figure. 6. Output referred noise of trimmable VR (simulation).

Relevant measurement results are summarized in Table I and compared to recent low voltage and low power VRs [7-9]. For designs without multi-die results, we use typical values. Die photos of the trimmable and 2T VRs in 0.13µm and 2T VR in 0.18µm CMOS are provided in Figure 7.

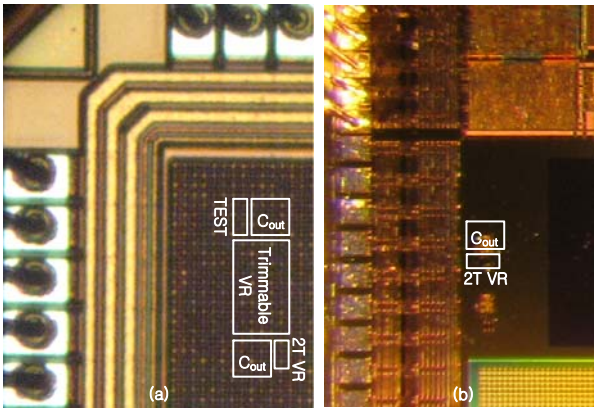

Figure. 7. Die photo in (a) 0.13µm and (b) 0.18µm CMOS

IV. CONCLUSIONS

This paper first investigates the effect of process variations, both run-to-run and die-to-die, on an ultra low power voltage reference using two process technologies and 3 different runs. We then propose a digitally trimmable VR to suppress observed spread of TC and output voltage. Using two-point temperature trimming with 8 trimming combinations, the spreads of TC and V_{out} are measured as 5.3-47.4ppm/^{o}C and 175.2-176.5mV for 25 dies. The VR, designed in 0.13µm CMOS consumes only 29.5pW at V_{dd}=0.5V and 25^{o}C. The 2T VR is also designed in 0.18µm CMOS, demonstrating the portability of the design and good performance across processes.

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Table I. Comparisons of Voltage Reference Circuits

	Trimmable VR	**2T VR**	**2T VR**	**[7]**	**[8]**	**[9]**
Process	0.13µm CMOS	0.18µm CMOS	0.13µm CMOS	0.35µm CMOS	0.6µm CMOS	0.35µm CMOS
V_{dd}	0.5-3.0V	0.5-3.6V	0.5-3.0V	0.9-4.0V	1.4-3.0V	1.0-4.0V
V_{out} (min) **V_{out} (max)**	175.2mV 176.5mV	326.8mV 330.0mV	174.9mV 178.7mV	670mV	290.05mV 328.57mV	190.1mV
TC (min) **TC (max)**	5.3ppm/^{o}C 47.4ppm/^{o}C	54.1ppm/^{o}C 176.4ppm/^{o}C	16.87ppm/^{o}C 231ppm/^{o}C	10ppm/^{o}C	2.7ppm/^{o}C 62.0ppm/^{o}C	16.9ppm/^{o}C
LS (min) **LS (max)**	0.036%/V	0.044%/V	0.033%/V	0.27%/V	0.012%/V 0.225%/V	0.76%/V
PSRR	-51/-64dB (100Hz/10MHz)	-49/-55dB (100Hz/10MHz)	-53/-62dB (100Hz/10MHz)	-47/-41dB (100/10MHz)	-47/-20dB (100Hz/10MHz)	-41/-17dB (100Hz/10MHz)
Power **(V_{dd}, temp)**	59pA (0.5V,25^{o}C) 847pA(3V,80^{o}C)	11pA (0.5V,25^{o}C) 139pA(3V,80^{o}C)	4.4pA (0.5V,25^{o}C) 81pA(3V,80^{o}C)	40nA (0.9V,RT) 70nA(4V, 80^{o}C)	9.7µA(3V,100^{o}C)	0.25µA(1V,RT) 0.56µA(4V,RT)
Size	9300µm^2	1425µm^2	1350µm^2	45000µm^2	55000µm^2	49000µm^2
Comment	Post trimming 1 run, 25 dies	1 run, 14 dies	2 runs, 49 dies	Only one part measured	C_{out}=0 for PSRR 3 runs, 45 dies	Only one part measured