# A 20-pW Discontinuous Switched-Capacitor Energy Harvester for Smart Sensor Applications

Xiao Wu, Yao Shi, Supreet Jeloka, *Student Member, IEEE*, Kaiyuan Yang, Inhee Lee, Yoonmyung Lee, Dennis Sylvester, *Fellow, IEEE*, and David Blaauw, *Fellow, IEEE* 

Abstract-We present a discontinuous harvesting approach for switch capacitor dc-dc converters that enables ultralowpower energy harvesting. Smart sensor applications rely on ultralow-power energy harvesters to scavenge energy across a wide range of ambient power levels and charge the battery. Based on the key observation that energy source efficiency is higher than charge pump efficiency, we present a discontinuous harvesting technique that decouples the two efficiencies for a better tradeoff. By slowly accumulating charge on an input capacitor and then transferring it to a battery in burst mode, dc-dc converter switching and leakage losses can be optimally traded off with the loss incurred by nonideal maximum power point tracking operation. Harvester duty cycle is automatically modulated instead of charge pump operating frequency to match with the energy source input power level. The harvester uses a hybrid structure called a moving-sum charge pump for low startup energy upon a mode switch, an automatic conversion ratio modulator based on conduction loss optimization for fast conversion ratio increment, and a <15-pW asynchronous mode controller for ultralow-power operation. In 180-nm CMOS, the harvester achieves >40% end-to-end efficiency from 113 pW to 1.5  $\mu$ W with 20-pW minimum harvestable input power.

*Index Terms*—DC–DC converter, discontinuous, energy harvesting, switched capacitor, ultralow power.

#### I. INTRODUCTION

**E** NERGY harvesting from the ambient environment is critical to self-sustaining IoT devices, such as miniature-scale sensor nodes [1] and implantable medical systems [2], [15]–[17]. Energy sources including photovoltaic [1], [11], thermal [18], piezoelectric [19], [20], and RF energy [16], [17] are available for harvesters to scavenge to charge the batteries.

However, there are three main challenges in energy harvesting for IoT devices. First, power level varies dramatically with ambient conditions. Illuminance can range from 10 lx at twilight to 100K lx under direct sunlight. Under the illuminance range of 10–100K lx, a 2.6 mm  $\times$ 3 mm solar cell can produce 20 nW–200  $\mu$ W [3], marking a 10000 times range, which is difficult for harvesters to efficiently scale

X. Wu, Y. Shi, S. Jeloka, K. Yang, I. Lee, D. Sylvester, and D. Blaauw are with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109-2122, USA (e-mail: lydiaxia@ umich.edu; yaoshi@umich.edu; sjeloka@umich.edu; kaiyuan@umich.edu; inhee@umich.edu; dmcs@umich.edu; blaauw@umich.edu).

Y. Lee is with Sungkyunkwan University, Suwon 440-746, South Korea (e-mail: yoonmyung@skku.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2016.2645741

[4] [5] [6] [7] 100m 100% МРРТ 10m 90% Efficiency 1m 80% Efficiency 100µ 70% Harvestable Input Range(W) 10µ 60% 50% 1μ 100n 40% DC-DC 30% 10n Converte 20% 1n Efficiency 10% 100p 10 [10] [11] [12] [4] [5] [6] [9] [7]

Fig. 1. Recent advances in low-power harvesting.

across. Second, it is advantageous for harvesters to harvest from low ambient power level. Admittedly, there are applications where sufficient high input ambient power is available to harvesters and sufficient battery size to survive through periods of low ambient input power. However, there are also situations where the sensor nodes are supplied with limited maximum input power for long periods of time or with very limited battery size or no battery at all. For some applications such as infrastructure monitoring, nodes may be placed in hidden or difficult-to-reach locations, often dark and possibly cold and quiet, providing extremely low ambient energy available for harvesting (e.g., 150 pW for a 0.01 mm<sup>2</sup> photovoltaic cell at 32 lx). Biological sensing, as another example, may require that the sensor nodes to be placed on moving animals possibly restricting the level of maximum ambient energy available from picowatts to nanowatts (from nanogenerators [23]-[25], from biofuel cell [26]). Therefore, harvesters, which remain efficient with low ambient input energy, may open up possibilities for wider choice of sensor node placements and energy scavenge sources. However, few harvesters have been presented to date that can maintain reasonable efficiency with subnanowatt input power. For convenience, we refer to the minimum harvestable power as the harvesting floor. As shown in Fig. 1, the harvesting floor has decreased in recent publications, with some papers pushing the limit to 1 nW at 30%-50% efficiency. An inductor-based harvester was proposed in [6], which extends the harvesting floor to 1.2 nW by reducing the leakage power of the harvester to 544 pW, setting the harvesting floor to be near 500 pW. As an alternative approach, a self-oscillating switched capacitor dc-dc converter was proposed [7] that extends harvesting floor by reducing clock generation overhead. Both these works sought to reduce the "ON-power" of the harvesters, and thus pushed the harvesting floor down to near 500 pW. This paper is the first to the best of our knowledge that can harvest below 500 pW; it does so while maintaining at least 40%

0018-9200 © 2017 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications\_standards/publications/rights/index.html for more information.

Manuscript received August 12, 2016; revised October 6, 2016 and December 13, 2016; accepted December 14, 2016. Date of publication January 23, 2017; date of current version March 23, 2017. This paper was approved by Guest Editor Brian Ginsburg.

#### **Conventional Continuous Harvester**



Fig. 3. Conceptual efficiency illustration of (a) traditional harvester efficiency and (b) proposed harvester.

efficiency across an input power range of 13000 times. The third challenge for a harvester is that each energy source needs to be biased properly to produce maximum power; this process is called maximum power point tracking (MPPT). As shown in Fig. 1, harvesters typically achieve  $\geq$ 90% energy source efficiency when incorporating MPPT. In summary, we face three challenges: wide input power range, low ambient power, and MPPT.

To extract energy efficiently from an energy source, a proper bias condition is required to match the ambient power levels (e.g., V<sub>mppt</sub> depends on incident light level for photovoltaics). Fundamentally, the ability to bias the energy source correctly for maximum power extraction is not limited by power levels, as long as the proper voltage or impedance is seen by the energy source. However, the efficiency of dc-dc converters is closely related to input power levels, and a dc-dc converter is usually only efficient for a certain power range [13], and limited by leakage for low input power. Hence, we observe that energy sources can offer much higher efficiency than dc-dc converters for low ambient power levels and across wide power ranges. Therefore, to extend the harvesting floor by increasing efficiency at low ambient power levels, this paper proposed a new method called a discontinuous harvester, in which we intentionally trade off MPPT efficiency for dc-dc converter efficiency.

Conventionally, a harvester is a dc–dc converter, with one common topology being a switch-capacitor (SC)-based charge pump as shown in Fig. 2. This charge pump is continuously pumping charge from the energy source, which produces a low voltage, in order to charge the battery at a high voltage. The dc–dc converter efficiency remains relatively flat for a certain range of input power as shown in Fig. 3(a). As input power increases, the charge pump will increase its frequency to match the power level. Eventually a point where efficiency flattens is reached where the efficiency is limited by the drive strength of the power switches. On the other hand, as input power decreases, the charge pump runs slower and becomes



Fig. 4. Concept of discontinuous harvester.



Fig. 5. Conceptual operation of discontinuous harvester.

leakage dominated, leading to poor harvesting efficiency at low ambient power. Typically, reducing switch sizes can limit leakage. However, this approach concurrently reduces the maximum input power the system can harvest, resulting in a similar harvesting range. Therefore, size optimization cannot effectively extend the range of harvestable input power. In contrast, while charge pump power range is inherently limited, it is relatively easy to maintain MPPT efficiency across a wide range of input power. Put another way, overall efficiency is given by MPPT efficiency multiplied by charge pump efficiency, and overall efficiency is limited by charge pump efficiency.

To extend the harvesting floor, the idea of this paper (extended from [21]) is to trade off MPPT efficiency to allow for higher charge pump efficiency at low input power levels. At the same time, efficiency is maintained at high input power, so that an ultrawide range harvester with low harvesting floor is achieved [Fig. 3(b)].



Fig. 6. Dependence of efficiencies on  $\Delta V$ sol based on model prediction and simulation.



Fig. 7. Dependence of simulated end-to-end efficiency on VH.



Fig. 8. Dependence of  $\Delta V$ sol, opt on Cbuf based on calculation.

II. PROPOSED TECHNIQUE: DISCONTINUOUS HARVESTING

#### A. Discontinuous Harvesting

This paper is a discontinuous harvester that operates in two phases (Fig. 4). In these two phases, the bias voltage of the energy source, V sol, deviates from V mppt, which results in



Fig. 9. Proposed architecture.

a slightly lower harvesting source efficiency. At the same time, the charge pump is duty cycled to achieve a much higher CP efficiency. This paper uses an off-chip capacitor controlled by on-chip switches S2 and S3 to isolate the charge pump. A mode controller enables the two-phase discontinuous operation.

It should be noted that this discontinuous burst-mode operation is only applicable when the ambient power accessible to the harvester is at the low end of its operating range. In this situation, the harvester efficiency is limited by leakage, and the discontinuous operation can effectively reduce the efficiency degradation due to leakage. When the ambient power accessible to the harvester is high enough for the harvester to operate efficiently and leakage is not dominant, the harvester is configured to operate continuously as a conventional charge pump, which matches its frequency to the given input power. In both the scenarios, we aim to extract maximum power from the input energy source.

Phase 1 is a harvest phase where S2 and S3 are open. In this phase, the energy source slowly accumulates charge on the capacitor. As shown in Fig. 5, bias voltage Vsol increases from below Vmppt to above Vmppt. In contrast, a conventional harvester attempts to hold the energy source output at a fixed voltage Vmppt. Hence, as shown in the second plot, the proposed method sacrifices MPPT efficiency. In this phase, the charge pump is power gated reducing system leakage to below 15 pW—this value is critical as it sets the harvesting floor. In contrast, conventional continuous harvesters have a consistently high leakage, resulting in a low or even negative charge pump efficiency at extremely low input power levels (e.g., subnanowatts).

When Vsol is sufficiently high, the harvester enters phase 2, which is a transfer phase. In this phase, S2 and S3 are closed to power on the charge pump, effectively transferring charge to the battery in a burst-mode. The charge pump goes through a startup mode and operates at its peak efficiency in steady state. Vsol quickly decreases in this phase, and at some point the harvester is reconfigured back to the harvest phase. It should be noted that when operating discontinuously (i.e., available input



Fig. 10. Detailed architecture of discontinuous harvester.



Fig. 11. Timing diagram of the discontinuous harvester.

power is low), the charge pump always operates at its optimal frequency with peak efficiency, and when input power level is high enough for efficient continuous operation, the charge pump needs to adjust operating frequency for maximum power extraction. Therefore, this technique simplifies the charge pump design because optimizations (flying capacitor size, switch size, and so on) are only needed for high input power range. In this implementation, capacitor and switch sizes are optimized for input power >100 nW for the given die area.

The resulting solar efficiency of the proposed harvester is lower, because Vsol deviates from V mppt, however, a much higher charge pump efficiency is achieved due to the low leakage in harvest phase and peak efficiency in transfer phase. Therefore, the discontinuous harvester has much higher overall efficiency under low input power.

#### B. Energy Efficiency Tradeoff Analysis

The discontinuous harvester enters transfer phase when the capacitor Cbuf is charged and returns to harvest phase when Cbuf is depleted, resulting in a voltage range seen at Cbuf. We refer to the voltage range of this capacitor as  $\Delta$ Vsol. It is important to note that there is a tradeoff between MPPT and dc–dc converter efficiencies that serves to limit  $\Delta$ Vsol.

 $\Delta$ Vsol is an indicator of how often the system goes into transfer phase. Fig. 6 shows the tradeoff related to  $\Delta$ Vsol based on a mathematical derivation given later in this section.

Fig. 12. Proposed reference voltages generation.

Voltage

Vref generation

0.40-100% approximated 0.38 efficiency optimal Vref H=0.86Voc 0.36 80% efficiency optimal Vref H voltages (V) 0.34 Vref\_L=0.77Voc 0.32 50% 50% Efficiency 40% optimal Vref\_L 0.30 Reference 0.28 0.26 0.24 20% 0.22 0.20 10pW 100pW 1nW 1pW Pmppt

Mode Controller

(MC)

OSC

/ref H ≈ 0.86Voc

Vref L≈0.77Voo

Asynchronous Logic

HV

Vsol

TR

Fig. 13. Simulated end-to-end efficiency with approximated Vref\_H and Vref\_L.

As  $\Delta$ Vsol decreases, Vsol becomes closer to V mppt and solar efficiency accordingly rises. As  $\Delta$ Vsol decreases toward zero, the harvester becomes a conventional harvester operating continuously, biasing the solar cell at a fixed voltage where MPPT can be achieved for the given light condition, battery voltage and the implemented charge pump. However, in this latter



Fig. 14. Structure of moving-sum charge pump.

case the harvester enters transfer phase more often, introducing extra losses. One cost associated with entering transfer phase very frequently includes a startup process in which the CP initializes the flying caps, requiring a large amount of energy. With infrequent entry to transfer phase (i.e., larger  $\Delta$ Vsol) the startup loss gradually becomes negligible, and total charge pump efficiency approaches its peak. In summary a large  $\Delta$ Vsol limits solar efficiency while a small  $\Delta$ Vsol is limited by charge pump efficiency. Therefore, there is an optimal  $\Delta$ Vsol that achieves the highest overall efficiency.

To derive the optimal  $\Delta V$ sol, we define two voltages VH and VL, which indicate the high and low voltages seen at Cbuf when the harvester enters transfer phase and harvest phase, respectively. Thus,  $\Delta V$ sol = VH–VL by definition. The optimal pair of VH and VL results in the maximum end to end efficiency. End-to-end efficiency Eff<sub>tot</sub> can be expressed as (1), where Eff<sub>solar</sub> is the solar efficiency in the harvest phase, Eff<sub>tran</sub> is the overall charge pump efficiency in the transfer phase,  $P_{\text{leak}}$  is the leakage power in the harvest phase, and  $P_{\text{mppt}}$  is the solar cell output power when biased at its maximum power point (see Appendix A for details). Equivalent series resistance (ESR) of the capacitor Cbuf (ESR = 0.3  $\Omega$ , measured) can potentially limit the maximum current (e.g., Imax = 30 mA for 10-mV voltage drop) supplied by Cbuf, and thus sets an upper bound on input power

in transfer phase for discontinuous operation. However, the charge pump implemented in this design operates at a much lower power level and, therefore, is not limited by ESR

$$Eff_{tot} = Eff_{solar} * Eff_{tran} - \frac{P_{leak}}{P_{mppt}}.$$
 (1)

Overall charge pump efficiency in the transfer phase is given in (2), where  $Eout_{st}$  and  $Ein_{st}$  are the energy drawn from the battery and Cbuf, respectively, during the startup step, and  $Eout_{ss}$  and  $Ein_{ss}$  are the steady-state output and input energy, respectively

$$Eff_{tran} = \frac{Eout_{ss} - Eout_{st}}{Ein_{ss} + Ein_{st}}.$$
 (2)

The transfer phase efficiency can be expressed in terms of VH and VL and charge pump efficiency in steady state,  $Eff_{ss}$  (3). For simplicity,  $Eff_{ss}$  is assumed to be independent of VH and VL for this derivation, since  $\Delta V$ sol is only a few hundreds of millivolts and charge pump efficiency is relatively insensitive to VH and VL compared with solar cell efficiency.  $Eout_{st}$  and  $Ein_{st}$  depend mostly on VH, and vary depending on the charge pump structure used. For simplicity,  $Eout_{st}$  and  $Ein_{st}$  are assumed to be independent of VH and VL

$$Eff_{tran} = \frac{\left[\frac{1}{2}*Cbuf*(VH^2 - VL^2) - Ein_{st}\right]*Eff_{ss} - Eout_{st}}{\frac{1}{2}*Cbuf*(VH^2 - VL^2)}.$$
(3)

When the harvester goes into harvest phase, solar cell outputs power to slowly charge Cbuf. Due to the voltage ripple  $\Delta$ Vsol = VH–VL, solar cell is not biased at its maximum power point, introducing a reduced solar efficiency. Therefore, solar efficiency can be expressed as in (4), where VL and VH are the voltage across Cbuf at the beginning and at the end of the harvest phase, respectively, and P(v) is the instantaneous output power of the solar cell when biased at voltage v (see Appendix B for details)

$$\mathrm{Eff}_{\mathrm{solar}} = \frac{\int_{VL}^{VH} 2v dv}{P_{\mathrm{mppt}} \int_{VL}^{VH} \frac{2v}{P(v)} dv}.$$
 (4)

Here, we set  $VH = V_{mppt}$ , which is the maximum power point of the solar cell. After simplification (see Appendix C for details), solar efficiency can be simplified as shown in (5) at the bottom of this page, where *Isc* is the short circuit current of the solar cell. Transfer phase efficiency can be rewritten in (6), as shown at the bottom of this page, in terms of  $\Delta$ Vsol.

The optimal  $\Delta V$ sol can be found by taking first order derivatives of (1) assuming  $P_{\text{leak}}$  is independent of  $\Delta V$ sol. Equation (7) shows that  $\Delta V$ sol, opt increases with startup

$$Eff_{solar} = \frac{(2V_{mppt} - \Delta Vsol) * Isc}{2P_{mppt}}$$

$$Eff_{tran} = \frac{\left[\frac{1}{2} * Cbuf * \left(V_{mppt}^{2} - (V_{mppt} - \Delta Vsol)^{2}\right) - Ein_{st}\right] * Eff_{ss} - Eout_{st}}{\frac{1}{2} * Cbuf * \left(V_{mppt}^{2} - (V_{mppt} - \Delta Vsol)^{2}\right)}$$
(6)



Fig. 15. Three-phase operation of moving-sum charge pump.

energy and decreases with Cbuf size. Fig. 8 shows the relationship between  $\Delta$ Vsol, opt, and Cbuf; intuitively as Cbuf grows the harvester should be able enter the transfer phase more often (startup costs are well amortized) and this improves total efficiency since the energy source operates closer to its MPP. One tradeoff here is in area and cost at the discrete component level

$$\Delta \text{Vsol, opt} = \frac{\sqrt{2}\sqrt{\text{Eff}_{\text{ss}} * Ein_{\text{st}} + Eout_{\text{st}}}}{\sqrt{\text{Cbuf} * Eff_{\text{ss}}}}.$$
 (7)

## III. IMPLEMENTATION OF DISCONTINUOUS HARVESTER *A. Proposed Architecture*

The proposed harvester (Fig. 9) consists of an alwayson power domain, shown in dashed lines, a gated power domain, an off-chip capacitor, and switches S1 through S3 used to enable the two phases. In harvest phase, the mode controller power gates the other circuits, while the solar cell charges the capacitor as discussed before. The low power mode controller consists of a clocked comparator that monitors Vsol and triggers a transition to transfer phase if Vsol increases



Fig. 16. Simulated startup energy comparison between moving-sum charge pump and Dickson charge pump.

above Vref\_H. The comparator is clocked by a leakage-based oscillator [22]. Mode transition is controlled using asynchronous logic to eliminate clock power that would otherwise be dominant.



Fig. 17. Structure of binary charge pump.

As shown in Figs. 10 and 11, when the harvester enters the transfer phase, S1–S3 are enabled and the system is powered ON. First, the charge pump needs to be powered up. The system controller is powered by battery voltage VBAT, which is the only voltage available. It configures the charge pump to an initial conversion ratio, and begins counting cycles as the charge pump builds up its internal voltages. The system controller runs at the same frequency as the charge pump to accurately control the duration of startup mode. As the charge pump stabilizes, it begins to produce a 1.2-V (labeled V1P2) supply. The system controller then immediately switches its power supply from VBAT to V1P2 to reduce power consumption. The 1.2-V supply is used for the remainder of the charge transfer phase.

At this point the system controller switches to a slower clock to reduce dynamic power; a divided down version of the charge pump clock is generated and selected by the Clock CTRL module. Once the charge pump is stabilized it only requires occasional conversion ratio reconfiguration. As Vsol decreases during the transfer phase, the harvester automatically increases the conversion ratio. An automatic conversion ratio modulator (ACRM) monitors Vsol and determines whether conversion ratio should be changed or not, and increments the conversion ratio accordingly. Comparator C2 is a clocked

comparator that controls the transition back to harvest phase. It fires when Vsol becomes lower than Vref\_L, and returns the harvester to harvest phase. In this implementation, Vref H and Vref\_L are external references, which vary with incident light conditions, and the light conditions here are sensed externally. A more complete system for future work should include the generation of the references, a light sensing module and a mapping module to map the lighting condition to the optimal reference voltages, which can be predetermined. The implementation of these modules may introduce extra power overhead. One possible method to generate the reference voltages is shown in Fig. 12. Vref\_H and Vref\_L can be approximated as fractions of the open circuit voltage (Voc) of a solar cell, which can be generated using a dummy solar cell unit connected in parallel with a voltage divider. This provides a low power (simulated power consumption: 14 fW typical, <100 fW across corners) way of generating reference voltages that automatically tracks the lighting condition. Fig. 13 compares the simulated optimal end-to-end efficiency with the efficiency when using the proposed circuit to generate Vref\_H and Vref\_L as fractions of Voc. Optimal reference voltages are approximated with <10-mV error, and the resulting efficiency degradation is within 2%.

#### B. Moving-Sum Charge Pump

The dc-dc converter used in the harvester upconverts Vsol to the battery voltage in order to charge the battery, and it is only enabled during transfer phase. To accommodate solar voltage from 0.25 to 0.45 V, we need 10-31 times variable conversion ratio. A standard approach would use a Dickson charge pump, which has high efficiency and offers fine-grained conversion ratios. However, Dickson charge pumps have drawbacks that are unique to the proposed discontinuous harvesting system. Dickson charge pumps have a large number of flying capacitors, and high voltage across each of them. For example, to obtain a 31 times conversion ratio, thirty flying capacitors are needed. Voltage across the capacitors range from  $1 \times VIN$ to 30  $\times$  VIN. This will result in large startup losses when initializing the flying caps. This is not a concern in alwayson continuous harvesters, however, these losses will greatly degrade efficiency in the proposed discontinuous harvester, as the harvester frequently starts and shuts down the charge pump.

In order to reduce the number of flying caps while maintaining all needed conversion ratios, we proposed a new structure named "moving-sum charge pump," which is shown in Fig. 14. It consists of a reduced Dickson charge pump to produce two to nine times VIN, a voltage mux to select four voltages from two to nine times according to the conversion ratio, and a summing series parallel stage where the selected voltages on the flying caps are placed in series and summed to charge VOUT.

The operation has three phases as shown in Fig. 15. In phases A and B, the reduced Dickson CP stage operates identically to a standard Dickson charge pump. Four different intermediate voltages are tapped out as Vs1–Vs4. Four flying caps in the summing stage are connected to the Dickson stage separately and charged to Vs1–Vs4. Charge is transferred from



Fig. 18. Two-phase operation of binary charge pump.



Fig. 19. Charge pump efficiency comparison based on simulation.

Fig. 20. ACRM.

Dickson stage to summing stage. In phase C, the four flying caps in the summing stage are disconnected from Dickson stage, and then stacked together to produce VOUT.

By selecting from two to nine times VIN and summing voltages, we are able to produce conversion ratios from 10 times to 31 times with only 12 fly caps instead of 30. For example, to produce a conversion ratio of 28 times, we need to select 5 times, 6 times, 8 times, and 9 times as Vs1–Vs4. Fig. 16 shows the improvement in startup energy of the proposed moving-sum charge pump compared with the traditional Dickson charge pump, with both the simulated and calculated values plotted. By reducing the number of flying caps and limiting the voltage across flying caps, the proposed structure reduces the startup energy by up to 20 times

compared with a Dickson charge pump. According to (16), this can translate to an increase in MPPT efficiency through an allowable reduction of  $\Delta V$ sol, opt by  $\sim 4.5 \times$ .

Approximation:0.5\*(R+1)\*Vin<0.5\*1/M\*VBAT

CR+1

VBAT/2

Vmult

Ø3

Vmult=0.5\*(R+1)\*Vin\*M

Switched-

Capacitor

Amplifier

Ø1Ø2

In addition to the moving-sum charge pump, alternative hybrid charge pump structures can also be considered. The SAR dc–dc converter proposed in [14] is modified here for stepup conversion. This structure achieves fine-grain conversion ratios by reconfiguring 1:2 doublers. Similar to the moving-sum charge pump, a new hybrid structure, which is referred to as binary charge pump, is compared here as an alternative. As shown in Fig. 17, the binary charge pump has two stages, a doubler chain stage that produces 2 times, 4 times, 8 times, and 16 times VIN, a voltage mux that selects four voltages (Vs1–Vs4), and a summing stage that sums

5bits

Ø1: Reset Ø2: Multiply

Ø3:Compare

+CR



Fig. 21. (a) Circuit diagram of the mode controller. (b) Timing diagram.



Fig. 22. Die photograph.

voltages Vs1–Vs4 using four capacitors. The voltage selection is directly based on the binary representation of the conversion ratio, and this is where the name binary comes from. The operation requires two phases as shown in Fig. 18. In phase A, the doublers chain stage is connected to the four capacitors from the summing stage in parallel, charging the capacitors to the desired voltages. In phase B, the four capacitors in the summing stage are disconnected from the doublers chain stage, and connected in series to produce output VOUT.

In theory, SAR and binary charge pump can further reduce the startup energy by reducing the number of flying capacitors. However, these two doubler-based structures have lower steady-state efficiency compared with Dickson-based structures such as the moving-sum charge pump. Fig. 19 compares the simulated efficiencies of traditional Dickson, moving-sum, SAR, and binary charge pumps. Moving-sum charge pump maintains a higher efficiency over a wider range of input voltages than binary or SAR structures. Therefore, considering both startup and steady-state losses, as well as a large desired input range, the moving-sum charge pump is implemented to achieve better overall performance.

#### C. Automatic Conversion Ratio Modulator

ACRM (Fig. 20) is only enabled in the transfer phase to automatically increase conversion ratio as Vsol decreases. For each input voltage, there is an optimal conversion ratio where the conduction loss is balanced with the switching loss. The harvester increases conversion ratio when the conduction loss is smaller than this balancing point. As an indicator of conduction loss, we use  $\Delta V$ , defined as conversion ratio CR multiplied by VIN minus VBAT, which is the difference between unloaded charge pump output and loaded output.

Conversion ratio is modulated by calculating  $\Delta V$  for the next conversion ratio,  $\Delta V_{CR+1}$ , and comparing it to the optimal  $\Delta V$ , which is approximated to be a fraction of VBAT. We reduce all voltages here by half for easy implementation. After cleanup, the equation used for implementation is (CR+1) \*Vin \*M < VBAT, where M is a constant.

The left-hand side of the equation is defined to be Vmult, which is generated using an SC amplifier in phases 1 and 2, and then compared with half VBAT in phase 3. If Vmult is smaller than half VBAT, the comparator fires and conversion ratio increases by 1. This conversion ratio signal will be sent to a switch selection module to change the configuration of the moving-sum charge pump. Since Vsol is guaranteed to monotonically decrease during transfer phase, the logic for ratio modulation is simplified as it only needs to check for improved performance in one direction (i.e., toward a higher CR).

#### D. Low-Power Mode Controller

The mode controller (Fig. 21) controls the transition between harvest and transfer phases. It consists of a flip-flop to store the current state, an MUX, two pulse generators to clock the flip-flop at phase transitions, and delay cells to ensure correct timing. The complete controller has leakage power of less than 15 pW, which is critical to enabling harvesting at ultralow input power levels. Asynchronous logic is used to save clock power.

#### **IV. MEASUREMENTS**

The chip is fabricated in 180-nm CMOS and occupies 1.7 mm  $\times$  1.6 mm (Fig. 22). The design uses 12 flying capacitors with total cap size of 1.5 nF. The chip is tested with controlled lighting conditions using a 0.01-mm<sup>2</sup> GaAs solar cell and two stacked CMOS solar cells, which are 0.001 and 0.037 mm<sup>2</sup>, respectively. Harvester output energy is accumulated on a test capacitor, whose voltage is continuously monitored by electrometer.

Fig. 23 shows the measurement of the ACRM across VIN, which is swept from 0.26 to 0.6 V. The ACRM can select the correct conversion ratio within two codes from optimal, resulting in only a few percent efficiency degradation for most of the conversion ratios.

Fig. 24 characterizes the moving-sum charge pump efficiency versus output power. It achieves 60% peak efficiency at 256-nW output power when converting solar voltage to a 4-V battery voltage, and maintains  $\geq$ 45% efficiency over the 4-nW–4- $\mu$ W output power range.

The efficiency improvement of the proposed discontinuous harvester over the conventional continuous harvester is compared in Fig. 25. Data points with Pmppt >66 pW are taken using the GaAs solar cell, and data points with Pmppt <66 pW are taken using stacked CMOS solar cells



Fig. 23. ACRM measurements.



Fig. 24. Moving-sum charge pump measurements.

TABLE I Performance Summary and Comparison

Metric	[7]	[6]	[5]	This Work
Technology	0.18µ	0.18µ	0.18µ	0.18µ
Topology	Switched- Capacitor	Boost with Voltage Doubler	Buck boost	Switched- Capacitor
Input voltage	0.14-0.5V	20-70mV	N/R	0.25-0.65V
Output voltage	2.2-5.2V	1.5-1.9V	1V,1.8V and 3V	3.8-4V
CP Peak Efficiency	50% @ 0.45V	56% @ 0.1V	N/R	60% @ 0.5V
End-to-end Peak Efficiency	50% @ 100nW output power <sup>1</sup>	56% @ 0.9nW output power <sup>1</sup>	83% @ 90µW <sup>1</sup>	50% @ 8nW
Input Power Range	12.5nW-12.5µW w/ >40% efficiency <sup>1</sup>	1.2nW-8nW w/>50% efficiency <sup>1</sup>	1.47µW-14mW w/>68% efficiency <sup>1</sup>	113pW – 1.5µW w/ >40% efficiency
Efficiency at minimum input power	> 30% @ 4.5nW	53% @ 1.2nW	68% @ 1.47µW	37% @ 66pW 22% @ 20pW
Harvestable Power Range (Pin,max/Pin,min)	1000	7	9500	13000
Idle Power Consumption	3nW	544pW	400nW	<15pW

N/R: Not reported

<sup>1</sup>Estimated number from the paper

to boost solar voltage at very low input light levels. End-toend efficiency is calculated as harvester output power Pout divided by source power at its maximum power point. For the continuous harvester, its harvestable input power range is approximately 10 nW–1.5  $\mu$ W. The proposed discontinuous harvester efficiency can harvest from 113 pW to 1.5  $\mu$ W with



Fig. 25. Harvester measurements.



Fig. 26. Measured tradeoff between transfer phase efficiency and solar efficiency.



Fig. 27. Measured dependence of transfer phase efficiency on Cbuf size.

efficiency >40%. The discontinuous harvester also provides >20% efficiency at 20 pW.

As described earlier, there is a tradeoff between MPPT efficiency and charge pump efficiency that is quantified by  $\Delta$  Vsol. Measurements in Fig. 26 show that as  $\Delta$  Vsol increases, the solar efficiency decreases, while charge pump efficiency increases. This yields an optimal  $\Delta$  Vsol of 120 mV

in this case. This measurement confirms the previous efficiency analysis. Fig. 27 provides measurements to demonstrate the relationship between Cbuf size and transfer phase efficiency, which confirms that increased Cbuf size will initially improve transfer efficiency and then saturate at peak efficiency.

#### V. CONCLUSION

This paper has presented a discontinuous harvester where the solar efficiency and charge pump efficiency are separated and co-optimized to allow for a wider output power range and lower harvesting floor. The harvester achieves 13 000 times input power range, 20-pW harvesting floor, and less than 15-pW idle power (Table I). To optimize discontinuous harvesting, a new moving-sum charge pump topology is implemented to reduce startup energy. An ACRM increments conversion ratio to match decreasing input voltage while charge transfers to the battery. A low leakage mode controller is implemented to reduce idle power, lowering the harvesting floor.

#### Appendix

### A. End-to-End Efficiency

End-to-end efficiency is defined as the total output energy from the harvester  $E_{out}$  divided by energy generated by the solar cell  $E_{mppt}$  when biased at its maximum power point (A.1). Total output energy is the output energy generated in transfer phase  $E_{out,tran}$  minus the total leakage energy from the battery in the harvest phase  $E_{\text{leak}}$  (A.2). Leakage power in the transfer phase is small (1.2 nW, simulated) compared with the steady-state output power in the transfer phase (>170 nW, measured), and is accounted for in  $E_{\text{out,tran}}(E_{\text{out,tran}})$  is the output energy of the charge pump minus the leakage energy in the transfer phase).  $E_{out,tran}$  can be expressed as the product of solar efficiency  $Eff_{solar} =$ (energy accumulated on Cbuf)/( $E_{mppt}$ ) in the harvest phase and overall charge pump efficiency in the transfer phase  $Eff_{tran} = (E_{out,tran})/(energy accumulated on Cbuf)$  (A.3). Therefore, total efficiency can be expressed in (1), where  $P_{\text{leak}}$ is the leakage power in harvest phase

$$\mathrm{Eff}_{\mathrm{tot}} = \frac{E_{\mathrm{out}}}{E_{\mathrm{mppt}}} \tag{A.1}$$

$$Eff_{tot} = \frac{E_{out,tran} - E_{leak}}{E_{mppt}}$$
(A.2)

$$Eff_{tot} = \frac{E_{mppt} * Eff_{solar} * Eff_{tran} - E_{leak}}{E_{mppt}}.$$
 (A.3)

#### B. Solar Efficiency

The solar efficiency in the harvest phase is defined as the ratio of the average power  $P_{\text{solar,avg}}$  accumulated on Cbuf in the harvest phase, and the maximum power point of the solar cell  $P_{\text{mppt}}$ , as shown

$$Eff_{solar} = \frac{P_{solar,avg}}{P_{mppt}}$$
(A.4)

where  $P_{\text{solar,avg}}$  is the average power harvested over duration of harvest phase (A.5). By definition, it can be expressed as the integral of P(v) (instantaneous output power of the solar cell when biased at voltage v) from t0 to t1 divided by the duration of harvest phase, where t0 and t1 are the start and end times of the harvest phase, respectively:

$$P_{\text{solar,avg}} = \frac{\int_{t0}^{t1} P(v)dt}{\int_{t0}^{t1} dt}.$$
 (A.5)

Here, dt can be calculated by (A.6) and simplified to (A.7)

$$dt = \frac{1}{2} * \text{Cbuf} * \frac{(v + dv)^2 - v^2}{P(v)}$$
(A.6)

$$dt = \frac{1}{2} * \text{Cbuf} * \frac{2vdv}{P(v)}.$$
(A.7)

Therefore, solar efficiency can be expressed in (4).

#### C. Model Simplifications

P(v), which is defined as the solar cell output power when biased at v, is the product of v and  $I_{solar}(v)$ .  $I_{solar}(v)$  is supposed to be modeled as (A.8) [27], where  $I_0$ ,  $I_L$ ,  $R_s$ , k, and  $R_p$ are variables related to solar cell characteristics. Unfortunately, there are no analytical solutions to (A.8). To simplify the calculation, two assumptions are made here. First, we assume  $I_{solar}(v) = Isc$  for v < Vmppt, where Isc is the short circuit current of the solar cell. Second, we set VH = Vmppt to limit the voltage range in this calculation to  $v \in [0, V \text{mppt}]$ , where VH is the voltage on Cbuf at the end of harvest phase. By assuming  $I_{solar}(v) = Isc$ , we overestimate solar output current  $I_{solar}(v)$  and, therefore, overestimate solar efficiency Eff<sub>solar</sub> in the harvest phase. The resulting error is shown in Fig. 6. By limiting VH to Vmppt, we could potentially miss the global optimal pair of VH and VL. The error compared with the optimal point found without setting VH = Vmppt is shown in Fig. 7. Practically, the optimal VH can be close to but slightly higher than V mppt for a better tradeoff between solar efficiency and overall charge pump efficiency. With the two assumptions, VH = Vmppt and  $VL = Vmppt - \Delta Vsol$ , The problem of finding the optimal pair of VH and VL is simplified to finding the optimal  $\Delta V$  sol. P(v) is simplified to (A.9)

$$I_{\text{solar}}(v) = I_L - I_0 * (e^{\frac{v + I_{\text{solar}}(v)R_s}{k}} - 1) - \frac{v + I_{\text{solar}}(v)R_s}{R_p}$$
(A.8)

$$P(v) = v * Isc. \tag{A.9}$$

Therefore, solar efficiency can be simplified as shown in (5) (Section II-B), and transfer phase efficiency can be rewritten in (6) (Section II-B) in terms of  $\Delta$ Vsol.

#### REFERENCES

- G. Chen *et al.*, "Millimeter-scale nearly perpetual sensor system with stacked battery and solar cells," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 288–289.
- [2] D. Hodgins *et al.*, "Healthy aims: Developing new medical implants and diagnostic equipment," *IEEE Pervasive Comput.*, vol. 7, no. 1, pp. 14–21, Jan./Mar. 2008.
- [3] I. Lee, W. Lim, A. Teran, J. Phillips, D. Sylvester, and D. Blaauw, "A >78%-efficient light harvester over 100-to-100klux with reconfigurable PV-cell network and MPPT circuit," in *IEEE ISSCC Dig. Tech. Papers*, Jan. 2016, pp. 370–371.

- [4] E. Carlson, K. Strunz, and B. Otis, "20mV input boost converter for thermoelectric energy harvesting," in *Proc. Symp. VLSI Circuits*, Jun. 2009, pp. 162–163.
- [5] G. Yu, K. W. R. Chew, Z. C. Sun, H. Tang, and L. Siek, "A 400 nW single-inductor dual-input-tri-output DC-DC buck-boost converter with maximum power point tracking for indoor photovoltaic energy harvesting," in *IEEE ISSCC Dig. Tech. Papers*, 2013, pp. 68–69.
- [6] S. Bandyopadhyay, P. P. Mercier, A. C. Lysaght, K. M. Stankovic, and A. P. Chandrakasan, "A 1.1nW energy harvesting system with 544pW quiescent power for next-generation implants," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 396–397.
- [7] W. Jung, S. Oh, S. Bang, Y. Lee, D. Sylvester, and D. Blaauw, "A 3nW fully integrated energy harvester based on self-oscillating switched-capacitor DC-DC converter," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 398–399.
- [8] I. Doms, P. Merken, R. Mertens, and C. Van Hoof, "Integrated capacitive power-management circuit for thermal harvesters with output power 10 to 1000μW," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 300–301.
- [9] Y. Qiu, C. Van Liempd, B. O. het Veld, P. G. Blanken, and C. Van Hoof, "5μW-to-10mW input power range inductive boost converter for indoor photovoltaic energy harvesting with integrated maximum power point tracking algorithm," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 118–120.
- [10] R. Enne, M. Nikolic, and H. Zimmermann, "A maximum powerpoint tracker without digital signal processing in 0.35μm CMOS for automotive applications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 102–104.
- [11] W.-C. Liu, Y.-H. Wang, and T.-H. Kuo, "An adaptive load-line tuning IC for photovoltaic module integrated mobile device with 470μs transient time, over 99% steady-state accuracy and 94% power conversion efficiency," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 70–71.
- [12] S. Uprety and H. Lee, "A 43V 400mW-to-21W global-search-based photovoltaic energy harvester with 350μs transient time, 99.9% MPPT efficiency, and 94% power efficiency," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 404–405.
- [13] Y. K. Ramadass, "Energy processing circuits for low-power applications," Ph.D. dissertation, Dept. Elect. Eng. Comput. Sci., Massachusetts Inst. Technol., Cambridge, MA, USA, 2009.
- [14] S. Bang, D. Blaauw, and D. Sylvester, "A successive-approximation switched-capacitor DC–DC converter with resolution of  $V_{IN}/2^N$  for a wide range of input and output voltages," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 543–556, Feb. 2016.
- [15] D. Jeon *et al.*, "An implantable 64nW ECG-monitoring mixed-signal SoC for arrhythmia diagnosis," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 416–417.
- [16] A. Donida *et al.*, "A 0.036mbar circadian and cardiac intraocular pressure sensor for smart implantable lens," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 392–393.
- [17] K. Paralikar *et al.*, "An implantable 5mW/channel dual-wavelength optogenetic stimulator for therapeutic neuromodulation research," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 238–239.
- [18] X. Liu and E. Sanchez-Sinencio, "A single-cycle MPPT charge-pump energy harvester using a thyristor-based VCO without storage capacitor," in *IEEE ISSCC Dig. Tech. Papers*, Jan. 2016, pp. 364–365.
- [19] M. Shim, J. Kim, J. Jeong, S. Park, and C. Kim, "Self-powered 30 μW to 10 mW piezoelectric energy harvesting system with 9.09 ms/V maximum power point tracking time," in *IEEE ISSCC Dig. Tech. Papers*, Oct. 2014, pp. 406–407.
- [20] Y.-S. Yuk *et al.*, "An energy pile-up resonance circuit extracting maximum 422% energy from piezoelectric material in a dual-source energyharvesting interface," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 402–403.
- [21] X. Wu et al., "A 66pW discontinuous switch-capacitor energy harvester for self-sustaining sensor applications," in Proc. Symp. VLSI Circuits, Jun. 2016, pp. 90–91.
- [22] M. Wieckowski, G. K. Chen, M. Seok, D. Blaauw, and D. Sylvester, "A hybrid DC-DC converter for sub-microwatt sub-1V implantable applications," in *Proc. Symp. VLSI Circuits*, Jun. 2016, pp. 166–167.
- [23] X. Wang, J. Liu, J. Song, and Z. L. Wang, "Integrated nanogenerators in biofluid," *Nano Lett.*, vol. 7, no. 8, pp. 2475–2479, 2007.
- [24] X. Wang, J. Song, J. Liu, and Z. L. Wang, "Direct-current nanogenerator driven by ultrasonic waves," *Science*, vol. 316, no. 5821, pp. 102–105, 2007.
- [25] Y. Qin, X. Wang, and Z. L. Wang, "Microfibre–nanowire hybrid structure for energy scavenging," *Nature*, vol. 451, no. 7180, pp. 809–813, 2008.

- [26] M. Rasmussen, R. E. Ritzmann, I. Lee, A. J. Pollack, and D. Scherson, "An implantable biofuel cell for a live insect," *J. Amer. Chem. Soc.*, vol. 134, no. 3, pp. 1458–1460, 2012.
- [27] J. L. Díaz-Bernabé and A. Morales-Acevedo, "Photovoltaic module simulator implemented in SPICE and Simulink," in *Proc. 12th Int. Conf. Elect. Eng., Comput. Sci. Autom. Control (CCE)*, Oct. 2015, pp. 1–5.



Xiao Wu received the B.S. degrees in electrical engineering and computer science from the University of Michigan, Ann Arbor, MI, USA, and Shanghai Jiao Tong University, Shanghai, China, and M.S. degree in electrical engineering from the University of Michigan, Ann Arbor, MI, USA. She is currently pursuing the Ph.D. degree with the University of Michigan.

Her research interests include harvester design for sensor nodes and power management.



Yao Shi received the B.S. degree in electronic and information engineering from Zhejiang University, Hangzhou, China, in 2013, and the M.S. degree in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2016, where he is currently pursuing the Ph.D. degree.

His research interests include analog/RF integrated circuits design, ultralow power radio architecture and circuit, and ultralow power wireless sensor node.



**Supreet Jeloka** (S'14) received the B.Tech. degree in electronics and communication engineering from the National Institute of Technology, Warangal, India, in 2007, and the M.S. degree in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2013, where he is currently pursuing the Ph.D. degree.

He was with Freescale, India, as a Senior Design Engineer. His research interests include low power circuits, memory design, memory-based computing, interconnect fabrics, and hardware security.



Kaiyuan Yang received the B.S. degree in electronics engineering from Tsinghua University, Beijing, China, in 2012, and the M.S. degree in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2014, where he is currently pursuing the Ph.D. degree.

His research interests include low-power digital and mixed-signal circuit design, and hardware security.

Mr. Yang was a recipient of the Best Paper Award at the 2015 IEEE International Symposium on Cir-

cuits and Systems and the 2016 IEEE Symposium on Security and Privacy.



**Inhee Lee** received the B.S. and M.S. degrees in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2006 and 2008, respectively, and the Ph.D. degree from the University of Michigan, Ann Arbor, MI, USA, in 2014.

He is currently a Research Scientist with the University of Michigan. His research interests include energy harvesters, power management circuits, battery monitoring circuits, and low-power sensing systems for Internet of Things applications.



Yoonmyung Lee received the B.S. degree in electronic and electrical engineering from the Pohang University of Science and Technology, Pohang, South Korea, in 2004, and the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2008 and 2012, respectively.

From 2012 to 2015, he was with the University of Michigan as a Research Faculty. In 2015, he joined Sungkyunkwan University, Seoul, South Korea, as an Assistant Professor. His current research inter-

ests include energy-efficient integrated circuits design for low-power highperformance very large scale integration systems and millimeter-scale wireless sensor systems.

Dr. Lee has received the Samsung Scholarship and the Intel Ph.D. Fellowship.



**Dennis Sylvester** (F'11) received the Ph.D. degree in electrical engineering from the University of California at Berkeley, Berkeley, CA, USA, in 1999.

He has held research staff positions with the Advanced Technology Group of Synopsys, Mountain View, CA, the Hewlett-Packard Laboratories, Palo Alto, CA, and as a Visiting Professor with the National University of Singapore, Singapore, and Nanyang Technological University, Singapore. He serves as a Consultant and a Technical Advisory Board Member for electronic design automation and

semiconductor firms in these areas. He co-founded Ambiq Micro, Austin, TX, USA, a fabless semiconductor company developing ultralow power mixedsignal solutions for compact wireless devices. He is currently a Professor of Electrical Engineering and Computer Science with the University of Michigan, Ann Arbor, MI, USA, where he is also the Director of the Michigan Integrated Circuits Laboratory, a group of ten faculty and over 70 graduate students. He has authored over 375 articles along with one book and several book chapters. He holds 20 U.S. patents. His current research interests include the design of millimeter-scale computing systems and energy efficient nearthreshold computing.

Dr. Sylvester was a recipient of the NSF CAREER Award, the Beatrice Winner Award at the IEEE International Solid-State Circuits Conference (ISSCC), the IBM Faculty Award, the SRC Inventor Recognition Award, and the eight best paper awards and nominations. He was also a recipient of the ACM SIGDA Outstanding New Faculty Award and the University of Michigan Henry Russel Award for Distinguished Scholarship. His dissertation in Ph.D. was recognized with David J. Sakrison Memorial Prize as the Most Outstanding Research at the Electrical Engineering and Computer Science Department, University of California at Berkeley. He served on the Executive Committee of the ACM/IEEE Design Automation Conference and serves on the Technical Program Committee of the IEEE International Solid-State Circuits Conference. He has also served as an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, and a Guest Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II.



**David Blaauw** (F'12) received the B.S. degree in physics and computer science from Duke University, Durham, NC, USA, in 1986, and the Ph.D. degree in computer science from the University of Illinois at Urbana–Champaign, Champaign, IL, USA, in 1991.

He was with Motorola, Inc., Austin, TX, USA, where he was the Manager of the High Performance Design Technology Group. Since 2001, he has been with the Faculty of the University of Michigan, Ann Arbor, MI, USA, where he is currently a Professor.

He has authored over 450 papers and holds 40 patents. His current research interests include very large scale integration design with particular emphasis on ultralow power and high performance design.

Dr. Blaauw was the Technical Program Chair and the General Chair of the International Symposium on Low Power Electronic and Design. He was also the Technical Program Co-Chair of the ACM/IEEE Design Automation Conference and a member of the International Solid-State Circuits Conference Technical Program Committee.