23.3 A 3nW Fully Integrated Energy Harvester Based on Self-Oscillating Switched-Capacitor DC-DC Converter

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Recent advances in low-power circuits have enabled mm-scale wireless systems [1] for wireless sensor networks and implantable devices, among other applications. Energy harvesting is an attractive way to power such systems due to the limited energy capacity of batteries at these form factors. However, the same size limitation restricts the amount of harvested power, which can be as low as 10s of nW for mm-scale photovoltaic cells in indoor conditions. Efficient DC-DC up-conversion at such low power levels (for battery charging) is extremely challenging and has not yet been demonstrated.

Boost DC-DC converters are widely used to harvest energy from DC sources and yield high conversion efficiency [2]. However, they require a large off-chip inductor at low harvested power levels, increasing system size. Alternatively, switched-capacitor (SC) DC-DC converters can be fully integrated on-chip and are favored for form-factor constrained applications [3-8]. However, at low power levels, SC converter efficiency has been constrained by overheads of clock generation and level-conversion to drive the switch capacitors. As a result, efficient SC converter operation has been limited to the μW range.

This paper presents a fully integrated energy harvester maintaining >35% end-to-end efficiency when harvesting from a 0.84mm² solar cell in low light condition of 260lux, converting 7nW input power from 250mV to 4V. The key contribution of this work lies in the proposed SC DC-DC voltage doubler structure, in which an oscillator is completely internalized within the SC network. This eliminates power overhead of clock generation and level shifting, and enables higher efficiency at lower power levels. Voltage doublers are cascaded to form a complete harvester with a wide load range from 5nW to 5μW and self-starting operation down to 140μW. Since each doubler is self-oscillating, the frequency of each stage can be independently modulated, thereby optimizing the overall conversion efficiency. The harvester’s conversion ratio is configurable from 9× to 23× and idle power consumption is less than 3nW.

Figure 23.3.1 shows a conventional SC DC-DC voltage doubler that includes a clock generator, level shifter, and clock buffers. Each of these blocks introduces power overhead, reducing efficiency. The proposed doubler consists of two stacked ring oscillators with the output nodes of corresponding stages connected through flying caps (Cs). In each stage, inverters from the top and bottom rings either charge or discharge the flying cap thereby transferring power to the upper ring. Simultaneously, the inverters drive the next stage in their ring, creating a multi-phase DC-DC converter with overlapping charge/discharge phases and self-sustaining operation. Because the two oscillators are synchronized at every stage, phase mismatch is <0.01μs, reducing contention loss to <1% of switching loss (simulation) and avoiding the need for non-overlapping clocks. RDLY is a delay element that ensures matching of the flying cap charging/discharging time to the oscillation period. In the harvester, this delay is automatically tuned to balance switching and conduction losses and maintain optimum conversion efficiency across a range of load currents.

The voltage doubler and energy harvester are fabricated in 0.18μm CMOS (Fig. 23.3.3). The voltage doubler and energy harvester are fabricated in 0.18μm CMOS (Fig. 23.3.3). The voltage doubler and energy harvester are fabricated in 0.18μm CMOS (Fig. 23.3.3). The voltage doubler and energy harvester are fabricated in 0.18μm CMOS (Fig. 23.3.3). The voltage doubler and energy harvester are fabricated in 0.18μm CMOS (Fig. 23.3.3). The voltage doubler and energy harvester are fabricated in 0.18μm CMOS (Fig. 23.3.3). The voltage doubler and energy harvester are fabricated in 0.18μm CMOS (Fig. 23.3.3). The voltage doubler and energy harvester are fabricated in 0.18μm CMOS (Fig. 23.3.3). The voltage doubler and energy harvester are fabricated in 0.18μm CMOS (Fig. 23.3.3). The voltage doubler and energy harvester are fabricated in 0.18μm CMOS (Fig. 23.3.3). The voltage doubler and energy harvester are fabricated in 0.18μm CMOS (Fig. 23.3.3). The voltage doubler and energy harvester are fabricated in 0.18μm CMOS (Fig. 23.3.3).

The conversion ratio is adjusted by changing the number of cascaded stages. In addition, we propose a new adjustment scheme where the VLOW port of a doubler is switched between VGH and VNEG. If VLOW is set to VNEG, the voltage across the flying capacitor increases, resulting in VOUT = (VNEG+VREF)² - 2*VLOW*VREF. If VLOW is set to GND for 4 cascaded stages, overall conversion ratio is 16×. However, if final stage VLOW is set to VNEG, overall conversion ratio increases by 1×, becoming 17×. This allows tuning the setting VLOW to Vnull, where the voltage decreases conversion ratio. In a binary manner, the conversion ratio is controlled from 9× to 23×. Measured results in Fig. 23.3.4 demonstrate that a 0.35V input can be converted to a 2.2 to 5.2V voltage range with similar conversion efficiencies across settings.

To enable cold start of the complete system, the control logic operates between VNEG and Vref rails. Upon initial system startup, VNEG and Vref become available and allow the control logic to turn on and configure the switches. As each stage is powered up, its internal frequency modulation is enabled and begins to control the frequency for optimum efficiency.

The voltage doubler and energy harvester are fabricated in 0.18μm CMOS (Fig. 23.3.7). Figure 23.3.4 shows a single doubler with >70% efficiency across 1nA to 0.35mA input current (×10 range), with low idle power consumption of 170μW. Figure 23.3.5 shows measured results of the complete harvester. When Vnull=4.5V, the harvester delivers 5nW to 5μW output power with >40% efficiency, and has an idle power consumption <3nW. For Vnull=0.25V, corresponding to a solar cell under very low light, the harvester can take in between 10nW and 120nW to charge a 4V battery voltage with >35% efficiency. Measured results with a small silicon solar cell (0.84mm²) show actual harvesting operation under dim light of <100lux. The harvester cold starts with <200lux of light and 6nW power source. Figure 23.3.6 summarizes the performance of the proposed design and compares it to prior work.

References:

Figure 23.3.1: Concept of the proposed voltage doubler.

Figure 23.3.2: Schematic of the voltage doubler.

Figure 23.3.3: Structure of the harvester.

Figure 23.3.4: Measured results of the doubler and harvester.

Figure 23.3.5: Measured results of the harvester.

Figure 23.3.6: Performance summary and comparison.
Figure 23.3.7: Die micrograph of the 0.18µm CMOS test chip.