# 45pW ESD Clamp Circuit for Ultra-Low Power Applications

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***Abstract*- Novel ultra low-leakage ESD power clamp designs for wireless sensor applications are proposed and implemented in 0.18µm CMOS. Using new biasing structures to limit both subthreshold leakage and GIDL, the proposed designs consume as little as 43pW at 25˚C and 119nW at 125˚C with 4500V HBM level and 400V MM level protection, marking an 18−139× leakage reduction over conventional ESD clamps.**

## I. Introduction

Robustness against electrostatic discharge (ESD) is a critical reliability issue in advanced CMOS technologies. To prevent circuit damage due to ESD events (which can expose the circuit to kV range voltages), ESD clamp circuits are typically incorporated in supply pad library cells. These circuits use extremely wide devices (100s of µm) and thus exhibit leakage currents of 10nA to 10µA (at 25˚C and 125˚C, respectively) despite the use of various low power approaches [1-4]. Recently, there has been increased interest in ultra-low power wireless sensor node systems [5, 6] with constrained battery sizes and system standby power budgets as low as 10-100nW. Considering the need for multiple power pads, these systems cannot use existing ESD structures due to their high leakage, thereby compromising their reliability. To address this challenge, we propose three ultra-low leakage ESD circuits that use special biasing structures to reduce subthreshold leakage and gate-induced drain leakage (GIDL) while maintaining ESD protection. In 180nm silicon test chip results, we demonstrate 10s of pA (nA) operation at room temperature (125°C), which is a >100× improvement over prior state of the art.

## II. Proposed ESD Techniques

A standard commercial ESD clamp circuit is shown in Fig. 1 and consists of an RC filter and inverter to detect the ESD event, as well as a large MOSFET to remove electrostatic charge. All transistors are thick-oxide high Vt devices. When a high voltage is applied to the supply rail due to an ESD event, transistor M2 turns on, pulling up the detection node and allowing the electrostatic charge to be dissipated through the large M4 shunt device. Waveforms for a 7kV Human-Body Model discharge are shown in Fig. 4. The key parameters associated with achieving high voltage protection are M4 size and the speed at which the detection node is pulled up. After the charge is dissipated, the resistor pulls up the inverter input to turn off the clamp.

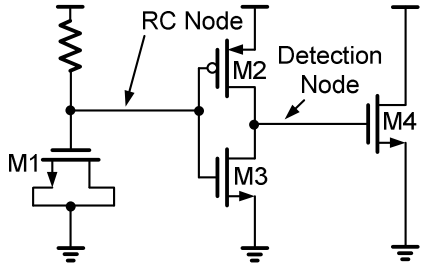


Fig. 1. Standard ESD schematic.

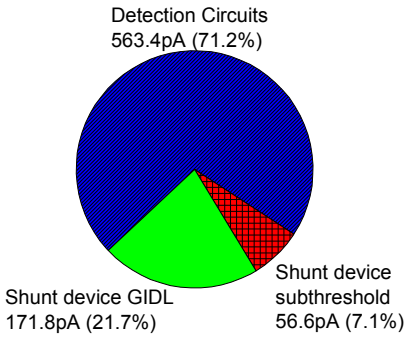


Fig. 2. Power breakdown of a standard ESD clamp circuit.

Fig. 2 gives the simulated power breakdown of this conventional design, with two major components: 1) Detection circuits, and particularly, pull-up device M2, which dominates leakage as it is sized up to speed detection and also exhibits poorer subthreshold slope compared to NMOS; 2) the large shunting device M4. Due to the high supply voltage

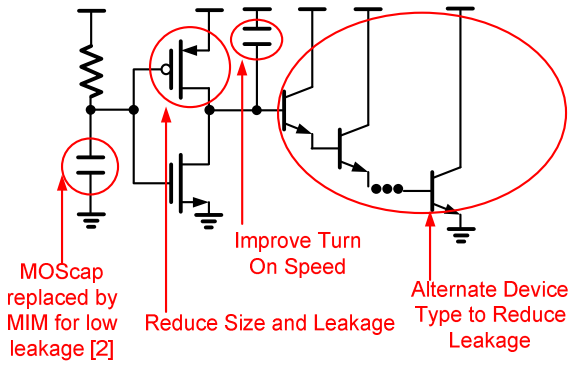


Fig. 3. The modified BJT based structure.

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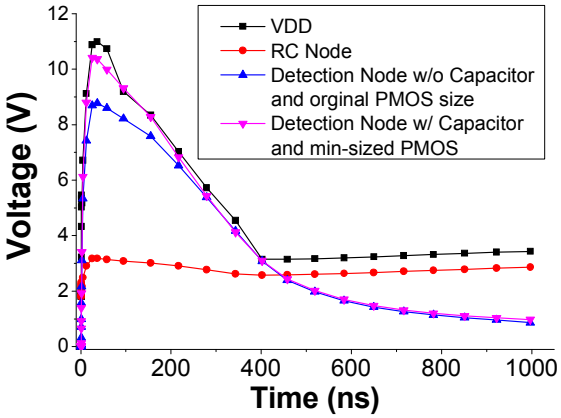



Fig. 4. Simulation waveform of the modified BJT based structure.

(≥1.8V), GIDL of M5 is larger than its subthreshold leakage.

To reduce these leakage sources, we propose and test three circuit structures. The first and most straightforward approach is shown in Fig. 3. To address M2 leakage, an assisting capacitor is added. At the onset of an ESD event, the supply voltage rises rapidly and this assisting capacitor couples the detection node up, allowing the PMOS to be down-sized (near min-size), while maintaining the same effective turn-on speed and ESD robustness. Simulated waveforms of the detection node in Fig. 4 show that the assisting capacitor with downsized M2 slightly improves response time. Note that although leakage through the MOS capacitor in this technology is small (<2pA), for a scalable low-leakage approach, a MIMCAP is used in the RC filter (as in [2]). To limit M4 leakage we employ a BJT, which provides lower off-current than MOSFETs. However, in standard CMOS technologies only parasitic BJTs with small current gains are available, making it necessary to use a Darlington-like structure.

Overall, these modifications offer a 10× (104×) leakage reduction at 25°C (125°C) (silicon measurements below). However, the parasitic BJTs introduce several technology scaling concerns that make MOS-based solutions preferable. In particular, from simulations the base-emitter current gain drops from 25 in 180nm to 5 in 65nm. Also, bipolar clamp

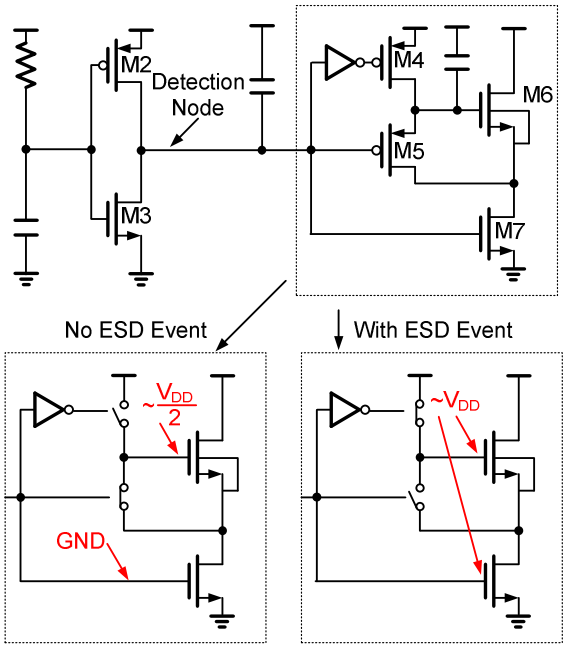



Fig. 5. Proposed GIDL reduction scheme.

snapback voltage decreases with technology scaling more rapidly than MOSFETs [8], reducing effectiveness for ESD protection. We therefore also propose two MOS-based structures that offer similar leakage reduction gains with better scalability and improved density. A well-known approach to reduce MOSFET leakage is stacking, which yields a 2.9× subthreshold leakage reduction in 180nm CMOS. However, as noted earlier, GIDL dominates leakage in the shunt device and hence stacking alone only reduces total leakage by 17%.

The first method to address GIDL in an MOS shunt device is shown in Fig. 5 and has similarity with [7]. When there is no ESD event the gate and source of M6 are shorted and the stacked shunt transistors M6 and M7 act as a voltage divider. As a result, the key GIDL parameter $V_{dg}$ is reduced by half for both transistors, lowering GIDL by 5.4×. When an ESD event occurs, the two MOS shunts fully turn on to remove the electrostatic charge. The same concept can be extended to a stack of 3 devices; simulations across temperature in Fig. 6 show temperature stability across a wide range (-20˚C to 125˚C). The 3-stack structure provides minimum leakage for this approach (denoted GIDL-1). Further extending the

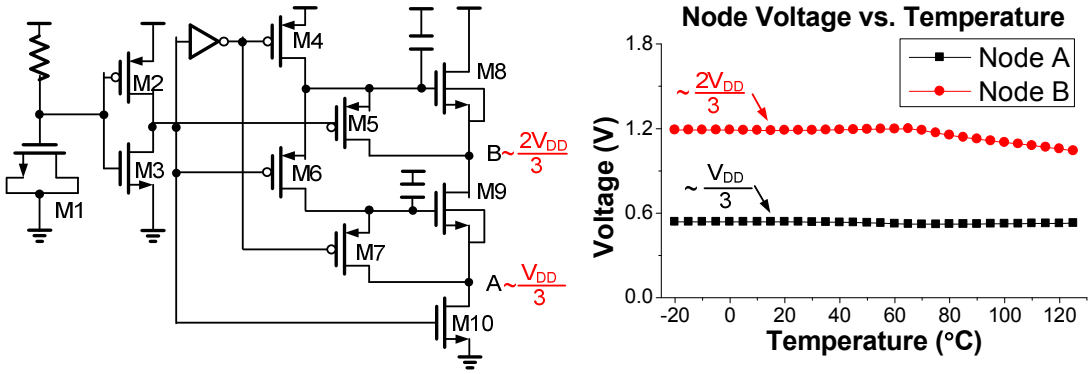



Fig. 6. GIDL reduction scheme for 3-stack (GIDL-1) with simulated internal node voltages across temperature at 1.8V.

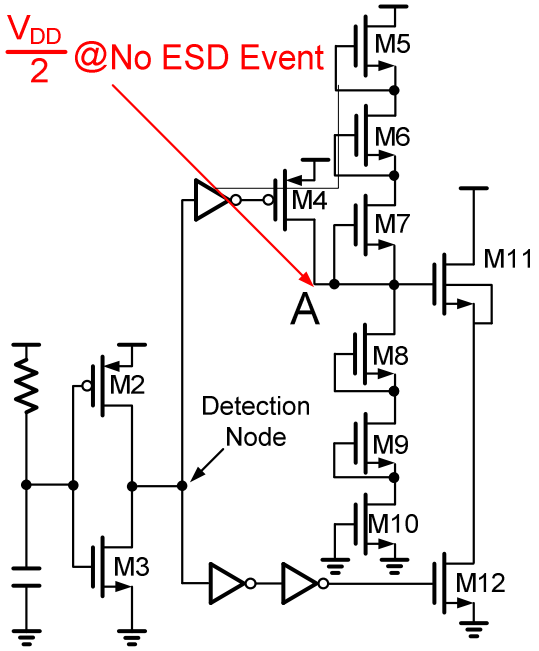



Fig. 7. Leakage-based GIDL reduction method (GIDL-2)

method to a 4-stack degrades shunt on-current, requiring device up-sizing for sufficient ESD protection and leading to higher leakage.

The second GIDL reduction approach (denoted GIDL-2) is given in Fig. 7. In this structure, a bias voltage of approximately VDD/2 is generated by a diode stack (M5-M10), which is then applied to the topmost stacked output device (M11) to reduce GIDL in M11 and M12. Since there is no need for leaky PMOS switches in GIDL-2, total transistor area and overall leakage is reduced. Note that diode-connected NMOS M5-M10 have minimum W (with increased L) since they only need to overcome the subthreshold leakage of M4 and gate leakage of M11 to maintain VDD/2 at node A. As a result, the diode stack leakage is negligible. Simulations across temperature/process show the stability of node A voltage (Fig. 8). During an ESD event node A is charged to VDD through M4 and then slowly discharges to VDD/2 through the diode stack. During this relaxation time (350µs in simulation) the ESD clamp experiences substantial GIDL. However, since ESD events are rare, the impact on total energy is minimal and the low quiescent current of the structure far outweighs it. Simulated leakage power breakdown of GIDL-2 is shown in Fig. 8, showing a 15.3 − 115× reduction (25 − 125°C) compared to a conventional commercial clamp.

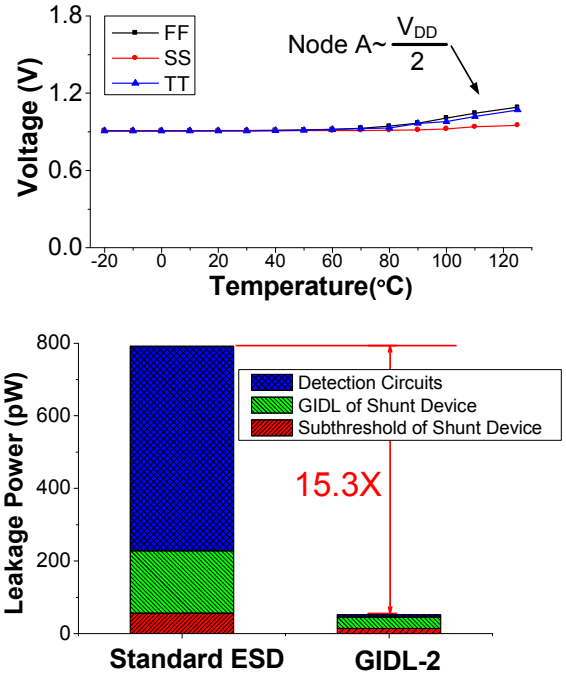



Fig. 8. Simulated internal node voltage across temperature and corners as well as leakage power breakdown of GIDL-2.

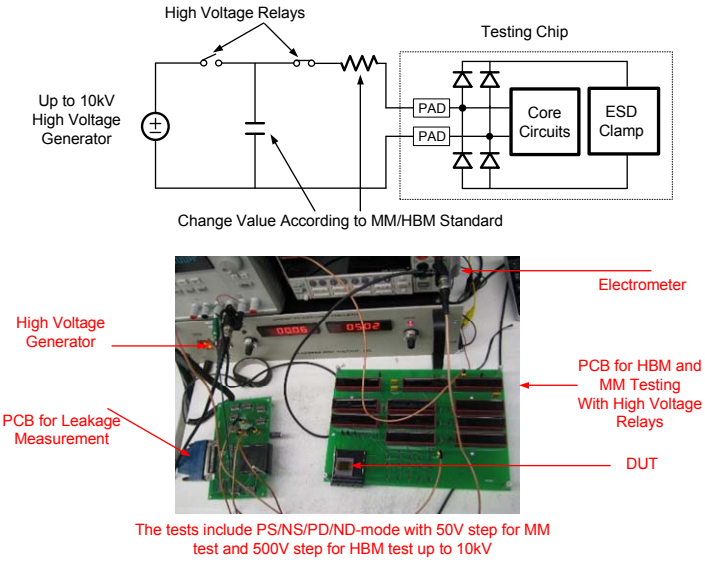
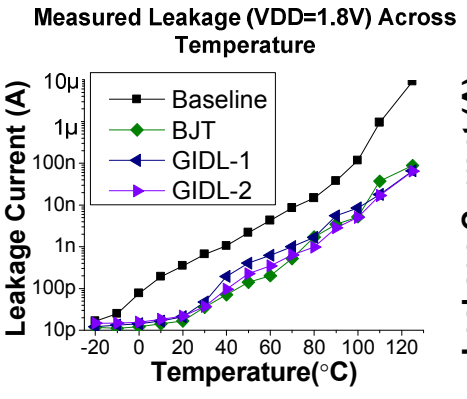
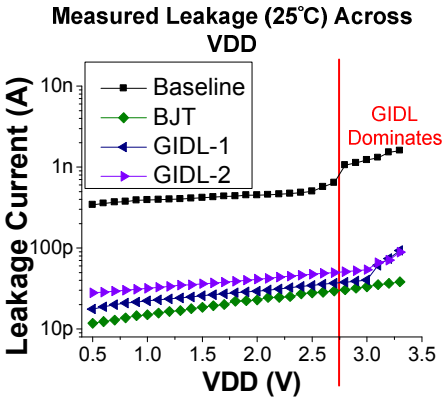



Fig. 9. Testing setup with high voltage generator for human body model (HBM) and machine model (MM).

## III. Measurement Reasults

The three proposed ESD structures (BJT, GIDL-1, GIDL-2) and a commercial ESD clamp circuit (baseline) were fabricated in a standard 180nm CMOS process. In addition, an ESD structure using smaller devices and offering a lower protection level was integrated with a mm-scale microsystem [5] to meet its nW system power budget. The human body model (HBM) and machine model (MM) are evaluated on the ESD structures (Fig. 9). Device leakage current is measured after each discharge of the HBM or MM test. We use a conventional definition of failure, namely the smallest voltage at which either 1) the structure exhibits a 30% increase in leakage, or 2) an analog block connected to the ESD pads functionally fails.



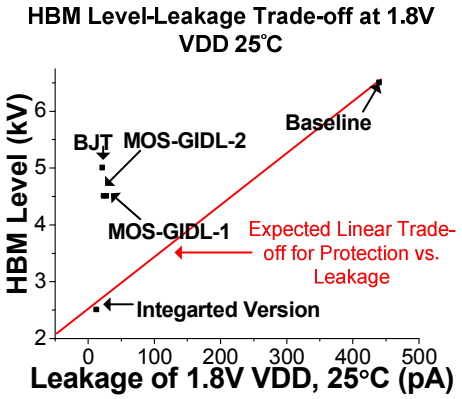




Fig.10. Measured leakage results across temperature and power supply

Fig.11.Measured scatter plot of baseline and 3 proposed structures

The measured leakage of each structure across temperature and VDD is shown in Fig. 10. The proposed clamps have lower leakage than the baseline design throughout the temperature range of 0°C to 125°C and VDD from 0.5V to 3.3V. The BJT structure has the lowest leakage (22pA) at room temperature, a 20× reduction over the baseline. At 125° C, GIDL-1 and GIDL-2 structures consume 67.8nA and 66nA, respectively, compared to 16.52µA for the baseline. A scatter plot showing ESD protection and leakage (25°C) of the 4 measured structures is also given in Fig. 11. The expected linear trend between protection level and leakage highlights the gains achieved by the proposed structures beyond straightforward device down-sizing. A histogram of leakage current for GIDL-2 at 85°C and 1.8V across 20 measured dies from one wafer is shown in Fig. 12. Nearly all dies consume 1.6−2.1nA with average leakage of 1.91nA and standard deviation of 317pA. The integrated version shows 13pA leakage at 25°C with 2.5kV HBM level and 300V MM level. Table 1 provides a summary table including a comparison of HBM and MM levels of the proposed structures to both the literature and measured baseline pads. Overall the proposed GIDL-2 structure provides 18−139× leakage reduction over commercial ESD clamps with 70-100% of ESD protection levels while avoiding special devices such as SCR. Die photos are given in Fig. 13.

Table 1. Summary table of proposed structures and related work.

| ESD Structure | Technology | Area (µm²) | HBM Level (kV) | MM Level (V) | Leakage 1.8V, 25°C | Leakage 1.8V, 125°C |
|---|---|---|---|---|---|---|
| Baseline Commercial Clamp | 0.18µm | 17500 | 6.5 | 400 | 440pA | 9.18µA |
| BJT | 0.18µm | 67200 | 5.0 | 350 | **22pA** | 88.1nA |
| GIDL-1 | 0.18µm | 67200 | 4.5 | 400 | **28pA** | **67.8nA** |
| GIDL-2 | 0.18µm | 44800 | 4.5 | 400 | **24pA** | **66nA** |
| Integrated Version For mm3 system [5] | 0.18µm | 35000 | 2.5 | 300 | 13pA | 41nA |
| [1] | 65nm | N/A | 4.0 | 350 | 358nA (1V) | 1.91µA (1V) |
| [2]* | 0.13µm | N/A | 6.5 | 400 | N/A | N/A |
| [3]* | 65nm | N/A | >8.0 | 750 | 228nA (1V) | 3.14µA (1V) |
| [4]* | 65nm | 1029 (7891)** | 7.0 | 325 | 96nA (1V) | 1.02µA (1V) |

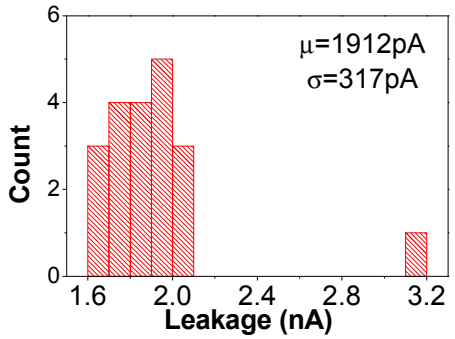



Fig.12. Measured histogram of leakage for GIDL-2 across 20 measured dies, 85°C and 1.8V.

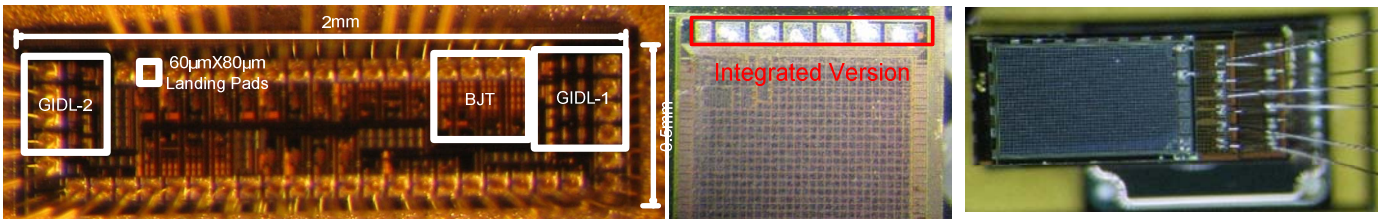



Fig. 13. Die photo. The BJT, GIDL-1, and GIDL-2 version are shown in the left, and the integrated version is shown in middle. The complete mm3 system is shown at right and the commercial clamp is measured in the same run on a different die.

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