21.5 A Current-Mode Wireless Power Receiver with Optimal Resonant Cycle Tracking for Implantable Systems

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Continuous health monitoring has become feasible, largely due to miniature implantable sensor systems such as [1]. To recharge batteries of such systems, wireless power transfer is a popular option since it is non-invasive. However, there are two main challenges: 1) strict safety regulations of incident power on human tissue; 2) small coil size for better biocompatibility. These issues reduce the received power at the coil, make it difficult to obtain sufficient power for implanted devices, and call for high power-efficiency (η_P)-transfer techniques, especially at very low received power levels.

Most conventional wireless power receivers are composed of a rectifier for AC-DC conversion, followed by a DC-DC converter or linear regulator (Figure 21.5.1). In this approach the input power (P_{IN}) at the receiver coil (L_{RX}) must be high enough to overcome the rectifier threshold voltage ($V_{TH,RECT}$), limiting the minimum harvestable input power ($P_{IN,\ MIN}$). Coil-based power receivers have a $P_{IN,\ MIN}$ in the 100's of μW to W range [2-4] while far-field RF power receivers report $P_{IN,\ MIN}$ of several μW [5,6] and a relatively low η_P of 15% at 10μW [7]. Also, charging voltage needs to be regulated to ensure battery safety. This paper proposes an approach that avoids rectification and voltage regulation. Instead, we place a capacitor in parallel with L_{RX} to form an LC tank. We then resonate the LC tank for *multiple cycles* to accumulate energy (config.1) and transfer this energy to the battery in a boost-converter fashion (config.2). This method has three advantages: 1) it significantly improves $P_{IN,\ MIN}$ by removing $V_{TH,RECT}$; 2) resonating an LC tank for multiple cycles builds up energy in the LC tank while most control circuits are kept idle, lowering their power overhead and reducing $P_{IN,\ MIN}$. In contrast, a non-resonant power receiver [8] employing current-mode charging could not collect power across multiple cycles, limiting η_P at low power levels and $P_{IN,\ MIN}$ (7.8μW); 3) it removes the need for voltage regulation during battery charging. To fully exploit these advantages, a maximum-efficiency tracker is designed to optimize key parameters including the number of resonant cycles (N_{RESO}), bias current of a zero-crossing detector (I_{BIAS}), and frequency of a V_{BAT} detector (F_{DET}) across a range of P_{IN}. Our test chip achieves a $P_{IN,\ MIN}$ of 600nW and η_P of 61.2% at P_{IN} of 2.8μW.

Figure 21.5.2 shows the system diagram of the wireless charger. This method has two modes: resonance (M_{RE}) and charging (M_{CH}). In M_{RE}, an L_{RX} is connected to a parallel capacitor (C_{RX}) and forms an LC tank. By matching this LC tank's resonant frequency with the frequency of the received wave, V_C amplitude increases for Q cycles (where Q is the inductor quality factor). When V_C is 0V and rising, all energy in the LC tank is stored in L_{RX} as $E_L=L_{RX}I_{IND}^2/2$. A zero-crossing detector (ZCD) detects this condition and switches the circuit to M_{CH}, where L_{RX} is disconnected from C_{RX} and connected directly to the battery. As a result, V_C instantly rises to the battery voltage (V_{BAT}) plus $I_{IND}\times R_{SW2}$, and then decreases as E_L is transferred to the battery. When V_C equals V_{BAT}, energy transfer is complete and a V_{BAT} detector switches the circuit back to M_{RE}. The modes are controlled by event-driven asynchronous logic since it consumes no dynamic power during a given configuration. Figure 21.5.3 describes the asynchronous controller driven by outputs of two detectors. The ZCD is a continuous comparator, and the V_{BAT} detector is a dynamic comparator for which the clock toggles only after M_{CH} begins.

Resonating more than 1 cycle improves η_P at low P_{IN}. The two main sources of energy loss are switching loss and conduction loss. If the energy saved in an LC tank for 1 resonant cycle is less than the switching losses of SW_1 and SW_2 (in Fig. 21.5.1), conduction loss of SW_2 , and other control overhead, the system cannot charge a battery after one resonant cycle. A larger N_{RESO}, however, allows the LC tank to build up sufficient energy to overcome these losses, enabling harvesting at the same P_{IN}. An overly high N_{RESO} can decrease η_P, however. This arises since resonant cycles contribute progressively less and less energy to the LC tank, as the conduction losses of SW_1 and the coil ESR grow as I_{IND} rises. In this way a given P_{IN} exhibits a corresponding optimal N_{RESO} that balances the loss from switches and control logic during charging with the conduction losses of the LC tank during M_{RE}.

A maximum efficiency tracker periodically samples the peak voltage of V_C, which is digitized with an 8b ADC (Fig. 21.5.2). Given this information about P_{IN}, an on-chip digital-signal processor (DSP) sets 3 parameters to maximize η_P: N_{RESO}, I_{BIAS}, and F_{DET}. The optimal N_{RESO} across varying P_{IN} levels is measured (Fig. 21.5.4). At P_{IN} = 600nW, the optimal N_{RESO} is 10, and it decreases at higher P_{IN}. This measured result confirms that for low P_{IN}, resonating for multiple cycles helps build up LC tank energy, while for high P_{IN} the large I_{IND} results in high conduction loss in M_{RE}, limiting gain from high N_{RESO}.

The limited bandwidth of the ZCD results in a switching-voltage error, V_{err}. As a result, C_{RX} has $C_{RX}V_{err}^2/2$ energy at the end of M_{RE}, not the ideal 0J. This energy is wasted by charge redistribution in M_{CH} and conduction loss at the next M_{RE}. Increasing I_{BIAS} reduces this loss by improving ZCD bandwidth, but increases its power consumption. With fixed I_{BIAS}, V_{err} increases for high P_{IN}, and thus a higher I_{BIAS} is required for higher P_{IN}. Similarly, a mistimed transition from M_{CH} to M_{RE} leads to energy loss, either by incomplete transfer of E_L to the battery (when switched too early) or by a transfer of battery energy into L_{RX} (when switched too late). Charging time (=$L\times I_{IND}/V_{BAT}$), is shorter for lower P_{IN}, and thus higher F_{DET} for the V_{BAT} detector is required at lower P_{IN}. As the optimal N_{RESO}, I_{BIAS}, and F_{DET} values depend on P_{IN}, the DSP divides P_{IN} into sub-regions and assigns optimal values accordingly.

Another advantage of current-mode charging is the reduced design complexity due to elimination of precise voltage regulation. In voltage-mode charging a mm-sized thin-film battery [9] requires a charging voltage accuracy of ±3.6% from a nominal voltage. Given process-dependent $V_{TH,RECT}$, a DC-DC converter requires wide input range, wide conversion ratio, and input voltage detection. On the contrary, charging current requires no regulation as long as the resulting voltage does not exceed the battery breakdown voltage, reducing charging overhead and enabling low P_{IN} operation.

The system was fabricated in 0.18μm CMOS and includes a Coilcraft 4513TC receiver coil and 1.4nF off-chip capacitor. Measured $P_{IN,\ MIN}$ (600nW) is 3.9× lower than the state-of-the-art work [5] and 13× lower than [8], which uses the same size coil. This sub-μW P_{IN} becomes harvestable when N_{RESO} exceeds 7. Maximum η_P is 61.2% at P_{IN}=2.8μW with N_{RESO}=4. The energy in the LC tank increases with larger N_{RESO}, but is upper-bounded by increasing conduction loss. Switching energy per 1 charging event remains the same regardless of N_{RESO}. However, as ZCD energy consumption increases with growing N_{RESO}, an optimal N_{RESO} arises. With a 20mW transmitter the maximum separation of TX/RX coils is 8.5cm in air. Identical performance is measured through 3cm of bovine tissue and 5.5cm air; this is expected since theoretically tissue absorbs negligible power at 50kHz. This result fits our target application where an implantable system is charged by an external transmitter under the energy exposure limits of human tissue. Oscilloscope waveforms in Fig. 21.5.5 show V_B building up in M_{RE}. V_{err} is captured, as is V_C rising past V_{BAT} to allow charging and then returning back to M_{RE}. This work shows the lowest $P_{IN,\ MIN}$ and maximum of η_P of 61.2% at >11× lower P_{IN} than state-of-the-art works in Fig. 21.5.6. Design area is 0.54mm^2 (Fig. 21.5.7).

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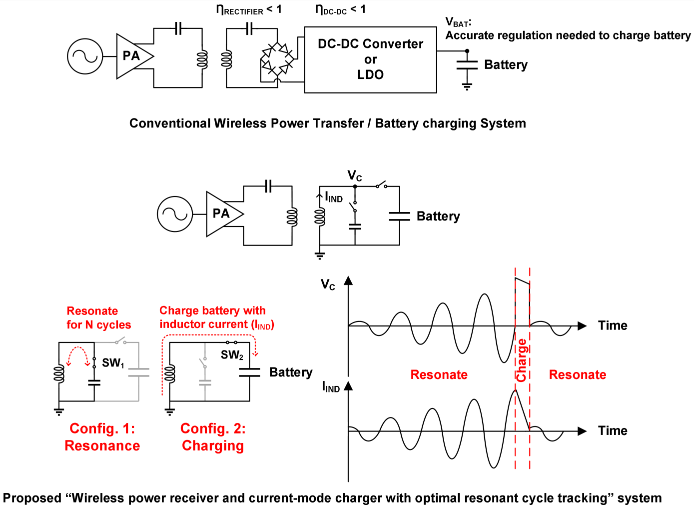

Figure 21.5.1: Conventional wireless power transfer / battery charging system (top) and proposed wireless power receiver and current-mode charger with optimal resonant cycles (bottom).

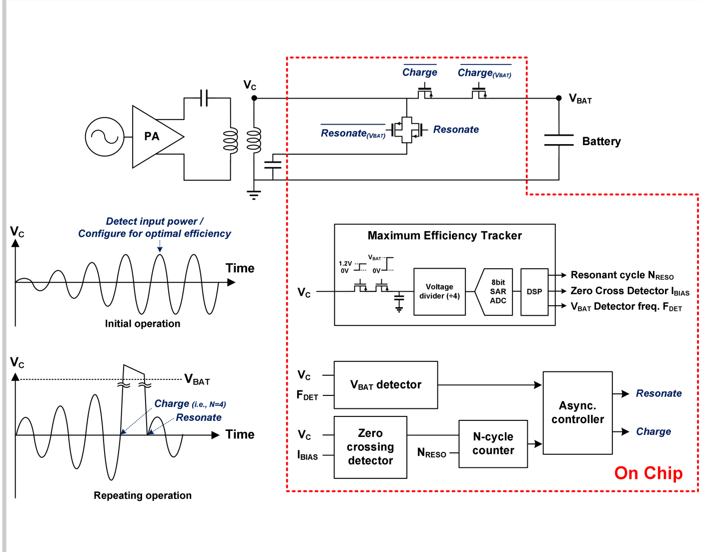

Figure 21.5.2: A system block diagram with operating waveforms.

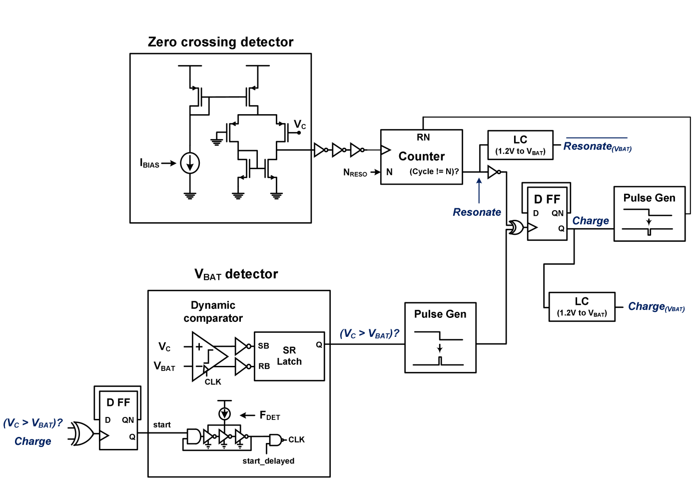

Figure 21.5.3: A detailed circuit diagram of the wireless power receiver controller.

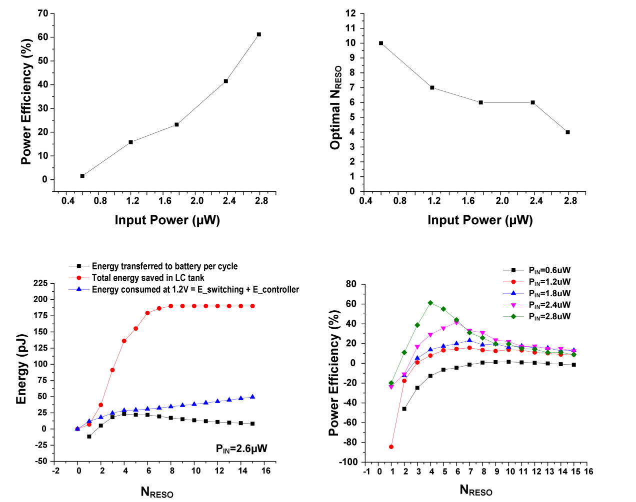

Figure 21.5.4: Measured power efficiency (top, left), optimal number of resonant cycles (top, right), energy transferred per cycle, saved in LC tank, and consumed at 1.2V (bottom, left), and power efficiency (bottom, right).

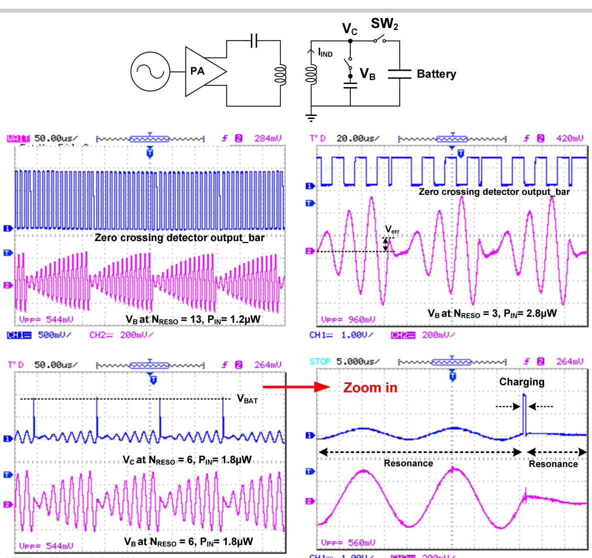

Figure 21.5.5: Waveforms measured by oscilloscope.

	This Work	[5] 2013 VLSIC	[6] 2008 JSSC	[8] 2015 ESTPE	[3] 2012 BCAS	[7] 2015 MTT	[2] 2015 ISSCC	[4] 2015 ISSCC
Technology(μm)	0.18	0.09	0.25	0.18	0.065	Off-chip	0.35	0.13
Chip area(mm^2)	0.544	0.029	0.4	0.26	0.6	N/A	5.415	14.44
Frequency(MHz)	0.05	868	906	0.125	1,860	900 / 1,800 / 2,100 / 2,450	13.56	6.78
Min. Harvestable P_{IN}(μW)	0.6	2.34	5.5	7.8*	200	N/A	N/A	N/A
Max. Receiver Efficiency @ P_{IN}	61.2% @ 2.8μW	31.5% @ 31.6μW	60% @ 158μW	84% @ 660μW	31.9% @ 500μW	84% @ 3.8mW	92.5% @ 59.45mW	84.6% @ 7.09W
Pickup Coil Size	2.6×3.5×11.7mm^3	20.9cm^2	30cm^2	2.6×3.5×11.7mm^3	2mm×2mm	10cm × 10cm	9.5mm diameter	N/A
Coil/Antenna	Coil	Antenna	Antenna	Coil	Antenna	Antenna	Coil	Coil
Measured distance @ TX Power	8.5cm @ 20mW	25 m @ 1.78W	15m @ 4W	7cm @ N/A	5cm @ 2W	50m @ 1.2mW/m^2	1.8cm @ 50mW	6mm @ N/A
Charging method	Resonant current-mode	Voltage-mode	Voltage-mode	Current-mode	Voltage-mode	Voltage-mode	Voltage-mode	Voltage-mode

* Quiescent system power is reported. Min. harvestable P_{IN} is not available.

Figure 21.5.6: Performance summary and comparison table.

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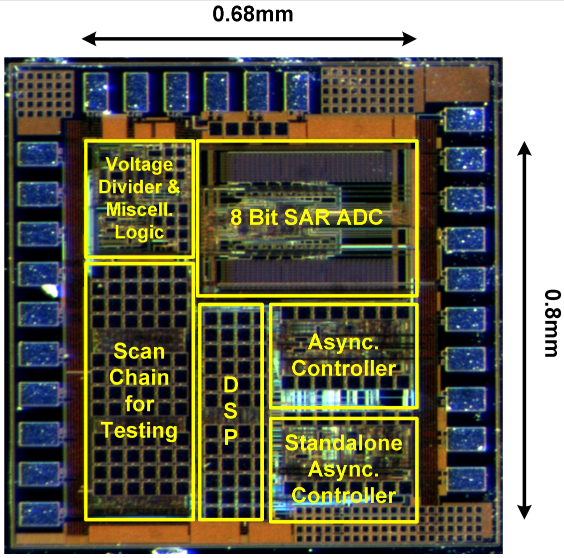

Figure 21.5.7: Micrograph of 0.18µm test chip (0.68mm × 0.8mm).

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