Subthreshold Voltage Reference With Nwell/Psub Diode Leakage Compensation for Low-Power High-Temperature Systems

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***Abstract*— This paper proposes a voltage reference operating up to 170 °C for low-power high-temperature systems. The proposed circuit buffers body voltages to avoid degradation of temperature coefficient from nwell/psub diode leakage. For low power overhead, it measures the diode leakage and adaptively adjusts the bias current of the buffers. This enables low power consumption at low temperature, which can allow an energy harvester to recharge a battery in the target system. Prototype chips, fabricated in a 180 nm CMOS process, show a ±3σ inaccuracy of 3.4% from 0 °C to 170 °C after single trim at 80 °C and a line sensitivity of 0.088 %/V from 1.8 V to 3.6 V. It consumes 76.3 pA at room temperature and 177 nA at 170 °C from 1.8 V.**

Keywords—voltage reference, body leakage, high temperature.

I. Introduction

A miniature sensing system can benefit from high-temperature applications such as oil exploration [1]. Circuits in the system need to maintain their function and performance at > 125 °C. In addition, the circuits should consume low power due to limited battery size and capacity. For example, in advanced miniature sensing system, the battery size, battery capacity, and system standby power are 2.2 mm^2, 2 µAhr, and 8 nW at room temperature, respectively [2]. Moreover, to recharge a battery, total system power consumption has to be less than harvested energy from an energy harvester. For instance, harvested energy using a PV cell in a miniature sensor is less than 1 µA at 10 klux [3]. Typically, an energy source for harvesting is available before a system is deployed or after retrieved at relatively low temperature or during deployment at higher temperature.

A voltage reference is a basic building block present in almost all sensor nodes. Voltage references for high-temperature applications have been proposed using an SOI process, but they consume > 2 µA [4], [5]. Designing a voltage reference that covers high temperature with low power consumption is critical for high-temperature systems. A bandgap reference (BGR) with BJT devices is a typical solution in traditional systems [6]. It shows an excellent output regulation performance, but the power consumption is typically larger than 1 µW. Nano-watt BGRs were recently reported using a switched-capacitor circuit (2 nA) [7] or a subthreshold circuit (29 nA) [8]. However, their operation is limited at < 120 °C. For low power, a CMOS voltage reference is a preferred candidate. Using subthreshold CMOS transistors, voltage references with pW power at room temperature were reported [9]–[12]. The output level is boosted using diode-connected PMOS transistors for easier use, but they cannot cover > 125 °C due to significantly increased diode leakage at high temperature [10], [11].

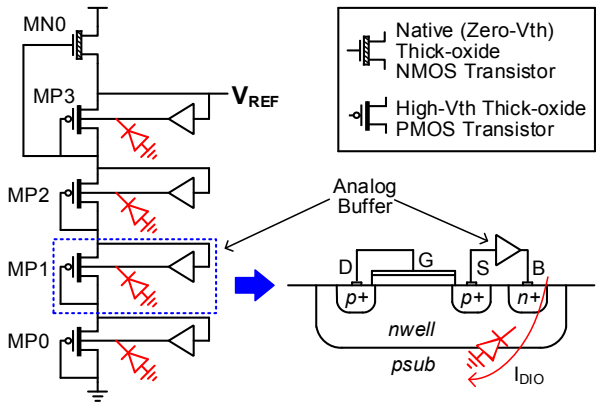

Fig. 1. Simplified diagram of the proposed voltage reference.

In this paper, we propose a CMOS subthreshold voltage reference that maintains its output voltage up to 170 °C. It consumes 76.3 pA at room temperature and 177 nA at 170 °C which is well below the harvestable power in many sensor applications. This circuit isolates nwell/psub diode leakage using analog buffers. This greatly improves the temperature coefficient (TC) by avoiding voltage drop at high temperature. A key challenge is to correctly set the bias current of the buffers which needs to be high enough to compensate for the relatively high diode current at high temperature but small enough to maintain low power at room temperature. To address this, the buffers are biased by measuring the body leakage and mirroring the current to energy-efficiently isolate the body leakage. The voltage reference, fabricated in a 180 nm CMOS process, achieves a ±3σ inaccuracy of 3.4% from 0 °C to 170 °C after trimming at 80 °C.

II. Proposed Voltage Reference

Fig. 1 shows the proposed voltage reference that consists of a main voltage reference and body voltage buffers. The main voltage reference is based on the voltage reference in [11]. It includes a native NMOS transistor (MN0) and 4 high-Vth PMOS transistors (MP0-MP3). The PMOS transistors have gates diode-connected to their drains, and they are connected in series to increase the output voltage (V_{REF}). MN0 has a gate connected to the drain of MP3, and its source is connected to V_{REF}. Since Vgs of MN0 is −0.3V, it operates in the subthreshold

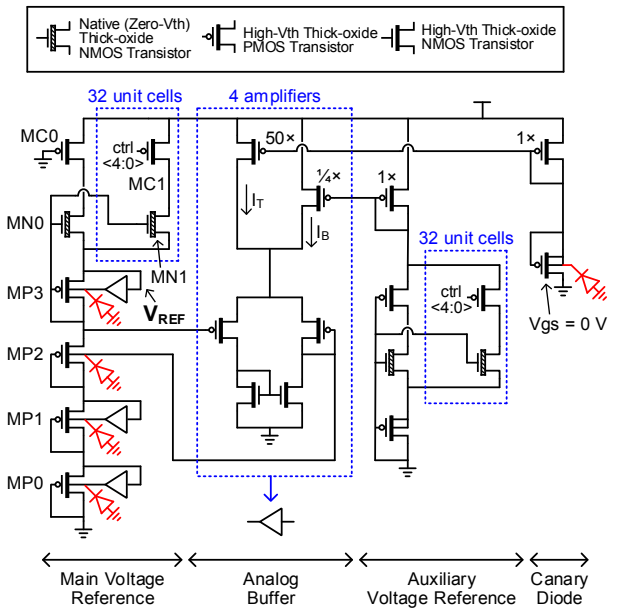

Fig. 2. Detailed circuit diagram with bias circuits.

region, and the drain current can be expressed as follows [13].

$$I_d = \mu C_{OX} \frac{W}{L}(m-1)V_T^2 e^{\left(\frac{V_{gs}-V_{th}}{mV_T}\right)}\left(1-e^{-\frac{V_{ds}}{V_T}}\right). \quad (1)$$

μ is mobility, C_{ox} is oxide capacitance, W and L are transistor size, m is subthreshold slope factor, and V_T is the thermal voltage. The factor '1-exp(-Vds/V_T)' is ignored since it is negligible for Vds > 0.2 V (0.5% error at 170 °C). With negligible nwell/psub diode leakage (I_{DIO} in Fig. 1) at low temperature, V_{REF} can be described as [11]:

$$V_{REF} = 4\left\{\left(\frac{m_1|V_{th2}|-m_2V_{th1}}{m_1+m_2}\right) + \left(\frac{m_1m_2V_T}{m_1+m_2}\right)\ln\left(\frac{\mu_1C_{OX1}\frac{W_1}{L_1}(m_1-1)}{\mu_2C_{OX2}\frac{W_2}{L_2}(m_2-1)}\right)\right\}. \quad (2)$$

W_1 and L_1 are the width and length of MN0. W_2 and L_2 are the MP0-MP3 size. TC can be minimized by properly sizing the transistors [9]. However, nwell/psub diode leakage (I_{DIO}) becomes noticeable at high temperature and worsen TC since current flows through each PMOS transistor Nwell to Psub and the voltage ratio among MP0-MP3 changes across temperatures. Thus, the voltage reference operates only up to 100 °C [10], [11].

Therefore, we proposed a new voltage reference using analog buffers to isolate I_{DIO}. It extends the maximum operating temperature up to 170 °C. Fig. 2 shows the circuit in detail. First, in this design, the size of nwell/psub diodes is minimized by using the minimum length of MP0-MP3 allowed in the given technology. The small device size increases V_{REF} variation from device mismatch. Thus, V_{REF} is trimmed at 80 °C using the segmented top native NMOS transistor (MN1 and MC1).

In addition, the body voltages of MP0-MP3 are buffered using amplifiers. Basic 5-transistor differential amplifiers are used as amplifiers for design simplicity and stable operation. The amplifiers need to support higher diode leakage at higher

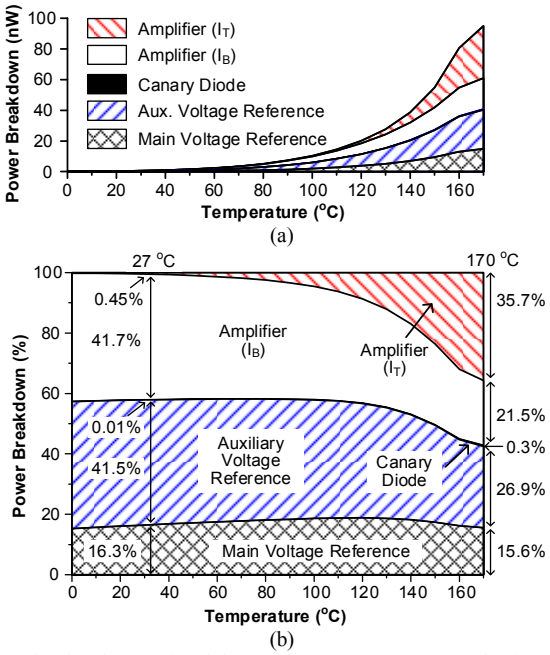

Fig. 3. Simulated power breakdown across temperatures: (a) absolute values (b) percentage.

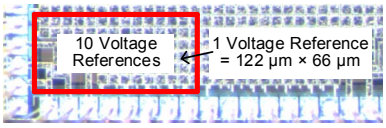

Fig. 4. Die photo.

temperature. To support the leakage, the amplifiers require high tail current at high temperature. To cover 170 °C, the amplifier needs a tail current of 7.9 nA in simulation. If we naively set the tail current of each amplifier to 7.9 nA for the entire temperature range (0 −170 °C), it will dominate the total power consumption at low temperature. For example, the main voltage reference itself consumes 23.7 pA at room temperature (simulation). Four buffers would consume 31.6 nA, and their current consumption would be three orders higher than the main voltage reference itself. This is even higher than the total power in the advanced sensor system [2].

To avoid this unnecessary power overhead, the proposed voltage reference uses an adaptive biasing scheme. It measures the leakage current using a canary PMOS transistor and adds current multiplied by 50 (I_T) to the tail current as shown in Fig. 2. This current adaptively covers increased diode leakage at high temperature and maintains TC.

By using only this bias current, the tail current is extremely small at low temperature. For instance, it is only 320 fA at room temperature. However, if the bias current is too small, the amplifier can malfunction since it can be easily affected by currents ignored and not modeled accurately in the SPICE model (e.g., gate leakage). Thus, a base current is added to the tail current. As shown in Fig. 2, the base current (I_B) is generated from a separate auxiliary voltage reference with only one bottom PMOS transistor. I_B is a quarter of the current consumption of the auxiliary one. Compared with the main voltage reference, the auxiliary reference has a similar structure and thus a similar trend of current consumption across temperatures. However, it

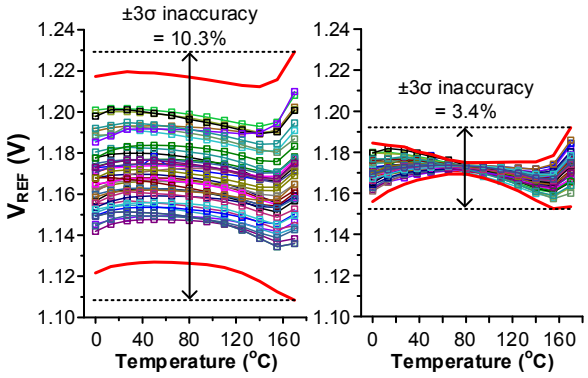

Fig. 5. Measured V_{REF} distribution across temperatures from 40 voltage references: (a) Without trimming (b) After trimming at 80 °C.

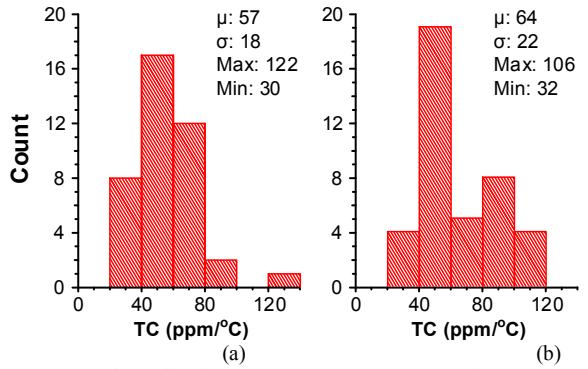

Fig. 6. Measured TC distribution temperatures from 40 voltage references: (a) Without trimming (b) After trimming at 80 °C.

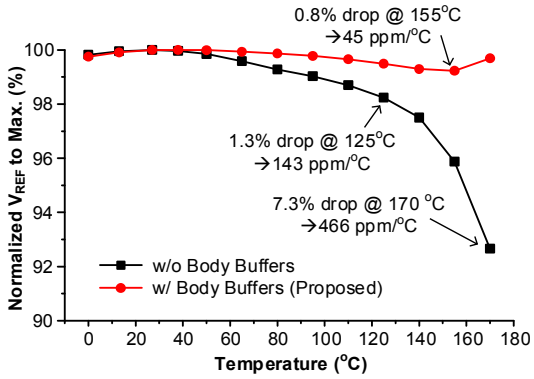

Fig. 7. Measured V_{REF} from voltage references without and with body buffers.

has more headroom due to fewer number of stacked PMOS transistors. Due to the 4:1 current copy ratio, 4 amplifiers consume as much as the auxiliary voltage reference. Fig. 3 shows simulated power breakdown of the proposed voltage reference across temperatures. I_B supplies the current consumption of the amplifier at low temperature while I_T supports additional current required at high temperature.

III. Measurement Results

The proposed voltage reference is fabricated in a 180 nm CMOS process as shown in Fig. 4. The area is 122 μm × 66 μm including a 7.2 pF decoupling capacitor. 20 dies are packaged in ceramic packages. Each chip has 10 voltage references, and they share supply voltage for more accurate power measurement due

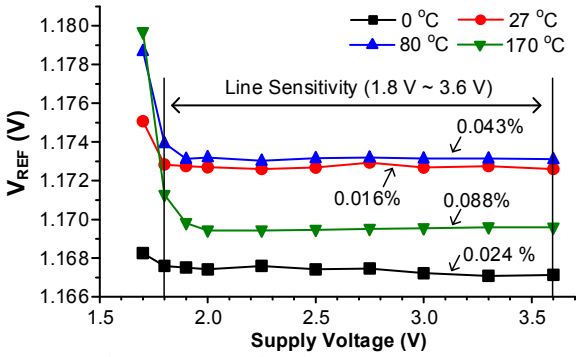

Fig. 8. Measured V_{REF} across supply voltages.

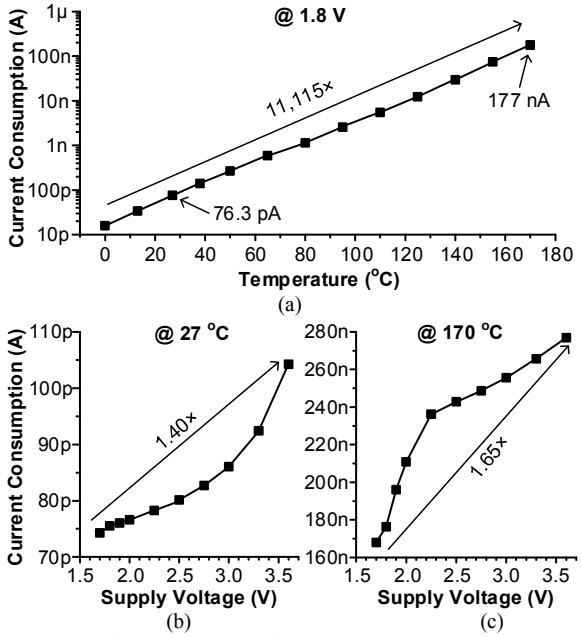

Fig. 9. Measured current consumption: (a) Across temperatures at 1.8 V. (b) Across supply voltages at room temperature. (c) Across supply voltages at 170 °C.

to its low power consumption. However, outputs of only two voltage references are connected to pads for V_{REF} measurement due to limited pad number. Keithley Electrometers with high input impedance are used for V_{REF} voltage and power measurement.

Figs 5 and 6 show the measured V_{REF} and TC distribution. Without trimming, the voltage references achieve a ±3σ inaccuracy of 10.3% from 0 °C to 170 °C and show an average of 57 ppm/°C. For trimming, 10 voltage references are measured at 80 °C with default control bits, and the average V_{REF} is 1.171 V. Next, all the voltage references are trimmed at 80 °C to obtain V_{REF} closest to 1.171 V. They obtain a ±3σ inaccuracy of 3.4% from 0 °C to 170 °C and show an average of 64 ppm/°C . Hence, the trimming reduces the ±3σ inaccuracy by 3.0× at the expense of a 12% TC degradation.

Fig. 7 shows both measured voltage references without and with body buffers. A typical chip is used for the voltage reference without buffers, but the average values from 40 voltage reverences are used for the one with buffers. V_{REF} of the

TABLE I. PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS VOLTAGE REFERENCES.

	This Work	[9]	[10]	[11]	[12]	[4]	[5]	[7]	[8]
Technology (nm)	180	130	180	180	180	130 (SOI)	1000 (SOI)	180	350
Type	CMOS	CMOS	CMOS	CMOS	CMOS	CMOS	CMOS	BJT	BJT
Supply Voltage (V)	1.8 – 3.6	0.5 – 3.0	1.2 – 2.2	1.4 – 3.6	0.15 – 1.8	2.5	5.0	1.5 – 2.5	1.4 – 3.0
V_{REF} (V)	1.17	0.18	0.98	1.25	0.018	1.5	1.8	1.19	1.18
Temp. Range (°C)	0 – 170	-20 – 80	-40 – 85	0 – 100	0 – 120	-40 – 200	-40 – 200	-20 – 100	-10 - 110
±3σ Inaccuracy @ Entire Temp. Range (%)	3.4	N/A	1.9	2.0	N/A	N/A	N/A	N/A	N/A
TC (ppm/°C)	32 – 106 μ:64	17 – 231 μ:62	48 – 124	11 – 73 μ:31	μ:1462 σ: 324	470	825	μ:25	13
Current Consumption @ Room Temp. (A)	76 p	4.4 p	95 p	24 p	174 p	20 μ	2 μ	2.0 n	29 n
Line Sensitivity (%/V)	0.09	0.03	0.38	0.31	0.31	N/A	N/A	2.03	0.20
Power Supply Rejection (dB)	-38 @ 100Hz	-53 @ 100Hz	-42 @ 100Hz	-41 @ 100Hz	-64 @ 100Hz	N/A	N/A	-67 @ 100Hz	-53 @ DC
# Samples	40	49	60	60	60	1	1	10	10
Active Area (mm^2)	0.0081	0.0014	0.0049	0.0025	0.0012	N/A	N/A	0.098	0.48

reference without the body buffers decreases only by 1.3% at 125 °C (TC of 143 ppm/°C). However, it drops by 7.3 % at 170 °C (TC of 466 ppm/°C). On the other hand, V_{REF} of the proposed references with body buffers decreases only by 0.8% at 155 °C (45 ppm/°C) demonstrating the efficacy of the proposed technique isolating body leakage.

Fig. 8 displays V_{REF} across supply voltages from 1.7 V to 3.6 V at 0, 27, 80, and 170 °C. Line sensitivity is 0.088% from 1.8V to 3.6V at 170 °C (worst temperature). The minimum supply voltage can be reduced down to 1.4 V by using NMOS input amplifiers for MP3. In this design, we choose PMOS input amplifiers for all the bodies since it can save one current branch for a current mirror and thus 8.8% current draw from the supply. In addition, the target system runs the designed voltage reference under a battery that has a voltage higher than 2.5 V.

Fig. 9 (a) shows power consumption across temperatures from 0 °C to 170 °C at 1.8 V. Fig. 9 (b) and (c) show power consumption across supply voltages from 1.8 to 3.6 V at room temperature and 170 °C, respectively. Due to subthreshold operation, current consumption significantly increases at high temperature. Low power is considerably important at low temperature since it allows an energy harvester to recharge the battery with limited harvested energy. In addition, typically, there are other dominant contributors to power consumption at high temperature (e.g., 12 μW from 8 MB SRAM memory at 125 °C [14]). Thus, the power consumption of the proposed circuit at high temperature is acceptable.

Table II shows performance summary and comparison with previous voltage references. The proposed voltage reference only can operate at > 120 °C with pA current consumption at room temperature. It also achieves competitive performance in terms of ±3σ inaccuracy, TC, line sensitivity, and power supply rejection.

IV. CONCLUSION

In this paper, we proposed a voltage reference operating from 0 °C to 170 °C for high temperature applications. For low temperature coefficient, this circuit isolates nwell/psub diode leakage using analog buffers. It achieves a ±3σ inaccuracy of 3.4% from 0 °C to 170 °C after one point trimming at 80 °C. For low power, the voltage reference itself is designed in subthreshold region, and the buffers are adaptively biased by measuring the body leakage and using its proportional current. It consumes 76.3 pA at room temperature and 177 nA at 170 °C at 1.8V. Low power consumption at low temperature allows the target miniature sensing system to recharge a battery.

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