A 114-pW PMOS-Only, Trim-Free Voltage Reference with 0.26% within-Wafer Inaccuracy for nW Systems

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Abstract

A sub-nW voltage reference is presented that uses only PMOS transistors, thereby providing inherently low process variation and enabling trim-free operation for LDOs and other applications in nW microsystems. Sixty chips from 3 different wafers in 180nm CMOS are measured, showing an untrimmed within-wafer σ/μ of 0.26% and wafer-to-wafer σ/μ of 1.9%. Measurement results also show a temperature coefficient of 48-124ppm/°C from −40°C to 85°C. Outputting a 0.986V reference voltage, the reference operates down to 1.2V and consumes 114pW at 25°C.

Introduction

Voltage references in LDOs, amplifiers, and ADCs for nW systems such as sensors and IoT devices can tolerate ~ 5% inaccuracy, but they require sub-nW power consumption [1]. Conventional bandgap voltage references achieve excellent uniformity across process variation and temperature, but their complexity leads to μW range power [2], which is unacceptable for emerging nW microsystems. To achieve low power, one approach is to use a V_{th}-based voltage reference with devices biased in the sub-threshold region [3, 4]. However, these sub-nW voltage references make use of native transistors, which are potentially at different corners than normal devices due to distinct doping processes, making them more sensitive to process variations. Also, native transistors are not provided by all fabrication technologies [3] and the output reference voltage is too low if an NMOS diode is used. Combining the native NMOS with stacked PMOS diodes can increase the reference voltage [4], but this further enlarges variation across corners.

For both bandgap references and the aforementioned sub-threshold references, post-fabrication trimming of each chip is required to alleviate the impact of process variations. However, this is a significant expense in cost-sensitive designs because of area overhead and testing complexity. In addition, non-volatile memory such as one-time-programmable (OTP) memory is required to store the trimming configuration information [3], requiring extra fabrication masks at increased cost. This paper proposes an ultra-low power PMOS-only voltage reference. By using only PMOS transistors, the reference has inherently low process variation. The untrimmed within-wafer σ/μ is 0.26%, and the untrimmed wafer-to-wafer σ/μ of 1.9%, which is sufficient for many applications in nW systems. With a 0.986V output reference voltage, the design can function down to 1.2V and consumes only 114pW.

Trim-free Voltage Reference Design

Fig.1 shows a simplified structure of the proposed trim-free voltage reference using only 4 PMOS devices (M1-M4). M1 is forward-biased and provides sub-threshold current flowing through the bottom PMOS diode M2. The current equations of M1 and M2 are expressed as in (1). By solving (1), V_{ref} can be expressed as (3). As M1 and M2 are the same type of PMOS, the difference between V_{th1} and V_{th2} comes solely from the body bias effect of M1. Random V_{th} mismatch is kept negligible by upsizing (> 20 μm^2) of all 4 devices in this reference.

$$I_R = u_p C_{ox} \frac{W_1}{L_1} nV_T^2 \, exp\left(\frac{0-V_{th1}}{mV_T}\right) = u_p C_{ox} \frac{W_2}{L_2} nV_T^2 \, exp\left(\frac{0-V_{ref}-V_{th2}}{mV_T}\right) \quad (1)$$

$$I_L = u_p C_{ox} \frac{W_3}{L_3} nV_T^2 \, exp\left(\frac{V_{body}-V_{dd}-V_{th3}}{mV_T}\right) = u_p C_{ox} \frac{W_4}{L_4} nV_T^2 \, exp\left(\frac{0-V_{th4}}{mV_T}\right) \quad (2)$$

$$V_{ref} = V_{th1} - V_{th2} + mV_T \, ln\frac{W_1 L_2}{W_2 L_1} \quad (3)$$

$$= \gamma\left(\sqrt{2\phi_b - mV_T \, ln\frac{W_4 L_3}{W_3 L_4}} - \sqrt{2\phi_b}\right) + mV_T \, ln\frac{W_1 L_2}{W_2 L_1} \quad (4)$$

M3 and M4 generate the required body bias for M1. M4 is an off-state PMOS and M3 is a PMOS diode. The current equations of M3 and M4 are expressed in (2). As M3 and M4 are also the same type of PMOS, V_{th3} and V_{th4} are essentially identical. The combination of M3 and M4 provides a body-bias voltage V_{body} that tracks V_{dd} and creates a constant V_{BS} (V_{body}-V_{dd}) for M1, as shown in Fig. 2. If the current through M3 (I_L) is much larger than the parasitic diode current (I_{dio}) from the source to the N-well of M1, V_{ref} can be expressed by (4). The left term of Equation (4) is complementary to temperature, whereas the right term is proportional to temperature (Fig. 1). With proper sizing of the four transistors, the first-order temperature dependency can be cancelled out. Moreover, V_{th} does not play a role in Equation (4) because each pair (M1/M2 and M3/M4) uses the same type of PMOS, thus significantly reducing process variation. Since I_{dio} is not well modeled, we designed I_L to be 3 orders of magnitude larger than I_{dio} to minimize the effect of I_{dio}. Proper sizing of these transistors can be determined using a global optimization tool.

As shown in Fig. 3, stacked PMOS diodes can replace M2 and M3 to generate a higher reference voltage, and multiple voltage levels can be generated in this manner. Three stages of PMOS diodes are used in our design to realize an approximately 1V output reference voltage. MIM capacitors C0 and C1 (both set to 1.78pF) are used to isolate the reference voltage from high-frequency power supply noise.

Fig. 4 compares simulated reference voltage distributions across corners for the proposed design as well as designs from [3] and [4]. The proposed design achieves < 4% inaccuracy across all corners, whereas [3] and [4] vary up to 10% and 19%, respectively.

Measurement Results

Sixty chips from 3 different wafers in 180 nm CMOS were tested. One wafer was in a typical corner with thin top-metal, another was found to be at a slow corner with ultra-thick top-metal, and the third was at a fast corner with ultra-thick top-metal. All measurements are reported without trimming.

Fig. 5 shows the measured reference voltage across temperature for all 60 chips. From −40°C to 85°C, the temperature coefficient of the typical wafer ranges from 48ppm/°C to 104ppm/°C, and those of the fast and slow wafers are 55.2−124ppm/°C and 56.1−117ppm/°C, respectively. The reference voltage distributions at 25°C of the 3 different wafers are shown in Fig. 6. Without trimming, the typical wafer shows a mean value of 986.2mV and standard deviation of 2.6mV. The average voltage difference between the fast and slow wafers is 3.6% (1.9% σ/μ), matching simulation and providing sufficient accuracy for many key circuit applications within nW systems.

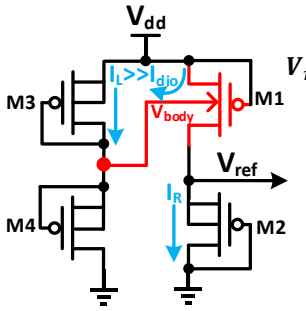
Fig. 7 shows the measured sensitivity of reference voltage to power supply voltage. Line sensitivity is 0.38%/V from 1.2V to 2.2V. Fig. 8 shows the measured temperature coefficients at different supply voltages. Fig. 9 shows the measured power supply rejection ratio (PSRR) from 10Hz to 10MHz. High-frequency PSRR is −56dB, which can be further improved with larger loading caps C0 and C1.

Fig. 10 shows the measured power consumption across supply voltage and temperature. The output reference voltage is approximately 1V with 3 stages of stacked PMOS diodes. The power supply can be reduced to 1.2V while maintaining this approximately 1V reference voltage. To lower the minimum power supply, fewer stages of PMOS diodes can be used, but the output reference voltage will be lowered as well. At 25°C and 1.2V, the power consumption is 114pW, which is suitable for low-power sensor and IoT applications.

Fig. 11 shows the die photo; the proposed voltage reference occupies an area of 4880μm^2 (80μm x 61μm) with this area dominated by the two MIM capacitors, C0 and C1. Table I summarizes the results of the proposed sub-nW trim-free voltage reference and compares them with previous works.

References

[1] T. Jang et al., ESSCIRC, 2015.
[2] G. Ge et al., JSSC, 2011.
[3] M. Seok et al., JSSC, 2012.
[4] I. Lee et al., VLSI, 2014.
[5] A. Shrivastava et al., ISSCC, 2015.
[6] Y. Osaki et al., JSSC, 2013.
[7] V. Ivanov et al, JSSC, 2012.



$$V_{ref} = V_{th1} - V_{th2} + mV_T \ln\frac{W_1L_2}{W_2L_1}$$

$$= \gamma\Big(\sqrt{2\phi_b - mV_T \ln\frac{W_4L_3}{W_3L_4}} - \sqrt{2\phi_b}\Big) + mV_T \ln\frac{W_1L_2}{W_2L_1}$$

Complementary to T | Proportional to T

V_{ref} is independent of V_{th} (corner compensated)

Fig.1 Simplified circuit of proposed voltage reference generator and its equations.

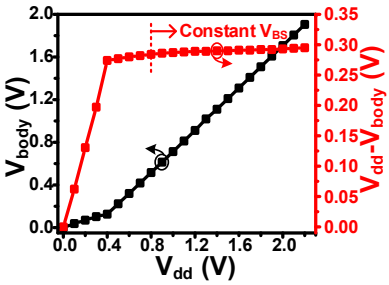


Fig.2 V_{body} tracks V_{dd} change and creates constant V_{BS} for M1.

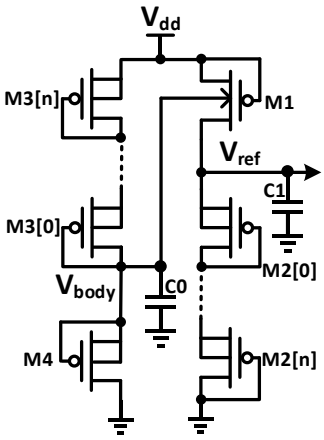


Fig.3 Proposed voltage reference generator with stacked PMOS diodes.

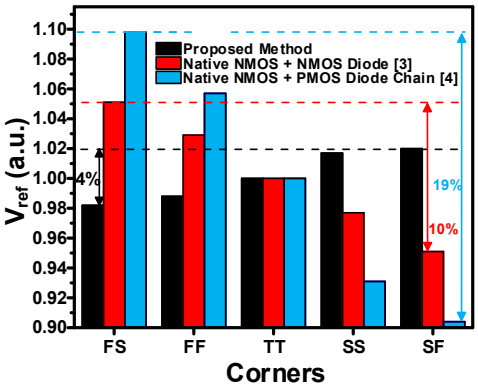


Fig.4 Comparison of V_{ref} simulation at all corners among the proposed design, [3], and [4].

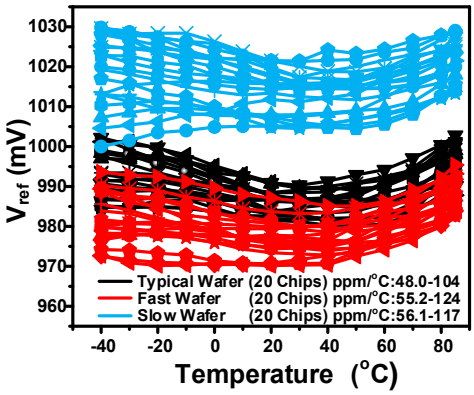


Fig.5 Measured V_{ref} across temperature for 3 wafers in 3 different corners.

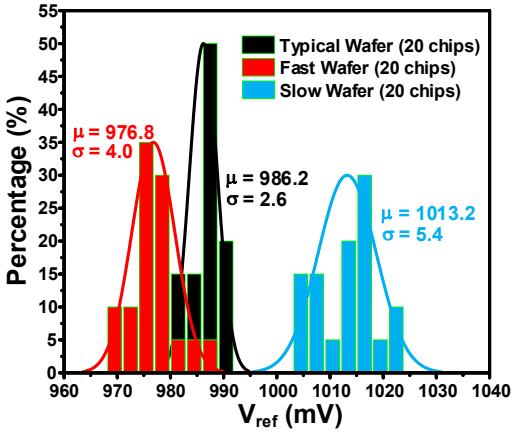


Fig.6 Distribution of V_{ref} on 3 different wafers.

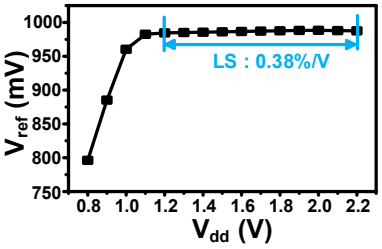


Fig.7 Measured line sensitivity.

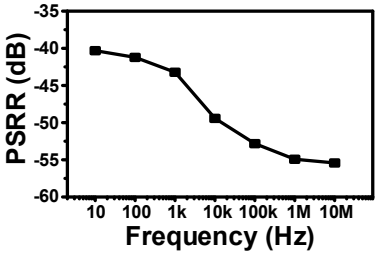


Fig.9 Measured PSRR.

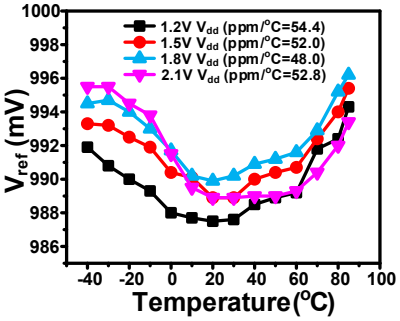


Fig.8 Measured temperature coefficients at different V_{dd}.

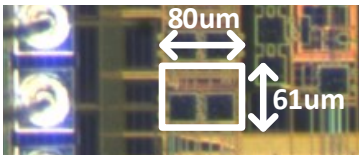


Fig.11 Die Photo in 180 nm CMOS.

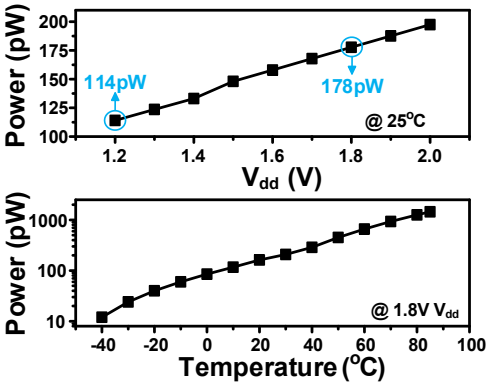


Fig.10 Measured power across V_{dd} and temperature.

Table 1. Comparison table to related works.

Parameters	This Work	[3]	[5]	[6]	[7]	[2]
Process (nm)	180	180	130	180	130	160
Power (nw)	0.114	0.006	32	52.5	170	99000
Min. V_{dd} (V)	1.2	0.5	0.5	0.7	0.75	1.62
V_{ref} (V)	0.9862	0.3268	0.498	0.548	0.256	1.0875
Within-Wafer Untrimmed σ/μ (%)	0.26	0.8	0.67	1.05	1	0.5
Wafer-to-Wafer Untrimmed σ/μ (%)	1.9 (3 wafers)	NA	NA	NA	NA	~0.3 (2 wafers)
Temp. Range (°C)	-40 ~ 85	-20 ~ 80	0 ~ 80	-40 ~ 120	-20 ~ 85	-40 ~ 125
TC (ppm/°C)	48.0 ~ 124	54.1 ~ 176.4	75	114	40	5 ~ 12
LS (%/V)	0.38	0.044	2	NA	0.35	NA
PSRR (dB)	-42/-56 (100Hz/10MHz)	-49/-55 (100Hz/10MHz)	-40	-56 (100Hz)	-93	-76 (DC)
Area (um^2)	4880	1425	26400	24600	70000	120000
Type	Vth	Vth	Bandgap	Bandgap	Bandgap	Bandgap
Chips Measured	60 chips in 3 wafers	14 chips	6 chips	9 chips	NA	61 chips in 2 wafers