

An Oscillator Collapse-Based Comparator with Application in a 74.1dB SNDR, 20KS/s 15b SAR ADC

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Abstract

This paper presents a new energy-efficient ring oscillator collapse-based comparator, which is demonstrated in a 15-bit SAR ADC. The comparator automatically adjusts comparison energy according to its input difference without any control, eliminating unnecessary energy spent on coarse comparisons. The employed SAR ADC supplements a 10-bit differential main CDAC with a 5-bit common-mode CDAC. This offers an additional 5 bits of resolution with common mode to differential gain tuning that improves linearity by reducing the effect of switch parasitic capacitance. A test chip fabricated in 40nm CMOS shows 74.12 dB SNDR and 173.4 dB FOMs. The comparator consumes 104 nW with the full ADC consuming 1.17 μ W.

Introduction

An energy-efficient comparator that automatically scales its conversion energy based on the input signal difference is useful for many applications, including voltage regulator, brown-out detection and analog to digital conversion (ADC). A low-noise comparator is especially important in SAR ADCs. SAR ADCs have enabled energy-efficient data conversion for moderate resolution (<12b). However, at higher resolution (≥ 12 b) their energy efficiency tends to be poor relative to pipeline or sigma-delta ADCs, due to the low noise requirement on the comparator, which wastes comparator energy on those cycles that require only coarse comparison. Hence a comparator that automatically adjusts its energy consumption to the noise requirement would be ideal for SAR ADC and would enable higher resolution SAR ADC with high energy efficiency. To address this need, a dual comparator structure that uses a coarse comparator for MSB bits [1], oversampling and selective majority voting for noise-critical bits [2] and a time-domain comparator with long digital preamplifier stages [3] were proposed. However, these structures impair the simplicity of the SAR structure, worsening design and control complexity. This paper proposes a ring oscillator collapse-based comparator, referred to as an *edge-pursuit comparator* (EPC), which automatically scales comparison energy according to its input difference without external control, tailoring comparison energy to each conversion. This work also proposes a fine-grain 5-bit CDAC with common mode to differential gain tuning to improve linearity.

Proposed Edge-Pursuit Comparator

Fig. 1 shows the structure and operating principle of the EPC, which is composed of two NAND gates and eight inverter delay cells (Fig. 1a). The comparator initiates a comparison when the signal *START* goes high simultaneously at both NAND gates. This injects two propagating edges into the oscillator, which travel around the comparator until one overtakes the other, collapsing the oscillation. Differential input signals (V_{INP} , V_{INM}) are applied to both the top and bottom

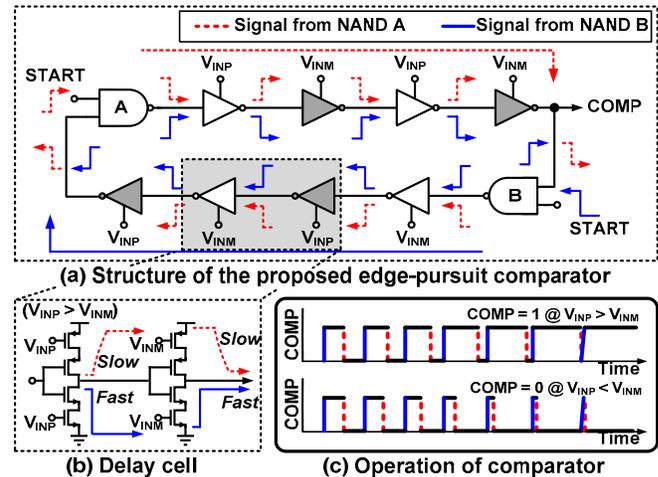


Fig. 1. Proposed edge-pursuit comparator

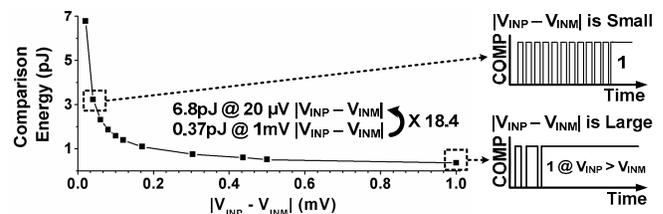


Fig. 2. Simulation results of the edge-pursuit comparator

current-limiting transistors of the delay cells, modulating the pull-up and pull-down edge-propagation delays (Fig. 1b). Propagation delay of these two edges is controlled by mutually exclusive current-limiting transistors such that increasing V_{INP} causes one edge to propagate faster and the other to become slower (and vice versa for V_{INM}). After one propagating edge overtakes the other edge, the oscillation collapses and the stage outputs settle to either V_{DD} or GND , dictated by which edge was slower and overtaken (Fig. 1c). Comparator output *COMP* is sampled from an internal stage that becomes one when $V_{INP} > V_{INM}$ and zero otherwise. When the voltage difference between V_{INM} and V_{INP} is small, the two injected edges have similar propagation delay and the number of cycles required to make a decision automatically becomes longer (Fig. 2). This filters out high frequency noise, as the design performs noise averaging over a long time. On the other hand, if the voltage difference is large, the oscillation inherently collapses quickly, limiting dynamic energy consumption for coarse comparison.

In this manner, the comparator inherently adjusts its energy consumption without any external control (by 18.4 \times for 20 μ V to 1mV input voltage difference, Fig. 2) and realizes both high accuracy and low power operation. Also, EPC performance at the same input voltage difference can be easily controlled by changing the supply voltage, MOSFET size in the delay cell, and the number of delay cells.

Proposed CDAC Structure

The proposed EPC was applied to a 15-bit SAR ADC, which

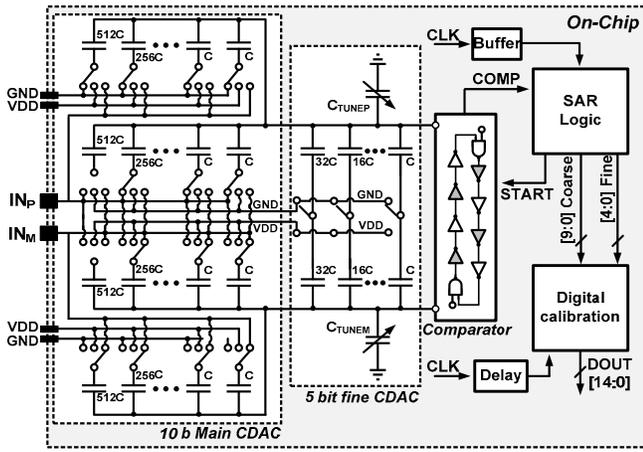


Fig. 3. Overall architecture of the SAR ADC.

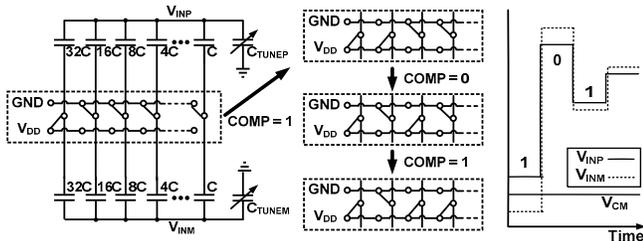


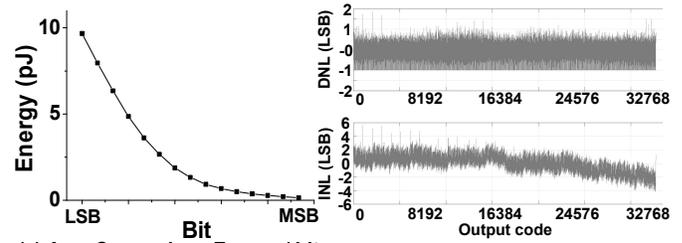
Fig. 4. Operation of the proposed 5-bit fine CDAC

consists of a main and fine CDAC, the EPC, logic, and a digital calibration block (Fig. 3). The 10-bit differential CDAC is implemented using a split capacitor array to reduce switching power. The proposed 5-bit fine CDAC shares top plates with the CDAC (V_{INP} , V_{INM}) and has the same unit capacitor size as the main CDAC. Intentional difference between tuning capacitors C_{TUNEP} and C_{TUNEM} induces a small differential voltage change as shared bottom plates of the fine CDAC change, allowing high resolution without significantly increasing overall CDAC capacitance.

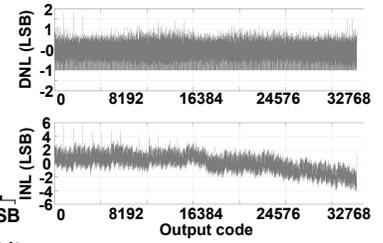
Differing from a conventional bridge technique [4], the proposed 5-bit fine CDAC has shared bottom plates of each pair of capacitors (Fig. 4, left). When a capacitor is switched, it injects the same charge into both CDAC output nodes. Hence, switching a capacitor only shifts the common mode voltage of the two output nodes and does not impact the SAR. However, by creating a small imbalance between the total capacitance to ground of the two CDAC output nodes, this common mode shift will also translate into a small differential voltage difference (Fig. 4, right). This common mode to differential gain is fine-tuned using the two tuning capacitors C_{TUNEP} and C_{TUNEM} . Because the tuning capacitors are connected to the shared top plate nodes, voltage across the tuning capacitors always stays near the input common-mode voltage whenever fine comparison is performed and changes only by a small amount during fine decision. This voltage swing is $\sim 32\times$ smaller than in the bridge capacitor scheme. Hence, the proposed top-plate shared fine CDAC structure shows improved linearity over the bridge technique by reducing non-linearity introduced by the non-linear parasitic capacitance of switches controlling C_{TUNEP} and C_{TUNEM} .

Measurement Results

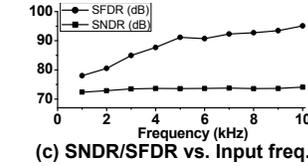
The ADC with proposed edge-pursuit comparator is fabricated in 40nm CMOS process with a total area of 0.315 mm². Measured SFDR/SNDR at the Nyquist frequency is



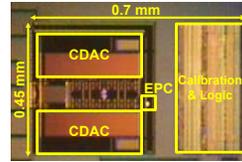
(a) Avg. Comparison Energy / bit



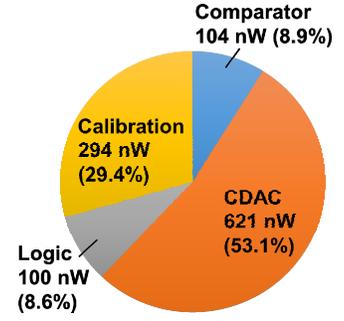
(b) INL/DNL



(c) SNDR/SFDR vs. Input freq.



(d) Die Photo



(e) Power Break Down of the ADC

Fig. 5. Measured results and die photo

Table 1. Comparison table with relevant ADCs.

	This work	Tai, ISSCC 2014 [1]	Harpe, ISSCC 2014 [2]	Lee, JSSC 2011 [3]	Lim, ISSCC 2015 [5]	Bannon, VLSIC 2014 [6]
Technology	40 nm	40 nm	65 nm	180 nm	65 nm	180 nm
Architecture	SAR	SAR	SAR	SAR	Pipelined-SAR	Pipelined-SAR
Resolution (bits)	15	10	12, 14	10	13	18
Sampling rate, F_s (kS/s)	20	200	32	100	50000	5000
Input voltage range (Differential)	$1.8 V_{pk-pk}$	Not reported	Not reported	$1.2 V_{pk-pk}$	$2.4 V_{pk-pk}$	$10 V_{pk-pk}$
Area (mm ²)	0.315	0.0065*	0.18	0.125	0.0544*	5.74
SFDR	95.1	76.25	78.4	67	84.6	Not reported
SNDR	74.12	55.63	67.8	69.7	57.7	98.6
ENOB (SNDR-1.76)/6.02	12.02	8.95	10.97	11.29	9.3	11.5
INL _{max} (LSB)	5.5	0.45	0.82	3.50	0.8	0.96
DNL _{max} (LSB)	1.9	0.44	0.58	1.75	0.4	0.58
Total Power (μ W)	1.17	0.084	0.310	0.352	1.3	1000
Critical Power** (μ W)	0.104	0.025***	0.124***	0.141***	0.130***	336***
FOMs (dB)	173.4	176.8	174.9	176.3	163.6	174.9
FOM _C (dB)****	184	181.6	178.9	180.2	173.6	179.7

* Active area ** Power for noise critical block (comparator in SAR, amplifier in pipelined SAR) *** Calculated value from the paper/presentation material **** SNDR+10log($F_s/2$ /Critical power)

95.1/74.12 dB. The measured total power consumption is 1.17 μ W and max DNL/INL are 1.9/5.5 LSB.

Fig. 5a shows the measured EPC comparison energy. Comparator energy is intrinsically adjusted as each bit comparison progresses. Comparator power is 104 nW, representing only 8.9% of the total ADC power consumption (Fig. 5e). FOM calculated using total power consumption of the ADC is 173.4 dB, however FOM_C, calculated based on comparator power only, is 184 dB, which compares favorably to other similar designs (Table 1). This underscores the applicability of the EPC to other low-power SAR ADC topologies.

Acknowledgements

The authors thank TSMC University Shuttle Program for chip fabrication and Analog Devices for partial financial support.

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