A 346µm^2 Reference-Free Sensor Interface for Highly Constrained Microsystems in 28nm CMOS

Laura Freyman, David Fick, David Blaauw, Dennis Sylvester
Department of Electrical Engineering and Computer Science
University of Michigan, Ann Arbor, MI 48109
{lfreyman, dfick, blaauw, dmcs}@umich.edu

Massimo Alioto
Information Engineering Department
University of Siena, 53100 Siena, Italy
malioto@dii.unisi.it

***Abstract*— A 346µm^2 reference-free, asynchronous VCO-based sensor interface circuit is demonstrated in 28nm LP CMOS. This design does not require high accuracy current sources, voltage sources, or low jitter timing references. It achieves wide resolution and voltage scalability, and consumes only ~1/100th the area of prior approaches. Resolution can be scaled from 2.8 to 11.7 bits and V_{DD} from 500mV to 1.0V.**

I. Introduction

Energy and area constrained wireless sensor nodes demand small flexible designs for interfacing with multiple sensors, and IP blocks that are reusable across SoC platforms. Traditional ADCs achieve high resolution and energy efficiency through charge transfer topologies, which require high performance off-chip references (or high accuracy supplies which function as references). Systems with only slowly-varying sensors (*e.g.*, temperature, pressure, strain) can avoid the complexity of traditional ADC topologies for digitizing output values. We propose a simple design that eliminates the need for high accuracy current sources, voltage sources, and low jitter timing references, and allows for significant size reduction (~10-100×).

High accuracy references are not available and not feasible in wireless sensor nodes. Systems such as those presented in [1] (Fig. 1) do not use crystal oscillators for precise timing references, and do not have the space or power budget to include highly accurate voltage or current sources. Off-chip references are also unreasonable as the die stack is too small for interfacing, and the references would need to be power gated, adding latency and energy consumption.

An additional benefit of the proposed approach is dynamic resolution scalability, which can yield significant energy and area savings. For example, in a microsystem containing a 5b battery sensor, 7b temperature sensor, and 9b strain sensor, a scalable resolution interface can reduce energy by 61% over using a fixed 9-bit interface for all sensors (Fig. 2). It also removes the need for multiple, specialized ADCs [2], reducing system energy and design cost. Resolution scalability can also be used in wakeup schemes, common in wireless sensing applications, where the system runs at low resolution for long periods of time and increases to higher accuracy settings when key events are identified in the coarse output data.

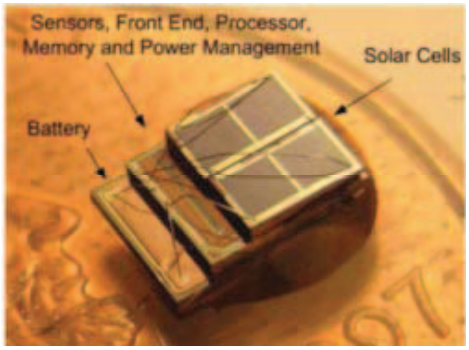

Fig. 1: Target application. Millimeter-sized wireless sensor nodes cannot support high accuracy references. [1]

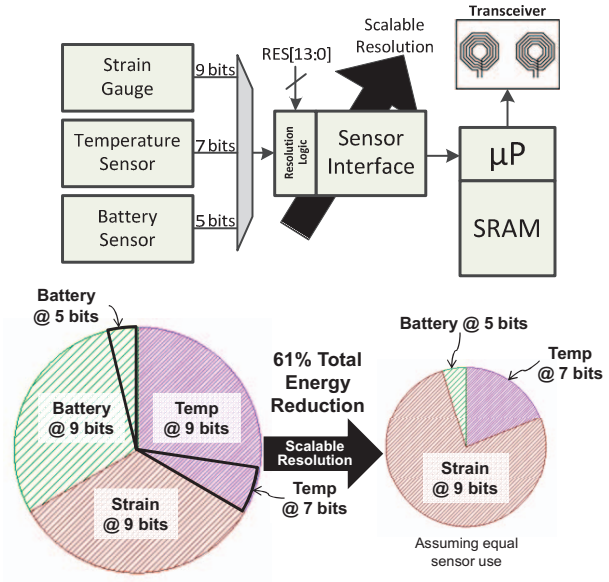

Fig. 2: Multiple sensor application. Energy scalability can be applied to multi-sensor applications, adjusting resolution (and energy) based on application specific requirements.

VCO-based ADC designs are common, but do not address the issues inherent in wireless sensing applications. A previous implementation [3] achieves very low energy (150fJ/conv-step), while still requiring a low jitter clock, digital post-correction, and large area (0.02mm^2; 10× area with ideal scaling versus the proposed design). Other designs [4,5] implement low energy, resolution scalable SARs that require high accuracy current sources and low jitter timing references, both of which are not feasible in millimeter-scale wireless sensing applications. Additionally, these SAR-based ADCs require ~100× larger area (ideal scaling) than the proposed approach. The proposed design trades off accuracy (post-correction) for a reference-free design, extremely low area, scalable resolution, and wide voltage range operation.

This paper presents a 346µm^2 VCO-based sensor interface circuit in 28nm CMOS. The topology is mostly digital and

978-1-4799-0280-4/13/$31.00 ©2013 IEEE

technology portable, unlike SAR and ΔΣ ADCs. Area scales well with maximum resolution, increasing by only two FF standard cells per bit, as opposed to exponentially larger capacitors.

II. Circuit Description

Fig. 3 shows a block diagram of the sensor interface. The system first converts input voltage V_{IN} to the frequency domain, and then digitizes the signal through a time to digital converter. The circuit consists of two current-starved VCOs and two pre-loadable ripple counters. The two VCOs have opposite frequency relationships with V_{IN}, shown in Fig. 4; the PMOS-starved VCO (PSV) slows with increasing V_{IN} and the NMOS-starved VCO (NSV) speeds up. After the counters are pre-loaded and enabled, digitization ends when the counter associated with the faster oscillator reaches full count (*i.e.*, when its MSB transitions). At this point, the 'Done' signal is set to '1' and the 'Winner' bit identifies which oscillator reached full count first (1: PSV, 0: NSV). The FSM then stops all oscillations and captures the value stored on the slower counter (non-full count). The Winner bit and the non-full counter value comprise the output code.

Dynamically adjustable, scalable resolution is readily achieved through the pre-loadable ripple counters. Resolution is directly controlled by the maximum counter value, which can be reduced by pre-loading a '1' into higher order bits, thereby deactivating them as shown in Fig. 5. Resolution scales linearly between 2.8 and 11.7 bits with 11 pre-loadable counter bits, with each extra bit adding two flip-flops. Low resolution applications can achieve extremely small footprints by limiting the number of counter bits.

The two oscillator frequencies become equal at the 'crossover point'. The VCOs are sized such that this crossover point nominally occurs when $V_{IN} = V_{DD}/2$ in order to increase the linearity of the output code. As shown in Fig. 4, this strategy aligns the linear regions of the two VCOs and largely cancels the remaining non-linearities.

The crossover point can be single-step calibrated to correct for VCO variation, as shown by the algorithm in Fig 5. For this technique, V_{IN} is set to $V_{DD}/2$ and the converter is run until completion. The difference remaining between the two counters is loaded back onto the slower counter as its offset in subsequent conversions. This value needs to be measured only once at the maximum resolution since it can be shifted for lower resolutions and does not significantly vary with V_{DD} or temperature (1 count difference across 0-80C at 1V V_{DD} TT). Measured and calculated offset values versus voltage and resolution are shown in Fig. 7. At a measured resolution of 10 active counter bits, the calibration offset average at 0.8V is 209 counts, and varies by up to 16 counts (8mV input voltage) when V_{DD} is changed to either 1.0V or 0.6V. This calibration value can also be scaled with resolution setting. As resolution is reduced by one bit, the calibration setting is divided by 2 since eliminating one FF reduces measurement time by half. Calibration measurements show that this estimation is accurate for each resolution setting at 0.8V, and that V_{DD} offset error reduces with decreasing resolution, resulting in a maximum error of only 1 count (4mV input voltage) at 7b resolution.

Linearity is further improved through the use of degenerated common source amplifiers, which generate the VCO bias voltages (Fig. 3 at top). These amplifiers do not need high accuracy current sources or bias voltages, and take only the sensor output voltage as an input. The goal of these amplifiers

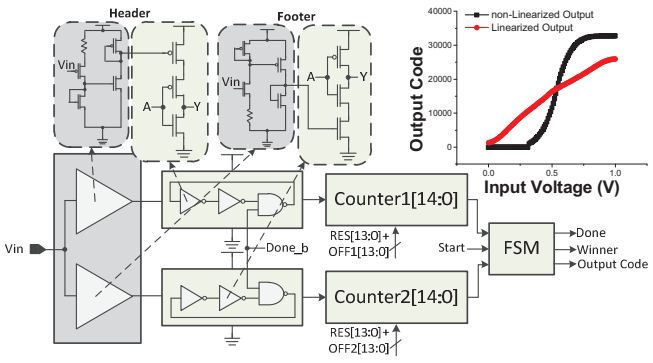

Fig. 3: Sensor interface block diagram and output codes. The sensor output is taken in as the input voltage (V_{IN}) and digitized into the above output code, which is linearized using simple degenerated amplifiers.

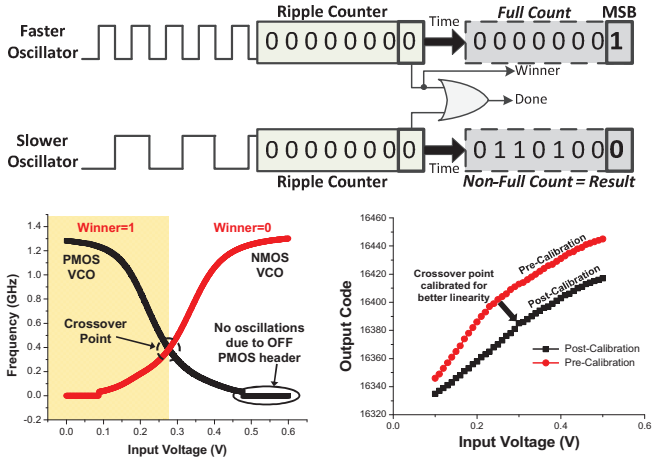

Fig. 4: Sample FSM operation crossover point calibration. (Top) FSM to monitor MSB transitioning (Bottom Left) PSV and NSV frequency vs input voltage (Bottom Right) Crossover point calibration.

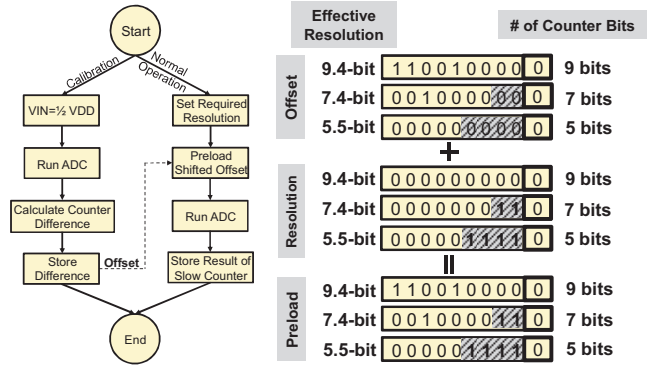

Fig. 5: Calibration flow and preload calculation example. (Left) Calibration flow chart (Right) Preload calculation

is to bias each oscillator in its highly linear range of operation for a wider range of input voltages. As shown in Fig. 3, without linearizing amplifiers, the usable input voltage range is between 0.3V and 0.6V, and is highly non-linear. With the additional amplifiers, the usable voltage range increases to full V_{DD}, and a more linear range exists between 0.1V and 0.9V.

For high-accuracy measurements, linearity can be further improved through post-processing of the data through a small look-up table, which is common in sensor node applications [6]. This correction is done off-chip, after data collection from the sensor nodes is complete. In low-resolution applications such as wakeup monitors, post-processing is not needed.

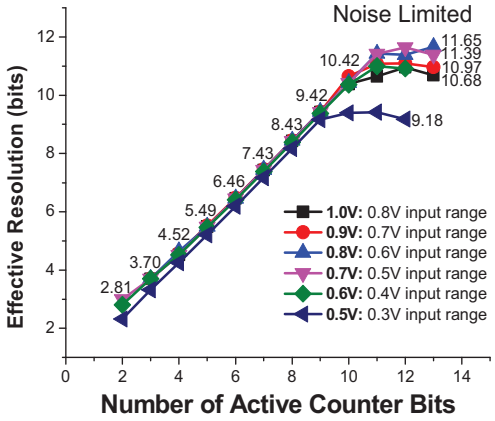

Fig. 6: Effective resolution versus the present resolution value (number of active counter bits). Resolution scales linearly with the number of active counter bits and is not impacted by voltage scaling until V_{DD} = 0.5V (near-threshold).

Comprised mostly of digital components, this circuit can be implemented as a compact, reusable IP block for a wide array of sensor applications. Resolution and calibration values are stable between 0.6V and 1.0V V_{DD}, allowing for use in a wide range of voltage domains with no additional design effort. Scalable resolution values allow for energy efficient use between a variety of sensors and applications, enabling small area and energy consumption. Reduced design constraints eliminate the need for high accuracy, high power off-chip components that are unavailable in wireless sensor node applications.

III. Measurements and Results

The proposed interface circuit was implemented in a 28nm LP bulk CMOS process. Effective resolution, measured as $\log_2 \frac{V_{input\_range}}{RMS\ Noise}$, scales linearly from 2.8 to a noise-limited 11.7 bits over a power supply range of 0.6V-1.0V (Fig. 6). At 0.5V V_{DD} (representing near-threshold operation in this LP process), the noise-limited maximum resolution decreases to 9.2 bits. Each additional active counter bit contributes nearly 1 additional bit of effective resolution. The linear relationship between counter bit setting and measured resolution allows for simple resolution control logic, which is beneficial in ultra-low power applications.

The acceptable input voltage range scales with V_{DD}, setting a constant 100mV offset from the rails to maintain the VCOs in a highly linear range of operation. The wide range of voltage scalability allows the proposed interface to be used in

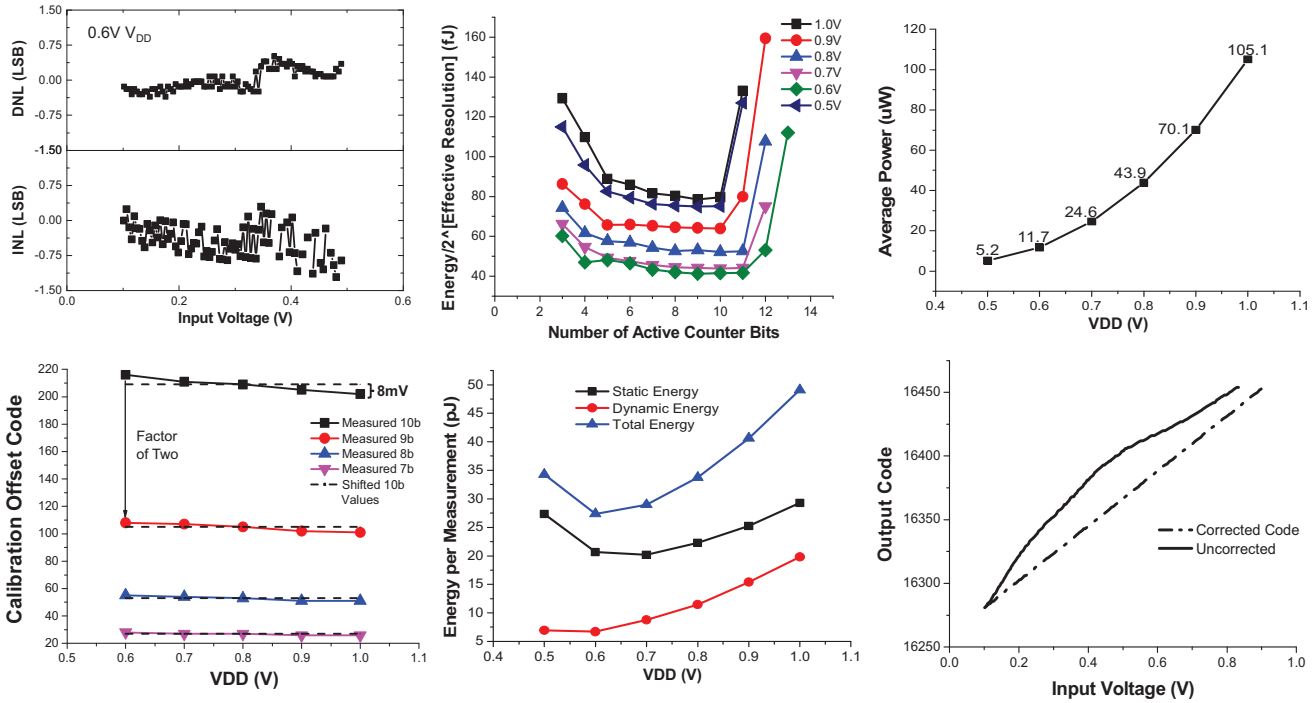

Fig. 7: Resolution, energy, power, and offset measurements. (Top Left) Post-correction DNL and INL with a small look up table (0.6V V_{DD}) (Top Middle) Energy per bit of resolution for each preset resolution value. (Top Right) Average power consumption over scaled V_{DD} from 0.5V to 1.0V. (Bottom Left) Calibration offset from stored and resolution scaled values. (Bottom Middle) Static and dynamic energy breakdown over scaled V_{DD}. (Bottom Right) Uncorrected and corrected (small lookup table) output codes versus input voltage. Post-correction preformed after data collection from the sensor nodes.

systems operating at significantly different voltages. Resolution is insensitive to voltage scaling down to 0.6V, allowing for consistent measurements across different voltage domains. The resolution range covers the maximum resolution required in most sensor applications and can be widely scaled to energy efficient resolutions for wakeup monitoring.

Average power scales linearly as V_{DD} is reduced from 1.0V to 0.7V, tapering off at 0.6V to 0.5V as the constant current draw of the linearizing circuit begins to dominate. Conversion time scales exponentially with the number of active counter bits, from 36ns to 9.3µs (2.8 to 11.0 bits) at 0.6V. At very low resolution, the conversion time saturates as the delay of the FSM becomes limiting. These conversion times are acceptable for sensor applications where values change on the scale of milliseconds (*e.g.*, temperature) and are comparable to ADCs presented in [2,7]. Energy per conversion step also scales exponentially with resolution, from 0.6pJ to 217pJ at 0.6V (Fig. 7). Thus, reducing the number of active counter bits is highly beneficial to system energy, decreasing it by up to 1000x.

Fig. 7 shows a breakdown of energy consumption for 9b operation. Minimum energy per conversion step is 27pJ, achieved at 0.6V. Energy per conversion step remains relatively constant over a range of 5-10 bits, increasing at higher resolutions due to system noise limitations and at lower resolutions due to the saturation of both power and conversion time mentioned above. The minimum achieved value for energy per conversion step at a setting of 9b is 41.2fJ/b at 0.6V with a maximum at 9b of 80.4fJ/b at 1V V_{DD} (Fig. 7). Energy per conversion step is constant between 5b and 10b due to the exponential scaling of energy and linear scaling of resolution.

At 1V, the average INL and DNL in 9b mode are +0.12/-0.52 LSB and +0.22/-0.17 LSB, respectively, after digital correction. Fig. 8 shows the pre- and post-transformation output codes.

The proposed sensor interface core area occupies 346µm^2. This area does not include a register used to store the offset value for crossover calibration, an additional 8 registers to store the offset value would add roughly 50µm^2 in additional area. Compared to more traditional implementations, this area is 100× smaller than a resolution scalable (up to 10.5b) SAR presented in [4] (ideally scaled from 65nm) and 10× smaller than an 8-bit 28nm sub-ranged SAR [8].

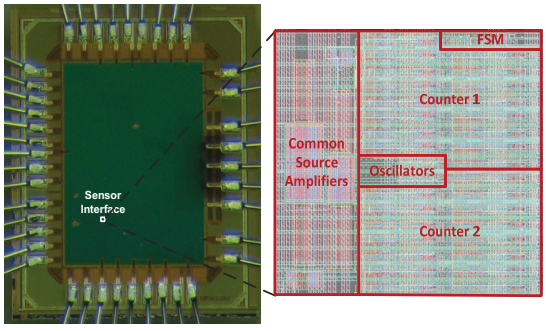

Fig. 8: Die micrograph and chip layout. Fabricated in a 28nm LP CMOS process and occupies 346µm^2.

Resolution scalability is increased by 4 bits and conversion time at low voltage is improved by 50× compared to [9]. While power consumption is higher, this implementation does not require high accuracy current and voltage sources or low jitter timing references, which are generally unavailable in sensor node applications.

IV. Conclusion

In this paper, we presented a reference-free, VCO-based sensor interface circuit in 28nm LP CMOS, designed to specifically address the constraints of wireless sensor nodes. This design is implemented in an area of ~1/100th that of prior approaches. Resolution scalability is between 2.8 and 11.7bits, and power supply can scale from 500mV to 1.0V. The ease of design and use, in addition to the wide range of operating conditions of this circuit, allow for implementation in a variety of sensor applications.

Acknowledgment

We thank STMicroelectronics for fabrication. This project is based upon work supported by the National Science Foundation Graduate Student Research Fellowship under Grant No. DGE 1256260.

References

[1] G. Chen, M Fojtik, D. Kim, D. Fick, J. Park, M. Seok, M. Chen, Z. Foo, D. Sylvester, and D. Blaauw, "Millimeter-Scale Nearly Perpetual Sensor System with Stacked Battery and Solar Cells," *ISSCC*, 2010, pp. 288-289.

[2] M. Suster, J. Guo, N. Chaimanonart, W. Ko, and D. Young, "A Wireless Strain Sensing Microsystem with External RF Power Source and Two-Channel Data Telemetry Capability," *ISSCC*, 2007, pp. 380-381.

[3] J. Daniels, W. Dehaene, M. Steyaert, and A. Wiesbauer, "A 0.02mm^2 65nm CMOS 30MHz BW All-Digital Differential VCO-based ADC with 64dB SNDR," *VLSI*, 2010, pp. 155-156.

[4] M. Yip, and A. Chandrakasan, "A Resolution-Reconfigurable 5-to-10b 0.4-to-1V Power Scalable SAR ADC," *ISSCC*, 2011, pp. 190-191.

[5] N. Verma, and A. Chandrakasan, "An Ultra Low Energy 12-bit Rate-Resolution Scalable SAR ADC for Wireless Sensor Nodes," *JSSC*, June 2007, pp. 1196-1205

[6] P. Clark, D. Johnson, M. Kniep, B. Huttash, A. Wood, M. Johnson, C. Mcgillivan, and K. Titus, "An advanced, low cost, GPS-based animal tracking system," *Rangeland Ecology & Management*, 2006, pp. 334-340.

[7] S. Hanson, M. Seok, Y. Lin, Z. Foo, D. Kim, Y. Lee, N. Liu, D. Sylvester, and D. Blaauw, "A Low-Voltage Processor for Sensing Applications with Picowatt Standby Mode," *JSSC*, Apr. 2009, pp. 1145-1155.

[8] Y. Lien, "A 4.5-mW 8-b 750-MS/s 2-b/Step Asynchronous Subranged SAR ADC in 28-nm CMOS Technology," *VLSIC*, 2012, pp. 88-89.

[9] P. Cong, N. Chaimanonart, W. Ko, D. Young, "A Wireless and Batteryless 10-Bit Implantable Blood Pressure Sensing Microsystem with Adaptive RF Powering for Real-Time Laboratory Mice Monitoring," *JSSC*, Dec. 2009, pp. 3631-3644.

	This work			Yip [4] ISSCC 2011	Suster [2] ISSCC 2007	Cong [9] JSSC 2009
Technology	28nm			65nm	1.5µm	1.5µm
Architecture	VCO			SAR	1st-order ΔΣ 2nd-order ΔΣ	Cyclic ADC
Key Features	Scalable Resolution, Low Area			Scalable Resolution	—	Low Power
Requires Accurate Current Sources	No			Yes	Yes	No
Requires Low Jitter Timing Reference	No			Yes	Yes	Yes
Area (µm^2)	346 – Linearized			212,000 91323 (scaled)	1,597,000 (total)** 687,938 (scaled)	532,400** 229,341 (scaled)
VDD (V)	0.6	0.8	1.0	0.4 – 1.0	3.0	2.0
Effective Resolution	2.81 – 11.00	3.70 – 11.65	3.70 – 10.96	6.4–10.5*	11.16* – strain 12.61* – temp	12.29* – pressure
Power (µW)	11.73	43.91	105.02	0.206	Not Reported	12
Conversion Time (µs)	0.036 – 9.3	0.022 – 3.3	0.016 – 1.02	0.0005	(1st-order) 5.88 (2nd-order) 0.39	500

* ENOB to ER conversion via IEEE standard 1057
** Not Reported – Estimated
Ideal scaling applied to areas

Fig. 9: Results and comparison table.