8.5 A 60%-Efficiency 20nW–500μW Tri-Output Fully Integrated Power Management Unit with Environmental Adaptation and Load-Proportional Biasing for IoT Systems

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As Internet-of-Things (IoT) systems proliferate, there is a greater demand for small and efficient power management units. Fully integrated switched-capacitor (SC) DC-DC converters are promising candidates due to their small form factor and low quiescent power, aided by dynamic activity scaling [1-3]. However, they offer a limited number of conversion ratios, making them challenging to use in actual systems since they often require multiple output voltages (to reduce power consumption) and use various input power sources (to maximize flexibility). In addition, maintaining both high efficiency and fast load response is difficult at low output current levels, which is critical for IoT devices as they often target low standby power to preserve battery charge. This paper presents a fully integrated power management system that converts an input voltage within a 0.9-to-4V range to 3 fixed output voltages: 0.6V, 1.2V, and 3.3V. A 7-stage binary-reconfigurable DC-DC converter [1-2] enables the wide input voltage range. Three-way dynamic frequency control maintains converter operation near-optimum conversion efficiency under widely varying load conditions from 6nW to 500μW. A proposed load-proportional bias scheme helps maintain high efficiency at low output power, fast response time at high output power and retains stability across the entire operating range. Analog drop detectors improve load response time even at low output power, allowing the converter to avoid the need for external sleep/wakeup control signals. Within a range of 1-to-4V input voltage and 20nW-500μW output power, the converter shows >60% conversion efficiency, while maintaining responsiveness to a 100× sudden current increase.

The entire control loop operates with a divided converter clock to maintain dynamic power consumption that is proportional to the SC converter switching loss. This ensures that efficiency loss due to the control loop is always a small predictable value regardless of load current level. Other digital blocks are also clocked by this divided converter clock (Fig. 8.5.3, bottom right). This helps reduce their power consumption relative to the system’s output power level, but also maintains control loop stability since the operating speed of the various blocks are all scaled by the same factor – hence, blocks can communicate with each other at similar relative response speed, including output voltage.

While the load-proportional speed adjustment scheme offers these benefits, it also has a drawback in the case of small output power. In that case, the system responds slower relative to external condition changes, such as a sudden load current increase. To address this problem, the frequency control loop in each converter has a dedicated fast voltage drop detector that monitors converter output voltage and triggers a drop detection signal when it goes below certain threshold. The drop detector requires periodic reset to detect output voltage changes and maintain a certain threshold level. Hence, each converter contains two drop detectors for uninterrupted overlapping operation and detection: one detector always remains on while the other is being reset. By focusing only on triggering upon a fast single drop event without considering stability or continuous detection, the detector’s response time can be boosted hundreds times faster compared to the main feedback path, rendering the control loop fast enough for sudden current load changes. Once the detection signal is triggered, the clock frequency is set to its maximum, quickly restoring the output voltage to safe levels. Afterwards, feedback through the main path slowly lowers the clock frequency to support any sustained increase in load current. Drop detector bias current is also adjusted to be load proportional.

The power management system chip was fabricated in 0.18μm CMOS and a die photo is shown in Fig. 8.5.7. The system stably delivers 1.2V, 3.3V, and 0.6V output voltages from an input voltage ranging from 0.9V to 4V (Fig. 8.5.4). Figure 8.5.5 (top) shows the drop detector responds to 100× sudden load current increase. Graphs and the bottom show the converter supplies 20nW–500μW with >60% efficiency. Fig. 8.5.6 summarizes results and compares the design with previous relevant work.

References:
Figure 8.5.1: Overall architecture of the complete power-management system and its operation.

Figure 8.5.2: Structure of SC converters.

Figure 8.5.3: Frequency control loop with load-proportional biasing scheme.

Figure 8.5.4: Measured performance vs. input voltage.

Figure 8.5.5: Measured drop detector operation (top) and performance vs. output power (bottom).

Figure 8.5.6: Performance summary and comparison.
Figure 8.5.7: Die micrograph.