A Fully Integrated Counter Flow Energy Reservoir for Peak Power Delivery in Small Form-Factor Sensor Systems

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Abstract—We present a fully integrated energy reservoir unit using a counter flow method for peak power delivery in space-constrained sensor systems. Recent advances in circuits have enabled significant reduction in the size of wireless systems such as implantable biomedical devices. As a consequence, the batteries integrated in these systems have also shrunk, resulting in high internal resistances (~10 kΩ). However, the peak current requirement of power-hungry components such as radios remains in the milliwatt range and hence cannot directly be supplied from the battery. Therefore, an energy reservoir with high output power but small size is required. We present an efficient energy reservoir that dynamically reconfigures a storage capacitor array using a so-called counter flow approach. By creating a voltage gradient on capacitor arrays and moving the capacitors along the slope of the gradient, the supply voltage can be maintained while the energy stored in the reservoir is delivered efficiently to the load. The counter flow energy reservoir delivers 65% of stored energy before recharging is needed which allows up to a 12× reduction in overall capacitor size compared with our implementation of the previous method. The design supplies up to 13.6-mW output power for 1 μs. We demonstrate the proposed concept with a pulsed radio, showing an 11.5× increase in pulse length compared with the previous method.

Index Terms—Biomedical implant, counter flow, countercurrent flow, energy reservoir, power, sensor node, wireless.

I. INTRODUCTION

SMALL form-factor systems are widely applicable in biomedical research and medical implants. Millimeter-scale implantable systems can monitor ECG signals [1], intraocular pressure [3], stimulate the spine [2], and analyze blood samples [4]. To store energy, many of these small implantable systems use small form-factor batteries, which often have high internal resistance. For example, the commercial battery used in [5] has an internal resistance of up to 30 kΩ, which limits the direct current that can be drawn from the battery to 7 μA

with 200-mV voltage drop. Moreover, the internal resistance of batteries becomes worse with cycling, which further limits the output current.

However, the peak current requirement of power-hungry components, such as radios, remains in the hundreds of microampere or even milliampere range. Therefore, if we directly connect the battery to the supply, as shown in Fig. 1, the battery voltage VBAT drops unacceptably when a burst of large current is pulled by the load circuits. One solution to this problem, illustrated in Fig. 2, is to directly power this high burst of current through a storage capacitor Cs, which is proposed for some pulse-based radios [6]. The capacitor is then recharged using a current limiter to protect the battery from excessive droop. This paradigm raises two challenges: 1) to supply sufficient energy, very large capacitance (>50 nF) is often needed based on calculation (200-mV drop with battery voltage of 4 V for 10-mW and 5-μs pulse duration), leading to a large die area or a bulky off-chip discrete component and 2) only a small fraction (~5% based on calculation) of energy stored in the capacitor is actually delivered to the high-power components since the capacitor can only be discharged by a few hundred millivolt while maintaining proper circuit operation. In this section, we set 200-mV drop (equivalent to 5% supply voltage drop) as criteria to compare different design alternatives, because it is reasonable for many supply voltage sensitive circuits, such as amplifiers and memory. In real implementation, the proposed method can still operate beyond 5% supply voltage drop.

Alternatively, to extract more energy from the storage capacitor and reduce its size, a dc–dc converter can be used to more fully deplete the stored energy while maintaining the required supply voltage (Fig. 3) [7]. However, such a high output power dc–dc converter requires either an off-chip discrete inductor or a large on-chip flying capacitor array with a total capacitance similar to or even larger than that of the mentioned storage capacitor, making this solution also unsuitable for small form-factor sensors.

Another alternative solution is to decompose the large storage capacitor Cs into multiple small capacitors and reconfigure them to maintain supply (Fig. 4). When the supply voltage drops below the minimum allowable voltage for the circuit, which we refer to as V_{min}, the simplest reconfiguration scheme is to stack the capacitors in series to boost the voltage [8]. However, this leads to a $2 \times V_{min}$ supply voltage overshoot, which is not possible for many circuits.
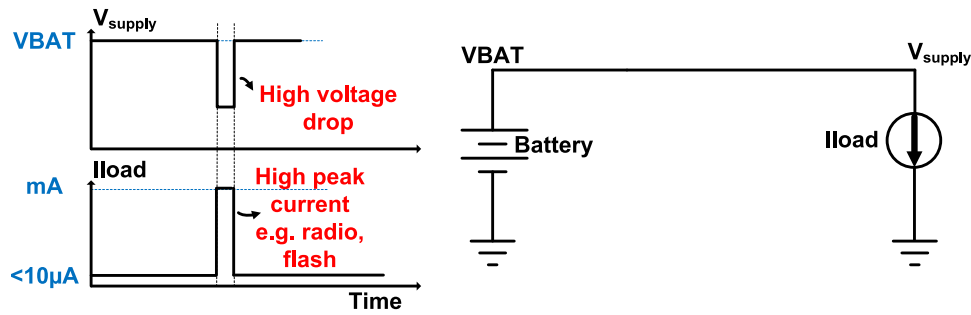
Fig. 1.   Voltage and current waveforms with direct battery connection.
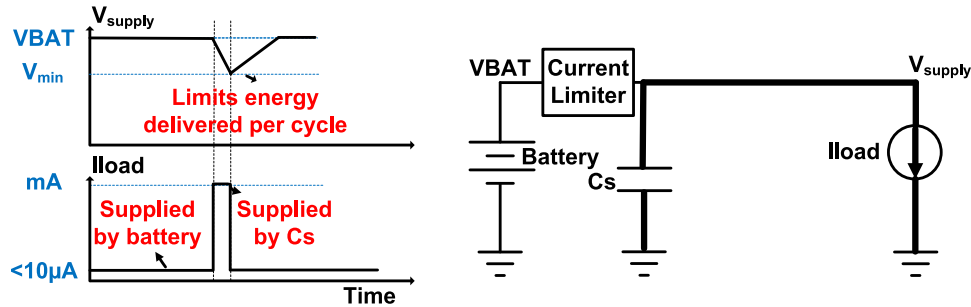

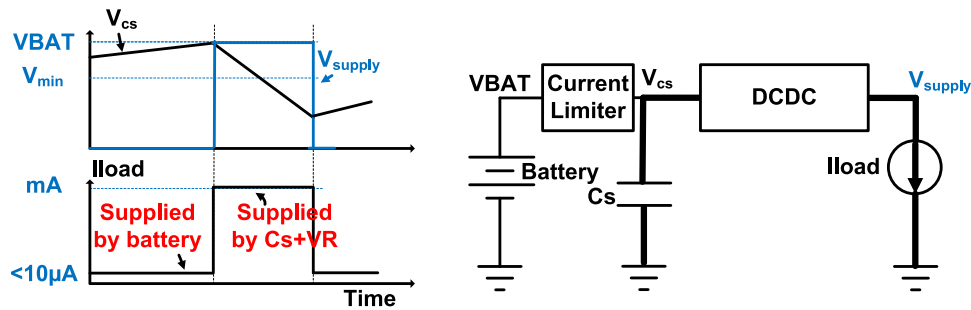Fig. 2.   Voltage and current waveforms with the single capacitor method.

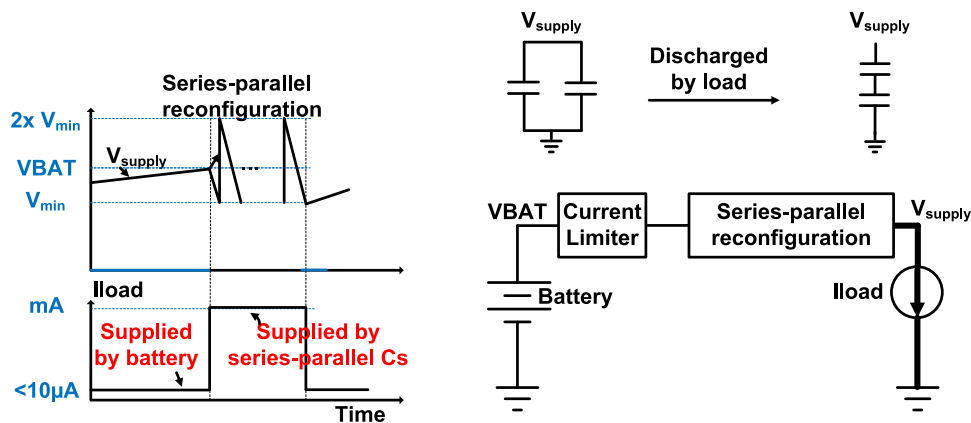Fig. 3.   Voltage and current waveforms with dc–dc converter.

Fig. 4.   Voltage and current waveforms with series parallel reconfiguration.

A feasible alternative is to stack a small portion of the capacitors in series and connect this stack in parallel with the rest of the capacitors (Fig. 5). The supply voltage can then be boosted with acceptable overshoot. However, each reconfiguration creates charge-sharing loss due to voltage drop across the switches. Therefore, the energy extraction is only 41% for 16 unit capacitors based on calculation.

To deliver charge with minimum charge sharing loss and to extract a very high percentage of the total charge, we propose a counter flow reconfigurable energy reservoir (extended
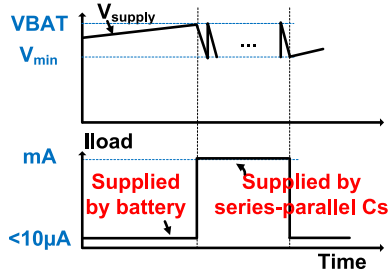
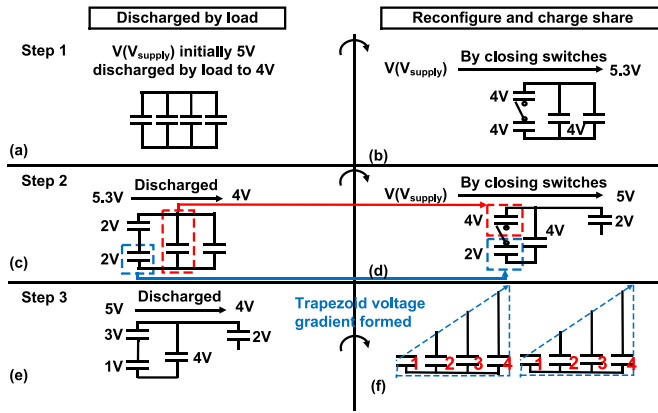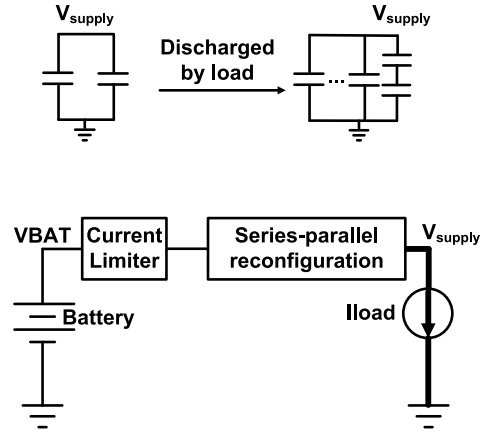Fig. 5. Voltage and current waveforms with charge sharing reconfiguration.

Fig. 6. Operation of the split phase in the proposed energy reservoir.

from [10]). This fully integrated energy reservoir unit dynamically reconfigures a storage capacitor array using a so-called counter flow approach. This design efficiently integrates the storage capacitor and dc–dc converter into one circuit, thereby maximizing the area efficiency and minimizing the charge sharing loss.

II. PROPOSED TECHNIQUE: COUNTER FLOW METHOD

A. Operation Concept of Counter Flow Method

The key challenge in the reconfigurable energy reservoir is to deliver charge with minimum charge sharing loss (i.e., minimized intentional charge sharing steps inside capacitor array) and to extract a very high percentage of the total charge (i.e., minimum remaining voltage on capacitors). To accomplish this, we use an approach inspired by a biological phenomenon called counter flow, where oxygen and blood flow in opposite directions in fish gills, creating a slowly declining oxygen gradient for maximum gas exchange.

We use this idea and apply it to our problem of the efficient extraction of energy from a storage capacitor. This method is conceptually shown in Figs. 6–8 with 8 unit capacitors, a battery voltage of 5 V and a minimum circuit operating voltage of 4 V. As shown in Fig. 6(a), we start with all

capacitors charged to 5 V in parallel, and they are then discharged by the load to 4 V. Then two capacitors are connected in series [Fig. 6(b)] and subsequently connected in parallel with the other two capacitors, boosting the supply voltage upon closing the switches. In a real implementation, a time-spreading technique (see Section II-C) in which switches are closed sequentially is used to limit the voltage overshoot to 5%. As the load discharges the supply voltage to 4 V [Fig. 6(c)], we obtain 2 capacitors at 2 V and 2 capacitors at 4 V. Next, we connect a capacitor at 2 V and a capacitor at 4 V in series [Fig. 6(d)] and then connect them in parallel with a capacitor at 4 V, boosting the voltage again. Similarly, at the end of discharge to 4 V by the load, we have formed a capacitor at 1 V and a capacitor at 3 V [Fig. 6(e)]. Along with the capacitor at 2 V and the capacitor at 4 V formed in the previous steps, we form a capacitor array with a trapezoid voltage gradient of 3 V [Fig. 6(f)]. In each round of reconfiguration, we stack the capacitor with the highest voltage with the lowest, the second highest with the second lowest, etc., and share charge with the capacitors when the load is at V_{min}. This operation has two purposes: 1) the supply voltage is maintained with each reconfiguration and 2) intermediate voltages are formed systematically at the end of discharge, and all previous formed voltages are conserved. In this way, the trapezoid capacitor array becomes more fine-grained with each round of operation. At the end of this process, each capacitor size is split in half, forming two identical sets of trapezoid capacitor arrays.

Then we stack the 2 set of capacitors in series, as shown in Fig. 7(a). The top four capacitors are charged to decreasing voltages that is represented by a trapezoidal shape, and the bottom four capacitors are charged to increasing voltages, creating a second trapezoid. The blue and red lines indicate the voltages of the different capacitors. Then we insert switches that allow us to reconfigure the capacitors. As the load discharges the supply voltage to 4 V [Fig. 7(b)], we shift the two trapezoids in opposite directions [Fig. 7(c)], boosting the supply voltage to 5 V again. This process is repeated. As the supply voltage is once again discharged to 4 V by the load [Fig. 7(d)], we shift the two trapezoids in opposite directions,
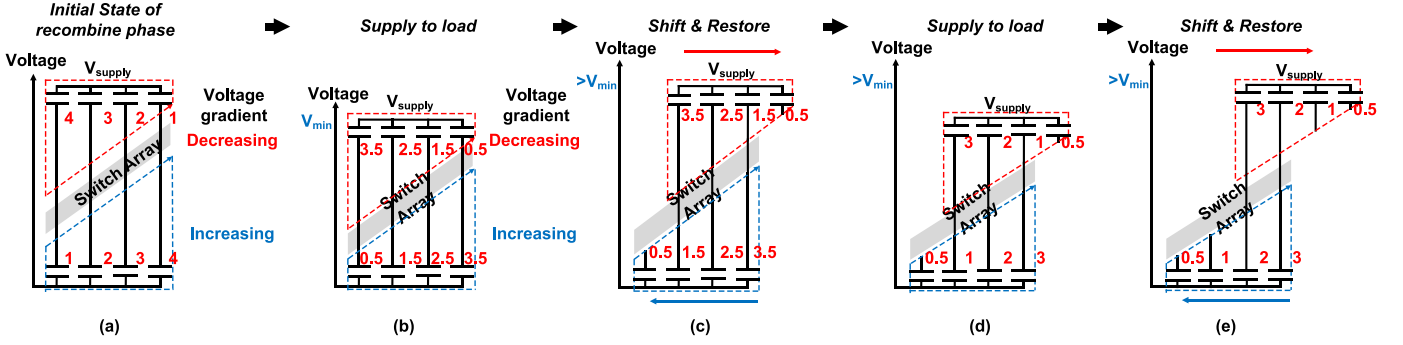
Fig. 7. Operation of the 1st round of recombine phase in the proposed energy reservoir.
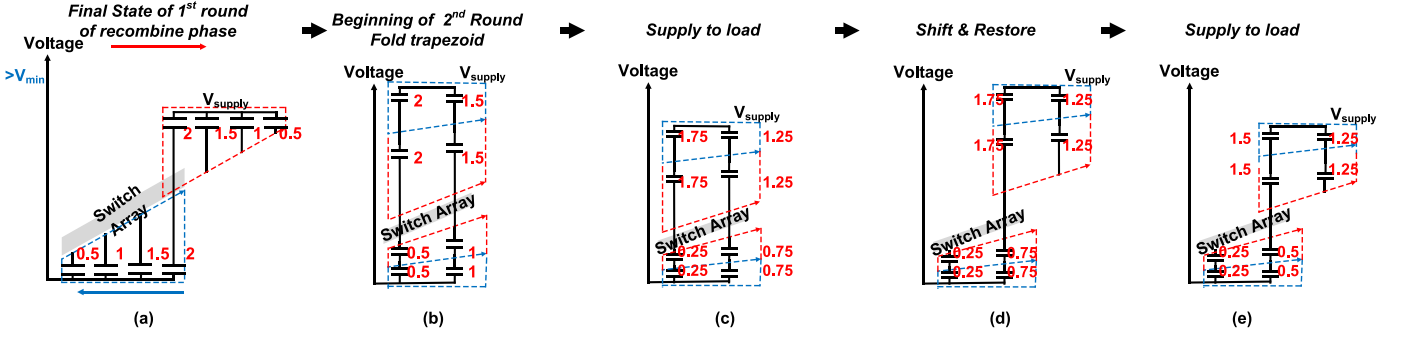

Fig. 8. Operation of the 2nd round of recombine phase in the proposed energy reservoir.

increasing the voltage by the slope of the gradient with each shift [Fig. 7(e)]. Since each shift operation simply increases the supply voltage and does not cause any charge sharing within the capacitor array, charge-sharing loss is eliminated, resulting in highly efficient energy delivery. 78% energy is extracted based on theoretical calculation with 16 unit caps and 200-mV voltage drop.

Fig. 8(a) shows the final state of this process and indicates the charge still remaining on the capacitors. To extract this remaining energy from the reservoir, we fold the trapezoid and stack four capacitors in series to restore nominal supply voltage, forming two new trapezoids. As shown in Fig. 8(b)–(e), when the voltage is discharged to V_{min}, we repeat the stack and shift operation as we previously did in the first round, resulting in 82% total energy extraction efficiency based on calculation with 16 unit caps and 200-mV voltage drop. This second round of operation requires 13 more switches in a real implementation.

In summary, the proposed counter flow energy reservoir has two phases (Fig. 9). In phase 1, which is referred to as the split phase, a voltage gradient is created across two sets of capacitors with 13% charge sharing loss. In phase 2, which is referred to as the recombine phase, the two sets of capacitors are stacked together in reverse direction and repeatedly shifted in opposite directions as the load draws charge from the reservoir, increasing the voltage by the slope of the gradient with each shift. Since this shift operation simply increases the load voltage V_{supply} and does not cause any charge sharing within the capacitor array, charge-sharing loss is avoided, resulting in highly efficient energy delivery. By repeatedly shifting, the vast majority of stored charge can be extracted,
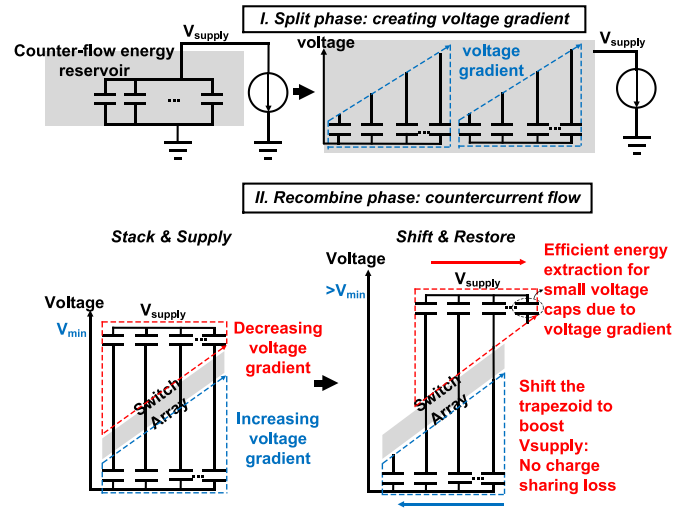

Fig. 9. Summary of the two-phase operation of counter flow energy reservoir.

maximizing the total delivered charge. A second round of the recombine phase can be implemented by folding the trapezoids, as described previously, leaving only 5% energy not extracted based on calculation with 16 unit caps and 200-mV voltage drop (see Section II-B for derivation). This process results in a total energy extraction efficiency of 82% for the entire process. It should be noted that we claimed no charge sharing loss in recombine phase assuming no decoupling capacitors at output. When decoupling capacitors are added at the output, there will be charge-sharing loss every time the energy reservoir is reconfigured, including the recombine phase. This can degrade energy delivery efficiency depending
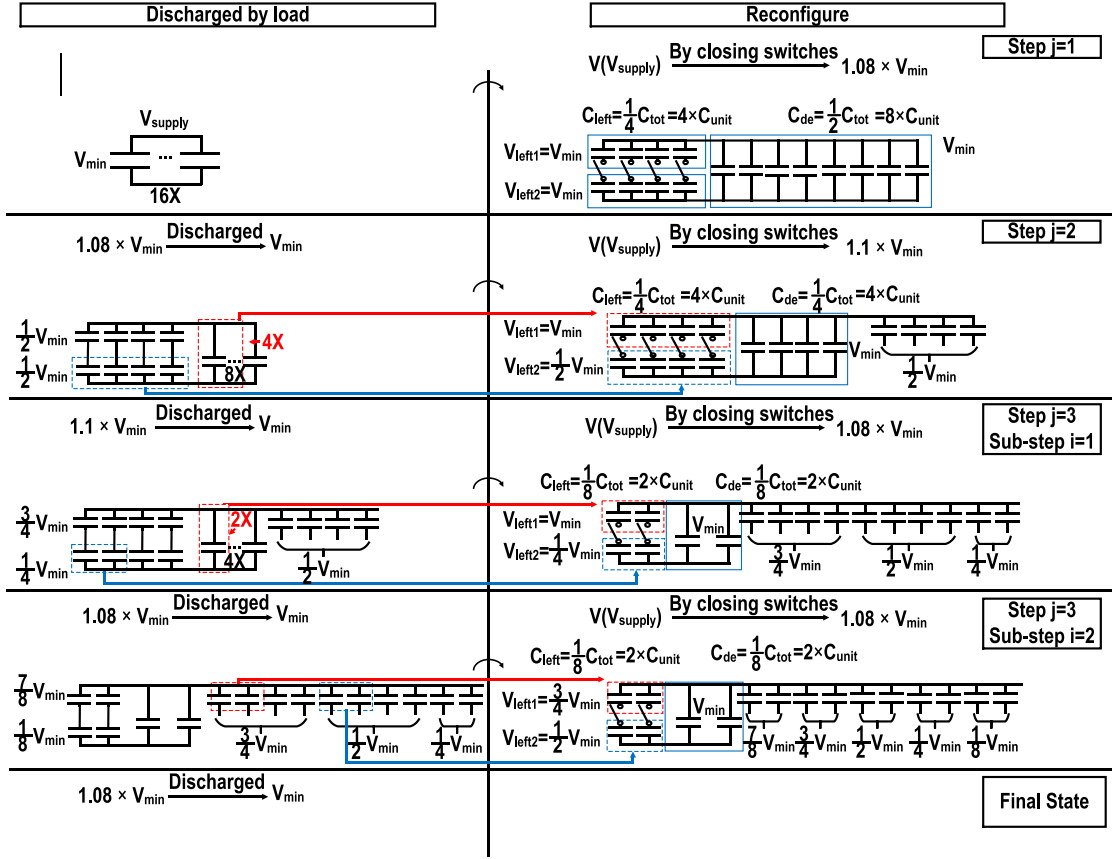
Fig. 10. Illustration of steps in split phase for 16 unit capacitors.

on the capacitance of the decoupling capacitor, and we think this issue is hard to avoid for most switched-capacitor energy delivery schemes.

B. Energy Efficiency Analysis

To analyze the theoretical performance of the proposed counter flow energy reservoir, we define an efficiency metric named single shot energy delivery efficiency, $\text{Eff}_{\text{single-shot}}$. The efficiency is defined in (1), where $E_{\text{deliver,split}}$ is the energy delivered in split phase, $E_{\text{deliver,recombine}}$ is the energy delivered in the recombine phase, and E_{stored} is the total energy originally stored in the energy reservoir. The single shot energy delivery efficiency indicates how efficiently energy is extracted before recharging

$$\text{Eff}_{\text{single-shot,proposed}} = \frac{E_{\text{deliver,split}} + E_{\text{deliver,recombine}}}{E_{\text{stored}}}. \quad (1)$$

In order to analyze the single shot energy delivery efficiency, we need to understand the two major sources of loss in the proposed design. The first source of loss is charge sharing. As discussed before, charge-sharing loss only exists in the split phase due to explicit charge sharing in each round of reconfiguration to boost the supply voltage. During the recombine phase, the supply voltage is maintained by shifting the capacitors without explicit charge sharing. The second source of loss is the residual energy in the reservoir at the end of the entire reconfiguration process.

This general analysis is performed with 2^{n+1} unit capacitors, total capacitance C_{tot}, a battery voltage VBAT, and a minimum voltage V_{min} for proper circuit operation.

First, we analyze the charge sharing loss in the split phase. In each step of the split phase, a set of capacitors (with capacitance C_{left} and voltage V_{left1}) is connected in series with a second set of capacitors (with capacitance C_{left} and voltage V_{left2}), and they share charge with another set of capacitors (with capacitance C_{de} and voltage V_{min}). Fig. 10 shows the three reconfiguration steps, which we denote as j, and their sub-steps, which we denote as i, in the split phase for 16 unit capacitors ($n = 3$). Values of C_{left}, C_{de}, V_{left1}, and V_{left2} for each step j and sub step i are also shown in Fig. 10. In general, these values are expressed in (2)–(5) for each step j and sub step i. In these equations, n is the number of steps in the split phase for 2^{n+1} unit capacitors

$$C_{\text{left},j} = \begin{cases} \dfrac{C_{\text{tot}}}{4}, & j = 1 \\ \dfrac{C_{\text{tot}}}{2^j}, & 2 \le j \le n \end{cases} \quad (2)$$

$$C_{\text{de},j} = \begin{cases} \dfrac{C_{\text{tot}}}{2}, & j = 1 \\ \dfrac{C_{\text{tot}}}{2^j}, & 2 \le j \le n \end{cases} \quad (3)$$

$$V_{\text{left1},ij} = \begin{cases} V_{\text{min}}, & j = 1 \\ \dfrac{V_{\text{min}}}{2^{j-1}} * i, & 2 \le j \le n, \ 1 \le i \le 2^{j-2} \end{cases} \quad (4)$$

$$V_{\text{left2},ij} = \begin{cases} V_{\min}, \quad j = 1 \\ \left(1 + \dfrac{1}{2^{j-1}}\right) * V_{\min} - V_{\text{left1},ij} \\ \qquad\qquad 2 \le j \le n, \quad 1 \le i \le 2^{j-2}. \end{cases} \quad (5)$$

The energy loss for the split phase is expressed in (6), as the sum of $E_{\text{loss,step}}$, where $E_{\text{loss,step}}$ (7) is the charge sharing loss at each sub step i. The total charge sharing loss in the split phase $E_{\text{loss,split}}$ is then calculated in (8). From the voltages across each of the capacitors at the end of the split phase [listed in (9), each number represents the voltage across 2 unit capacitors], we can derive the energy remaining in the reservoir at the end of the split phase, $E_{\text{endstate,split}}$ (10). Finally, the energy delivered to the load during the split phase $E_{\text{deliver,split}}$ can be calculated using (11), where E_{stored} is the energy originally stored in the energy reservoir, $E_{\text{endstate,split}}$ is the energy left at the end of split phase and $E_{\text{loss,split}}$ is the charge sharing loss in the split phase

$E_{\text{loss,split}}$

$$= \sum_{j=1}^{n} \sum_{i=1}^{2j-2} E_{\text{loss,step}}(C_{\text{left},j}, C_{\text{de},j}, V_{\text{left1},ij}, V_{\text{left2},ij}) \quad (6)$$

$$E_{\text{loss,step}}(C_{\text{left},j}, C_{\text{de},j}, V_{\text{left1},ij}, V_{\text{left2},ij}) = \frac{2^{1-3j}}{3} C_{\text{tot}} V_{\min}^2 \quad (7)$$

$$E_{\text{loss,split}} = 0.05 C_{\text{tot}} V_{\min}^2 + \frac{2^{-3-2n}}{9}(-4 + 4^n) C_{\text{tot}} V_{\min}^2 \quad (8)$$

$$\left\{ \frac{V_{\min}}{2^n}, \frac{2V_{\min}}{2^n}, \frac{3V_{\min}}{2^n}, \ldots, V_{\min} \right\} \quad (9)$$

$$E_{\text{endstate,split}} = \frac{1}{2} \frac{C_{\text{tot}}}{2^n} \sum_{m=1}^{2n} \left(m \frac{V_{\min}}{2^n} \right)^2 \quad (10)$$

$$E_{\text{deliver,split}} = E_{\text{stored}} - E_{\text{endstate,split}} - E_{\text{loss,split}}$$

$$= \left[\frac{1}{2} C_{\text{tot}} V_{\text{bat}}^2 \right] - \frac{1}{2} \frac{C_{\text{tot}}}{2^n} \sum_{m=1}^{2n} \left(m \frac{V_{\min}}{2^n} \right)^2$$

$$- [0.05 C_{\text{tot}} V_{\min}^2 + \frac{2^{-3-2n}}{9}(-4 + 4^n) C_{\text{tot}} V_{\min}^2. \quad (11)$$

Next, we will analyze the energy non-extracted in the first round of the recombine phase. In this phase, the trapezoid capacitor arrays are stacked in reverse direction and repeatedly shifted in opposite directions. The capacitors with original voltage $m(V_{\min}/2^n)$ are shifted m times in total. The voltage across each capacitor is discharged by $(V_{\min}/2^{n+1})$ with each shift. Therefore, the voltage across each capacitor at the end of the first round of the recombine phase is $m(V_{\min}/2^n) - m(V_{\min}/2^{n+1}) = (1/2)m(V_{\min}/2^n)$, which is half of the original voltage, as shown in (12) (each number represents the voltage across 2 unit capacitors)

$$\left\{ \frac{1}{2} \frac{V_{\min}}{2^n}, \frac{1}{2} \frac{2V_{\min}}{2^n}, \frac{1}{2} \frac{3V_{\min}}{2^n}, \ldots, \frac{1}{2} V_{\min} \right\}. \quad (12)$$
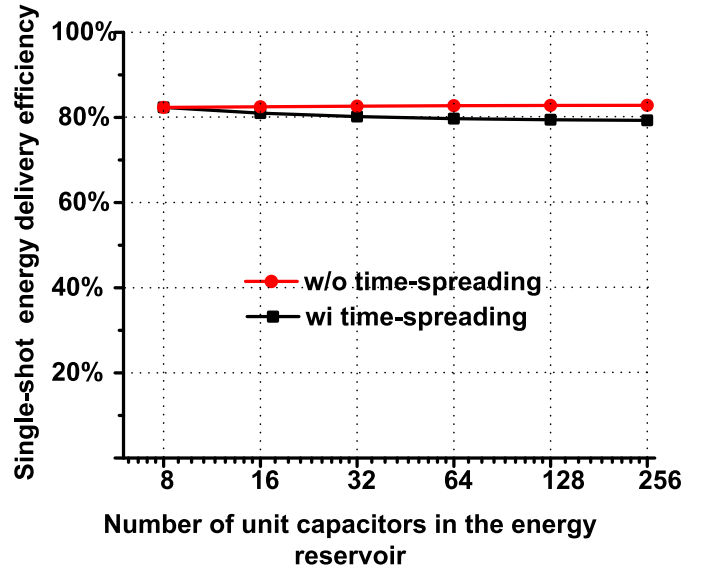

Fig. 11. Efficiency of counter flow energy reservoir over number of discrete capacitors.
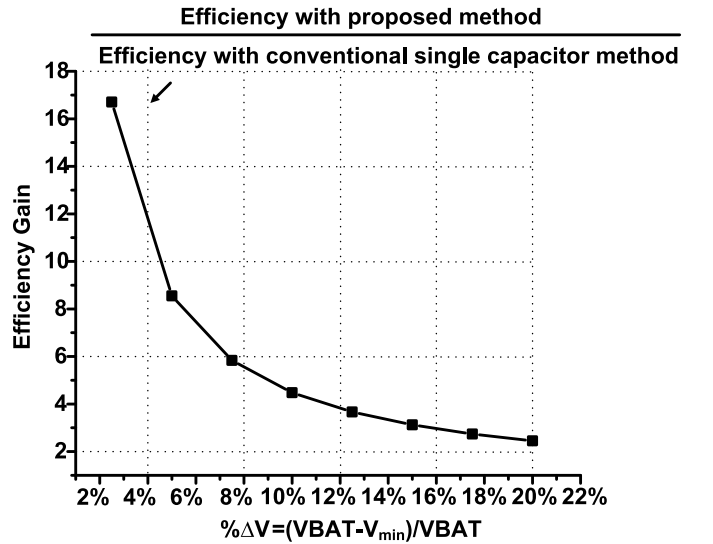

Fig. 12. Efficiency gain of the proposed method across relative allowable supply voltage drop.

By folding the trapezoids in the second round of the recombine phase, more energy can be extracted. The voltage across each capacitor at the end of the second round of recombine phase (13) can be derived by writing out the start and end state of each step. The energy remaining at the end of this phase is expressed in (14). This is the final step in the counter flow energy reservoir. Therefore, $E_{\text{endstate,2ndrecombine}}$ shown in (14) is the energy left non-extracted at the end of the process, which is 5% for 16 unit capacitors and 200-mV voltage drop. Since there is no charge sharing loss in the recombine phase, this residual energy $E_{\text{endstate,2ndrecombine}}$ is the only loss in the recombine phase. The energy delivered for 2 rounds of the recombine phase can easily be calculated in (15), as the difference between the energy left at the end of split phase $E_{\text{endstate,split}}$ and the energy left at the end of
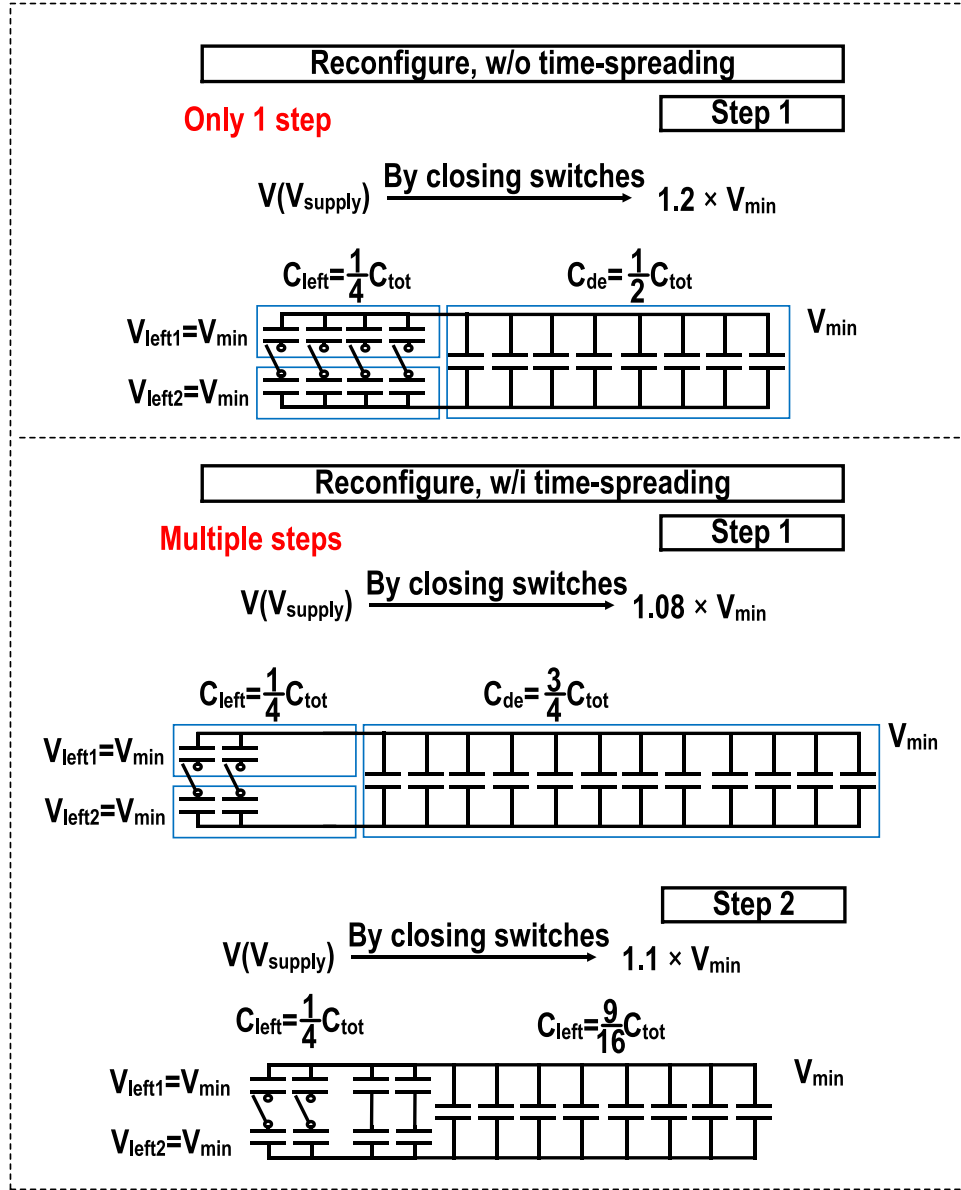
Fig. 13. Operation concept of time-spreading technique.

the second round of recombine phase $E_{\text{endstate,2ndrecombine}}$

$$
\begin{Bmatrix}
\dfrac{1}{4}\dfrac{V_{\min}}{2^n}, \dfrac{1}{4}\dfrac{2V_{\min}}{2^n}, \dfrac{1}{4}\dfrac{3V_{\min}}{2^n}, \dots, \dfrac{1}{2}(2^{n-1}+1)\dfrac{V_{\min}}{2^n} \\
-\dfrac{1}{4}\dfrac{V_{\min}}{2^n}, \dfrac{1}{2}(2^{n-1}+2)\dfrac{V_{\min}}{2^n} - \dfrac{2}{4}\dfrac{V_{\min}}{2^n}, \dots, \dfrac{1}{2}2^n\dfrac{V_{\min}}{2^n} \\
-\dfrac{1}{4}2^{n-1}\dfrac{V_{\min}}{2^n}
\end{Bmatrix}
\quad (13)
$$

$E_{\text{endstate,2ndrecombine}}$

$$
= \dfrac{1}{2}\dfrac{C_{\text{tot}}}{2^n}\left(\sum_{m=1}^{2n-1}\left(\dfrac{1}{4}m\dfrac{V_{\min}}{2^n}\right)^2 \right.
$$
$$
\left. + \sum_{m=2^{n-1}+1}^{2n}\left(\dfrac{1}{2}m\dfrac{V_{\min}}{2^n} - \dfrac{1}{4}(m-2^{n-1})\dfrac{V_{\min}}{2^n}\right)^2\right)
$$
$$
\quad (14)
$$

$E_{\text{deliver,recombine}}$

$$
= E_{\text{endstate,split}} - E_{\text{endstate,2ndrecombine}}
$$
$$
= \dfrac{1}{2}\dfrac{C_{\text{tot}}}{2^n}\left(\sum_{m=1}^{2n}\left(m\dfrac{V_{\min}}{2^n}\right)^2 - \sum_{m=1}^{2n-1}\left(\dfrac{1}{4}m\dfrac{V_{\min}}{2^n}\right)^2\right.
$$
$$
\left. - \sum_{m=2^{n-1}+1}^{2n}\left(\dfrac{1}{2}m\dfrac{V_{\min}}{2^n} - \dfrac{1}{4}(m-2^{n-1})\dfrac{V_{\min}}{2^n}\right)^2\right).
$$
$$
\quad (15)
$$

Finally, the single shot energy delivery efficiency for the entire reconfiguration process is expressed in (16), where a, b, and c are positive, topology-dependent constants; c is approximately 0.18. As shown in (16), c is a topology-dependent scaling factor which indicates how sensitive efficiency is to $((V_{\min}/\text{VBAT}))^2$. One major contribution of c comes from the charge sharing loss in the first step of split phase
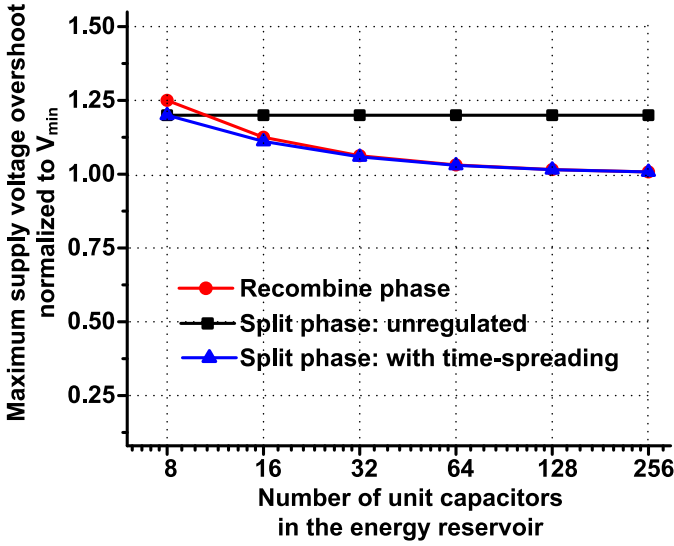
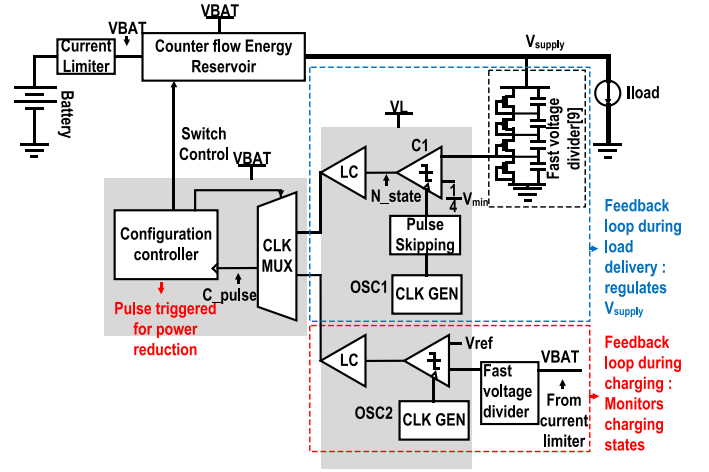Fig. 14. Maximum supply voltage overshoots wi/wo time spreading across number of capacitors.

Fig. 15. Top-level architecture of the implemented counter flow energy reservoir.
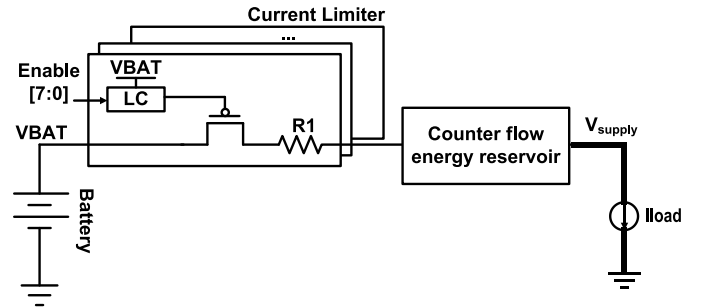
Fig. 16. Circuit implementation of the current limiter.

(step $j = 1$ in Fig. 10), due to the lack of reconfiguration choices. As shown in this equation and Fig. 11, the efficiency of the proposed energy reservoir is relatively independent (for $n > 1$) of the total number of discrete capacitors, 2^{n+1}. However, efficiency is more dependent on V_{min} than on number of capacitors. To compare the efficiency gain of the proposed reservoir over the conventional single capacitor method, we calculate the efficiency using the conventional method in (17). The efficiency gain of the proposed method is expressed in (18) and plotted in Fig. 12 for 16 unit capacitors over $\%\Delta V$, which is the relative voltage drop between V_{min} and VBAT. The efficiency gain is $16.7\times$ with 2.5% voltage drop (100 mV with VBAT = 4 V)

$$\text{Eff}_{single-shot,proposed}$$
$$= \frac{E_{deliver,split} + E_{deliver,recombine}}{E_{stored}}$$
$$= 1 - \left(\frac{V_{min}}{VBAT}\right)^2 * (c + b * 2^{-n} - a * 4^{-n})$$
$$\approx 1 - c \left(\frac{V_{min}}{VBAT}\right)^2 \tag{16}$$

$$\text{Eff}_{single-shot,conventional}$$
$$= \frac{\frac{1}{2}C_{tot}(V_{bat}^2 - V_{min}^2)}{\frac{1}{2}C_{tot}VBAT^2} = 1 - \frac{V_{min}^2}{VBAT^2} \tag{17}$$

$$\text{Gain} \approx \frac{1 - c \left(\frac{V_{min}}{VBAT}\right)^2}{1 - \frac{V_{min}^2}{VBAT^2}}. \tag{18}$$

C. Voltage Overshoot Analysis

After each reconfiguration step in the proposed energy reservoir, the supply voltage is boosted. In the split phase, the boosted voltage in each step is denoted as $V_{boost,j}$, where j is the step number. Without any regulation, the maximum supply voltage overshoot occurs in the first step and is denoted as $V_{max,unregulated,split} = (6V_{min}/5)$. To reduce $V_{max,unregulated,split}$,

time spreading is used. As shown in Fig. 13, instead of stacking two sets of big capacitors and over boosting the supply voltage in one-step, we stack smaller sets of capacitors to boost the supply voltage in multiple steps. In this way, smaller capacitor decks C_{left} are charge shared with C_{de} to reduce the resulting voltage overshoot after charge sharing. The maximum boosted supply voltage using time spreading is denoted as $V_{max,ts,split}$ and shown in (19).

In the recombine phase, the maximum supply voltage overshoot $V_{max,recombine}$ is shown in (20). Fig. 14 shows $V_{max,ts,split}$, $V_{max,recombine}$, and $V_{max,unregulated,split}$ over the total number of capacitors 2^{1+n}, and voltage overshoot is reduced from 20% to <6% with time-spreading (when the total number of capacitors is 32)

$$V_{max,ts,split} = \left(1 + \frac{1}{1 + 2^n}\right) V_{min} \tag{19}$$

$$V_{max,recombine} = \left(1 + \frac{1}{2^n}\right) V_{min}. \tag{20}$$

It is also important to note that time spreading lowers the supply voltage overshoot at the cost of slightly higher charge sharing loss. As shown in Fig. 11, the resulting efficiency is still >79%, only 2% lower compared with the efficiency achieved without using time spreading. Efficiency degradation is slightly overestimated here because time spreading is applied to all of the steps of the split phase. In a real implementation, only the first few steps require time spreading.
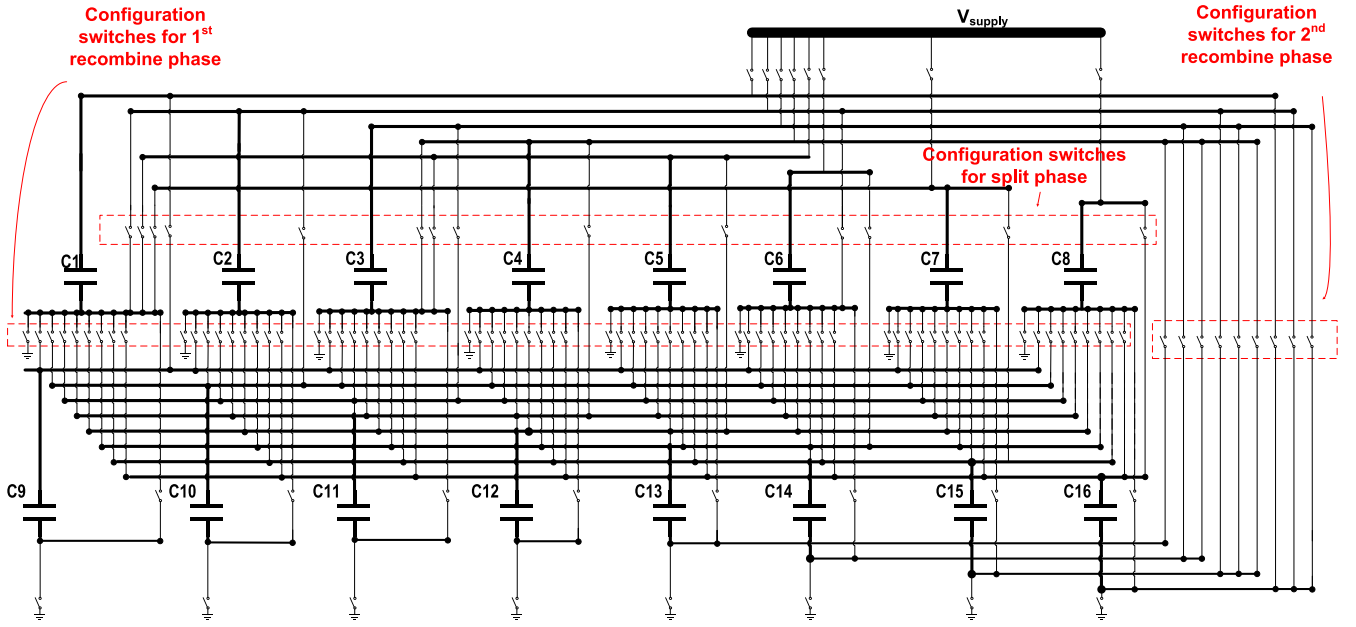
Fig. 17.   Illustration of switch connections in the energy reservoir.

III. IMPLEMENTATION OF COUNTER FLOW ENERGY RESERVOIR

Fig. 15 shows the top-level architecture of the design, consisting of the counter flow energy reservoir, a feedback loop for delivery modulation, a feedback loop for charging modulation, and a configuration controller. When the energy reservoir is in delivery mode, the load is enabled, and V_{supply} is monitored using the "fast voltage divider," which combines a resistive and capacitive voltage divider for fast response time. Capacitors in the fast voltage divider are sized to mitigate the effect of parasitic capacitance at the output node. Leakage power of this structure is 1.9 nW in simulation. When V_{supply} drops below V_{min}, the comparator C1, clocked by clock generator OSC1, triggers a pulse N_state. The configuration controller is an unconditional pulse-based state machine, which proceeds through pre-programmed states on each rising edge of N_state and generates the reconfiguration control signals. In charging mode, the reservoir energy is restored by reversing the steps of the recombine phase, which reduces the voltage difference seen by the current limiter to achieve a much lower charging loss ($\sim 3\times$ lower) than that resulting from directly charging all of the capacitors. The charging state is again monitored by a clocked comparator. The comparators and clock generation operate at 1.2 V to reduce dynamic power (measured 5.2 μW for 700-μW output power). Static power consumption of the proposed energy reservoir is assumed to be negligible compared to >100 μW designed output power. A pulse-skipping module skips clock cycles immediately after C_pulse triggers a configuration change, allowing time for the energy reservoir to restore V_{supply} and thus avoiding false C_pulse edges.

It should be noted that the 1.2-V supply in this implementation is generated off-chip for prototype verification. In a more realistic system implementation, this voltage can be generated on-chip by power management unit (PMU). Since many sensor systems require PMU to generate voltages lower than the battery voltage for efficient operation [2], [11], the efficiency and area degradation of generating an extra voltage may be mitigated by sharing the 1.2-V supply with already existing voltage domains in the system.

The topology used for current limiter is shown in Fig. 16, which composed with a resistor array and eight selection switches for tuning. It should be noted that this structure cannot eliminate reverse current from the energy reservoir to the battery when V_{supply} is higher than battery voltage (simulated peak current is 60 nA when V_{supply} is 300 mV higher than battery voltage). A reverse current protection unit can be implemented to completely turn off PMOS selection switches during charge delivery.

There are 16 unit capacitors used in the implemented energy reservoir, and each of them is 0.197 nF. All capacitors are implemented using MIM capacitors. Fig. 17 illustrate the switch connections. There are in total 119 switches used to configure the capacitor array. There are 22 switches used in split phase, 60 switches used in first round of recombine phase, 13 switches used in second round of recombine phase, and 24 switches used for supply and ground connections.

IV. MEASUREMENTS

The test chip shown in Fig. 18 is fabricated in 180-nm CMOS, and the die area is 3.8 mm^2. The total capacitor is 3.15 nF with 16 unit capacitors, and the control loop area overhead is 18%. We implemented the idea proposed in [6] to compare the performance gain of the proposed method over the single storage capacitor method [6].

Fig. 19 shows the captured supply voltage waveform for a load power of 1.4 mW, V_{min} setting of 3.6 V and VBAT of 3.8 V. The waveform shows $8\times$ longer high-current delivery
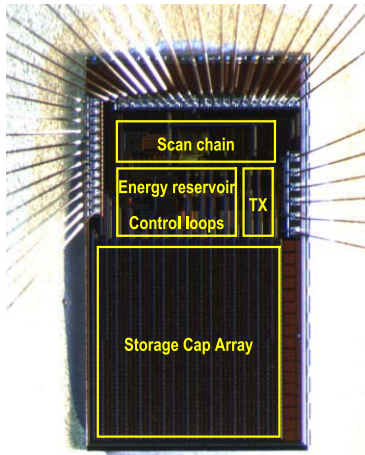
Fig. 18.   Die photograph.
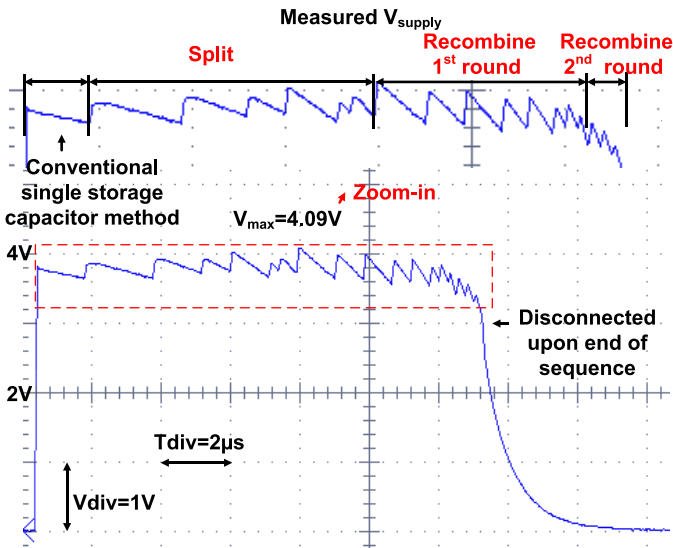

Fig. 20.   Measured energy breakdown.

Fig. 19.   Captured supply voltage waveform.

time compared with the conventional single storage capacitor method (i.e., the first spike on the waveform labeled as "the conventional single storage capacitor method"). It should be noted that the dip of supply voltage in second round of recombine phase is due to the inability of the energy reservoir to be reconfigured fast enough at heavy load, causing a degradation of energy delivery efficiency. In the second round of recombine phase, 4 capacitors are connected in series, making the equivalent capacitance the smallest, and therefore the time allowed for reconfiguration is the smallest.

Fig. 20 depicts the measured energy breakdown, which shows that comparator and control overhead is 5.5% (power overhead is 59 μW when delivering 700 μW output power, at average output voltage of 3.71 V), and the measured charge sharing loss and residual energy loss is 28.97%.

In Fig. 21, we quantify the performance of the reservoir using single shot energy delivery efficiency, as defined in Section II. We measure it over the allowable voltage drop ΔV on the left. The first line from the top is the energy stored originally. The 2nd and 3rd lines are the energy extracted
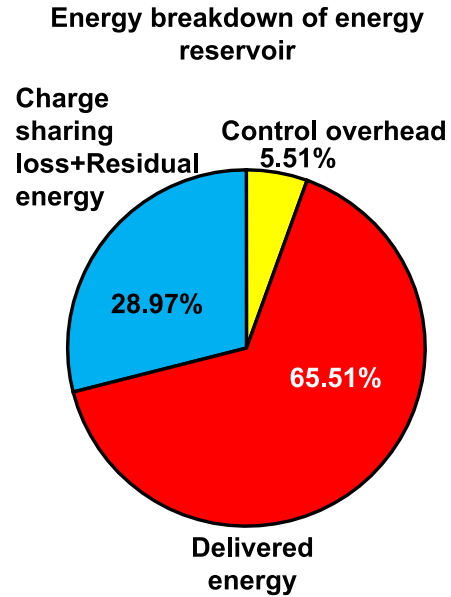
using the proposed method, and the 4th and 5th lines are the energy extracted using the conventional single storage capacitor method. The third line shows that the reservoir extracts 17.5 nJ before recharging, representing an up to 12× improvement over the conventional single storage capacitor method. We also measure the single shot energy delivered over load power on the right. The third line shows that the reservoir maintains >62% efficiency across 45-μW to 8-mW load power. The discrepancy between the measured and theoretical calculated energy extraction is caused by factors including decoupling capacitance at supply voltage, switching loss of power switches and controllers, parasitic bottom capacitance of the capacitor array, and possible incorrect reconfiguration timing. It should be noted that the single shot efficiency drops at heavy load power. There are two main reasons: 1) as load power goes up, V_{supply} drops faster than the reservoir controller can catch up, causing the capacitors to be reconfigured at non-optimal time. This inaccurate timing leads to insufficient energy extraction and 2) On-resistance of the reconfiguration switches causes large voltage drop at heavy load, and therefore capacitors connected to the switches cannot be fully discharged to the intended voltages. Hence the resulting efficiency is lower than expected. This degradation may be improved by using a more advanced technology. Fig. 22 shows the measured single shot energy delivered at different temperatures.

In Fig. 23, we measure the end-to-end efficiency, which is the ratio of the energy delivered to the load to the energy supplied by the battery. The top line shows the end-to-end efficiency achieved by reversing the steps in the recombine phase during charging. The bottom line shows the efficiency achieved by connecting the reservoir to the battery directly. The proposed counter flow charging method improves the end-to-end efficiency from 45% to 70%.

Fig. 24 shows the captured waveforms using counter flow charging and discharging. By reversing the steps in recombine
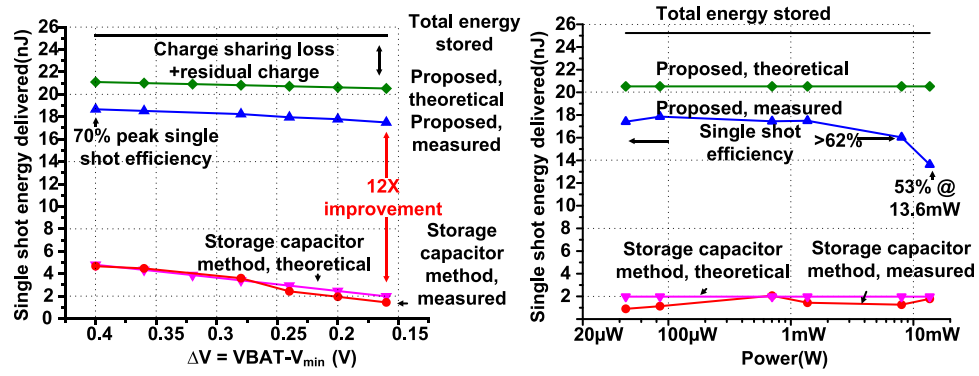
Fig. 21. Single shot energy delivered across allowable voltage drop (left) and load power (right).
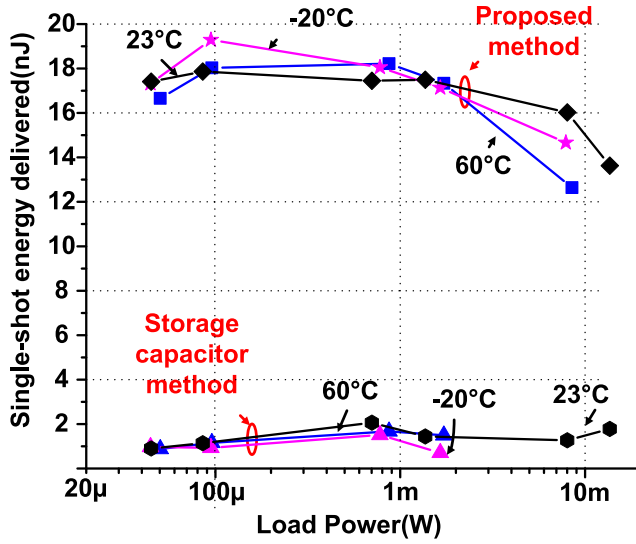

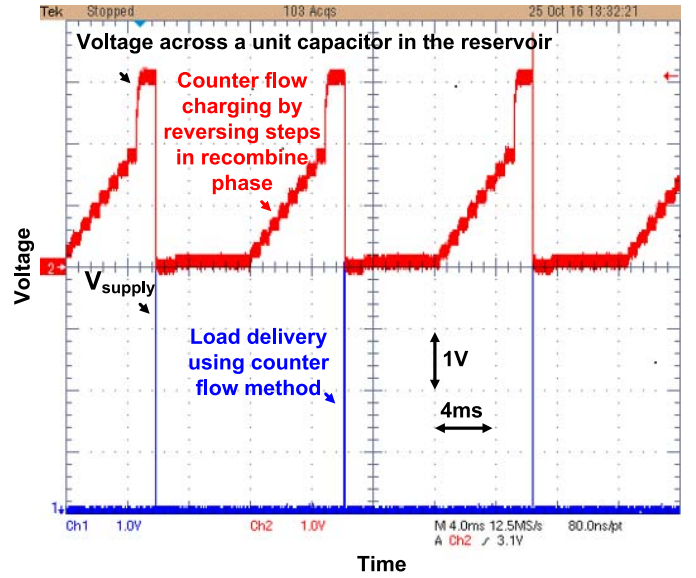Fig. 22. Single shot energy delivered at different temperatures.

Fig. 23. End-to-end efficiency of the proposed energy reservoir.

Fig. 24. Captured waveform showing counter flow charging.

Fig. 25. Integration with radio.

represents a shift of trapezoid stacks in opposite directions. By charging in small steps like walking up a ladder, voltage difference seen across the power switches in each step is reduced, and therefore the resulting charging efficiency is higher than directly connect all capacitors in parallel with the battery.

In Fig. 25, we integrate the test chip with a transmitter as load, which is connected with an inductive antenna. In Fig. 26, the captured transmitter output pulse, shown on the top, demonstrates $11.5\times$ longer continuous transmission than the conventional single capacitor method (i.e., first spike representing energy delivered without configurability) with

phase, capacitors with trapezoid voltage gradients are stacked in reverse directions, and shift in opposite directions whenever the stacked voltage V_{supply} is charged to battery voltage VBAT. The top waveform shows the charging process of one of the unit capacitors in the energy reservoir. Each small step
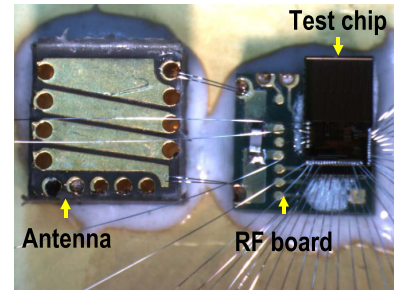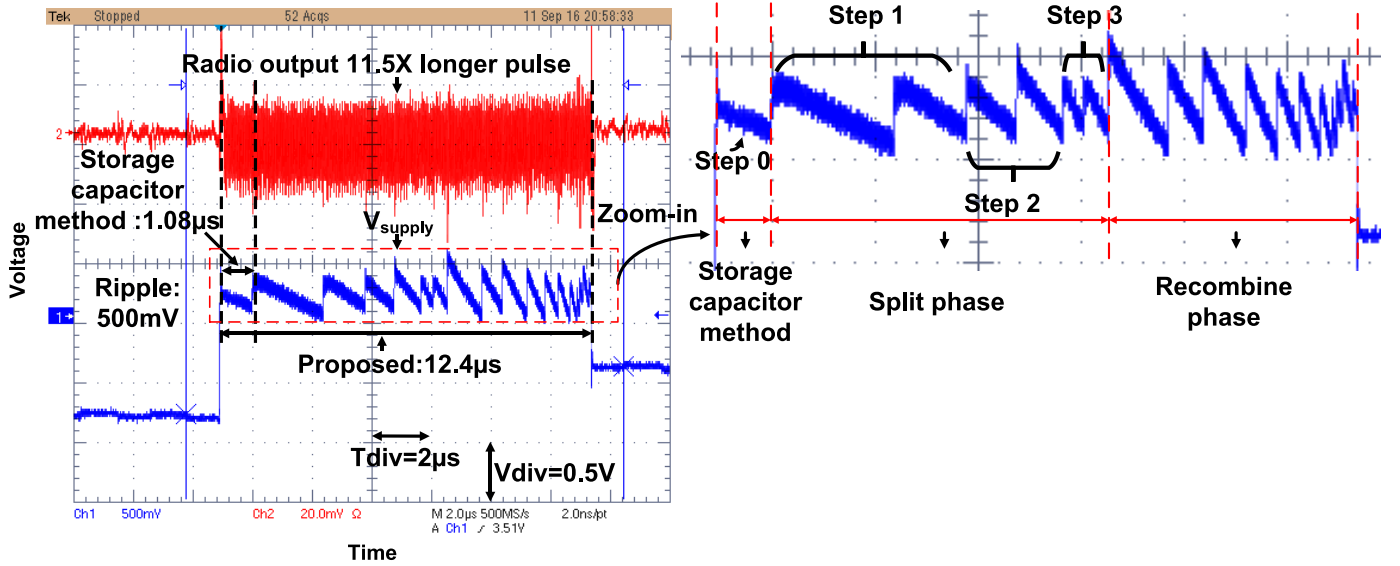
Fig. 26.   Captured transmitter output pulse and supply voltage waveform.

TABLE I

CHIP CHARACTERISTIC SUMMARY

Technology	0.18μm CMOS
Chip area	3.8mm^2
Fully integrated	Yes
Capacitor size	3.15nF
Output power range	45μW – 13.6mW
Control overhead	5.5%
Single shot energy delivered	18.7nJ @ 10% V_{supply} drop

radio power 2 mW and duration of 12.4 μs. The captured supply voltage waveform on the bottom shows supply voltage ramping up at radio power-on. A zoomed-in view of the supply voltage waveform is shown on the right, with each spikes in split phase labeled with step numbers 1–3 corresponding to step $j = 1 - 3$ in Fig. 10. Step 0 is when all capacitors are connected in parallel and discharged by the load as a single capacitor. This corresponds to the conventional single storage capacitor method. For steps 1 and 2, two small spikes are seen in each step because time-spreading technique is used.

Table I summarizes that the proposed reservoir can deliver 18.7 nJ with 10% supply voltage drop.

V. CONCLUSION

In conclusion, we presented an energy reservoir that dynamically reconfigures a storage capacitor array using a so-called counter flow approach for large single shot energy output at high power. The reservoir achieves 45-μW to 13.6-mW output power range and 70% peak single shot energy delivery efficiency with 10% voltage drop (Table I). The proposed method consists of a split phase, where a trapezoid voltage gradient is formed across capacitor arrays, and a recombine phase, where the capacitor arrays are stacked in series and shifted in opposite directions to achieve energy extraction with no charge sharing loss.

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