A 2.2 NEF Neural-Recording Amplifier Using Discrete-Time Parametric Amplification

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Abstract

This paper proposes a 2.2 noise efficiency factor (NEF) instrumentation amplifier for neural recording applications. A parametric amplifier based on the MOS C-V characteristic is designed as a pre-amplifier stage, lowering the input referred noise of the following stages by 3.4×. Sampling noise is minimized by oversampling the input signal and switching power is reduced by adopting an 8-phase soft-charging technique.

Introduction

Neural recording sensor systems require miniaturization to limit brain tissue damage and accommodate tightly spaced electrodes. At the same time, neural potential sensor interface circuits must achieve aggressive input referred noise (IRN) levels to monitor neural signals with sufficient accuracy. Given the small size and close proximity to sensitive brain tissue, power consumption is also highly constrained to meet strict tissue heating limits.

NEF is the typical metric to quantify amplifier noise vs. power efficiency [1] with the goal of achieving low IRN while drawing low current. While some amplifiers [2] have approached the ideal NEF of 1 (i.e., the NEF of a single bipolar junction transistor), neural recording amplifiers tend to have much larger NEF (3−7) because of many other stringent specifications such as: high input impedance, low signal frequency, high common mode rejection ratio, and high power supply rejection ratio [3]. In this work, we propose a new neural recording amplifier that achieves an NEF of 2.2 while meeting the other listed specifications. We use a pre-amplifier stage that performs discrete-time parametric amplification based on MOS C-V characteristics. The sampling-induced *kT/C* noise is minimized by oversampling the input signal. The resulting power overhead is limited with stepwise charging and discharging of the source voltage in the parametric amplifier. Altogether, the design achieves the lowest-reported NEF among neural amplifiers while consuming 5.5uW with 1Hz – 8kHz bandwidth.

Proposed Architecture

Parametric amplification via modulation of capacitance was introduced in [4], and is shown in Fig. 1. The DC gate voltage of the sampling capacitor sets the MOS capacitor in strong inversion during the track phase (V_s = *VDD*). After the input signal is sampled, the source/drain voltage of the sampling p-type transistor is switched from *VDD* to *GND*, increasing the threshold voltage and switching the transistor to depletion mode as shown in Fig. 2. This reduces the gate capacitance, and with the total charge on the capacitor unchanged, a "parametric" amplification of the input signal is achieved. However, sampling operation of the parametric amplifier incurs *kT/C* noise, making it difficult to achieve low IRN. This additional noise overhead can be minimized by oversampling the input signal so that the IRN floor becomes kT/Cf_s. However, this incurs high switching power consumption due to the parasitic capacitance at the source and drain of the sampling capacitor.

To address this issue, we adopt an 8-phase soft-charging technique (Fig. 3, [5]). Instead of driving the source voltage directly to *VDD* or *GND*, the voltage is switched in small steps by charge sharing intermediate capacitors at each step. The intermediate voltages are uniformly self-defined after several cycles of transitions. The switching current is reduced by the number of intermediate stages (N_{int}) as the power supply drives only the last transition from $VDD\times(N_{int}-1)/N_{int}$ *to VDD*. The cost of this approach is additional area for the capacitors, which is about 0.045mm^2. However, this area penalty can be amortized as neural recording front ends are often implemented as an array of large number of channels allowing for the capacitors to be shared.

The IRN of the following amplifier chain is scaled down by the parametric amplifier gain, A_{par}. Therefore, the overall noise efficiency factor improves by adopting the power efficient parametric amplifier at the input stage.

Circuit Implementation

Fig. 4 shows the detailed schematic of the proposed amplifier. A variable gain amplifier (VGA) employs a conventional structure using capacitor ratio and is placed after the low noise amplifier (LNA). The low cutoff frequency of the amplifier chain is determined by the pseudo-resistor that forms a DC servo loop for the VGA. A fast settling path is implemented using pseudo-resistors with lower threshold voltage in order to reduce startup time while retaining a sufficiently large pseudo-resistance during normal operation. An LNA is implemented as an inverter-based input stage to reduce its NEF. LNA gain is defined using gm ratio. Device transconductance is proportional to the bias current when it operates in the subthreshold region. Therefore, LNA gain can be accurately controlled by using the current ratio of 8 to 1. Flicker noise is avoided by chopping at 25kHz. Typically, LNA chopping results in reduced input impedance, which is highly disadvantageous in neural recording applications whose source impedance can exceed 1MΩ [3]. The LNA of the proposed amplifier, on the other hand, can have much smaller input capacitance because its flicker and thermal noise are reduced by A_{par}, thus the measured input impedance is 147MΩ even with amplifier chopping.

Measurement Results

The proposed design was fabricated in 0.18μm CMOS with an area of 0.073mm^2. Fig. 5 shows the measured amplifier transfer function. Amplifier mid-band gain is improved by 3.4× via parametric amplification. Gain of the complete proposed amplifier is configurable from 30 to 60dB. Fig. 7 plots the measured noise spectral density. The input referred noise for the action potential (AP) frequency band (0.3-8kHz) is 2.3μV$_{rms}$ while consuming 5.5μW from 1.2V. Measured IRN for the local field potential (LFP) band (1-500Hz) is 3.4 μV$_{rms}$(0.35μW). Fig. 7 also plots the measured performance metrics of seven samples.

Fig. 8 shows the measured noise characteristic of the proposed amplifier while varying LNA amplifier bias current, I_{amp}, and parametric amplifier sampling frequency, f_s. With a fixed f_s of 1.2MHz, the LNA dominates total noise when I_{amp} is small and the noise eventually saturates at larger I_{amp} when sampling noise starts to dominate (Fig. 8a). Similarly, output noise also decreases as the sampling frequency increases until it saturates to the noise level of the LNA (Fig. 8b). Therefore, optimal NEF is achieved when the noise sources are balanced with each other, as seen in Fig. 8c. Fig. 9 shows a measurement result using previously recorded data with a Utah array chronically implanted in a nonhuman primate and its clustered spikes. Table I summarizes the performance of the design. The parametric amplifier achieves 0.85 NEF in LFP and AP bandwidths. The full proposed design has an NEF of 2.2 in AP mode and 3.1 in LFP mode while achieving competitive common-mode and power supply rejection ratios of >70 dB. Fig. 10 provides a die photo of the design.

References

[1] M. S. J. Steyaert et al., JSSC, Dec. 1987.
[2] L. Shen et al., VLISC, 2017. [3] H. Chandrakumar et al., JSSC, 2017.
[4] S. Ranganathan et al., ISSCC, 2003. [5] N. Butzen et al., JSSC, 2017.

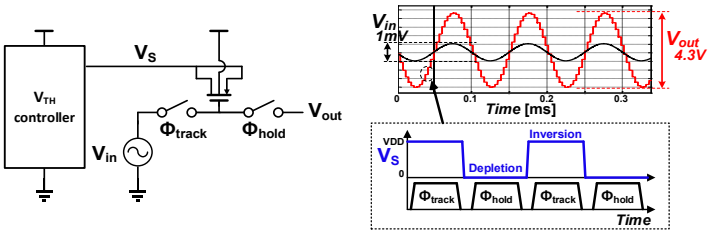


Fig. 1. (a) A schematic of a PMOS discrete-time parametric amplifier. (b) Input (V_{in}), output (V_{out}) and control signals of the parametric amplifier.

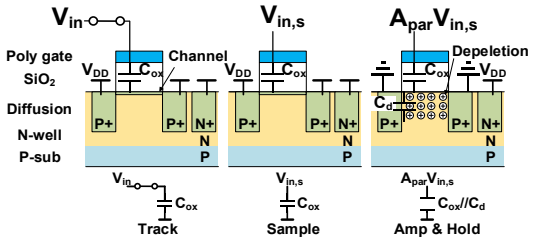


Fig. 2. Cross section view of the PMOS transistor in tracking, sampling and amplification modes.

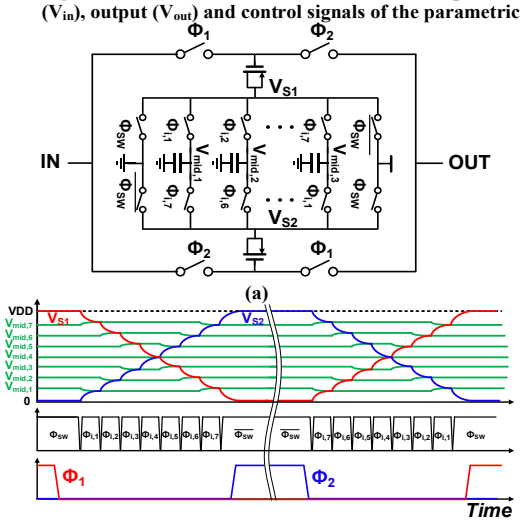


Fig. 3. (a) Schematic and (b) Waveforms of the proposed parametric amplifier with the 8-phase soft-charging technique.

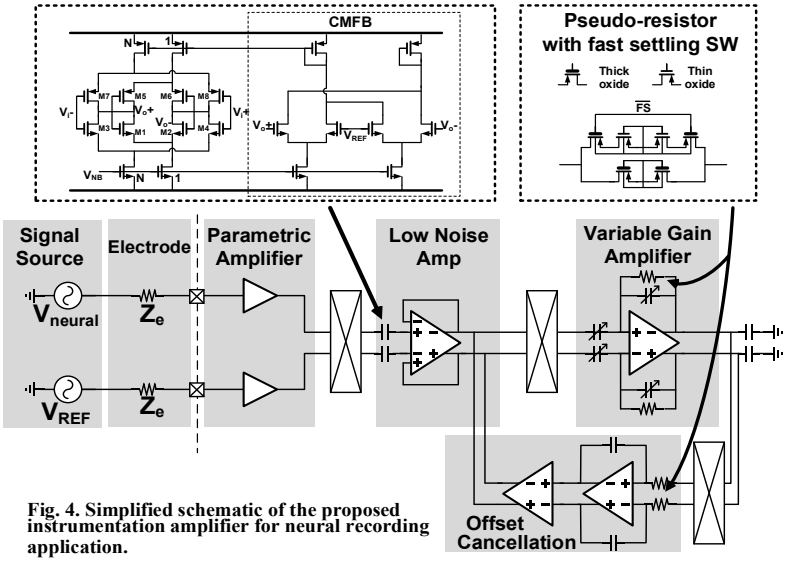


Fig. 4. Simplified schematic of the proposed instrumentation amplifier for neural recording application.

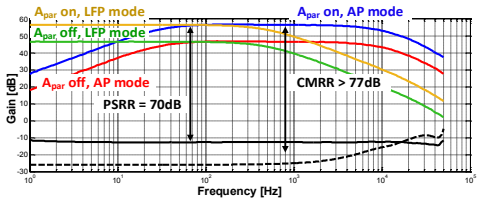


Fig. 5. Measured transfer function of the proposed amplifier plotted with its CMRR and PSRR.

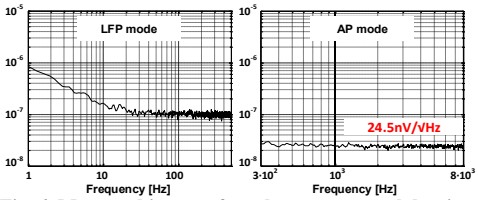


Fig. 6. Measured input referred power spectral density from 1 to 10kHz.

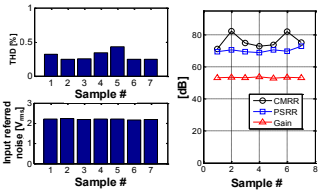
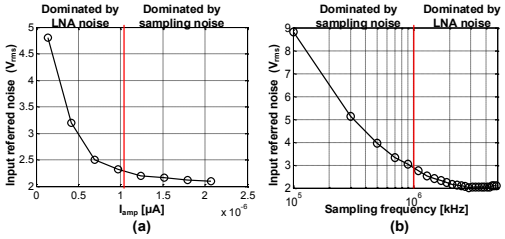


Fig. 7. Measured THD ($2mV_{pp}$), IRN, CMRR, PSRR and gain of 7 samples.



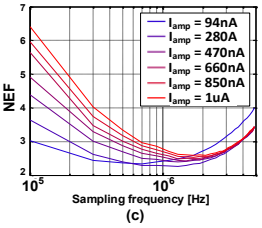


Fig. 8. Measured input referred noise in AP bandwidth and NEF while varying the sampling frequency and the amplifier bias current.

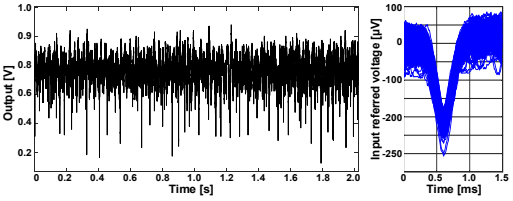


Fig. 9. In-vivo measurement (repeated with previously recorded data) and the time-aligned spikes.

Table I. Performance summary and comparison

	This work		Ng, ISSCC2015	Muller, ISSCC2014	Chandrakumar, ISSCC2016	Chandrakumar, ISSCC2017	Lopez, JSSC2014
Power (μW)	5.5		2.8	2.8	2	2.8	7.02
Input referred Noise (μV_{rms})	AP: 2.3 LFP: 3.4		4.13	1.3	AP: 7 LFP: 2	AP: 5.2 LFP: 1.8	AP: 3.2 LFP: 5.8
Bandwidth (Hz)	1-8000		1-8200	1-500	1-5000	1-5000	0.5-6000
NEF	Parametric Amp	0.85	2.93	4.76	AP: 4.9 LFP: 7	AP: 4.4 LFP: 7.4	AP: 3.08
	Total Amp. front-end	AP: 2.2 LFP: 3.1					
Gain (dB)	30-60		57.8	-	26	25.7	30-72
Signal type	AP+LFP		AP+LFP	LFP	AP+LFP	AP+LFP	AP+LFP
Input common mode range (mV_{pp})	100		200	-	40	40	-
Input impedance (MΩ)	147		-	28	300	1600	-
PSRR (dB)	> 70		78	-	-	-	70
CMRR (dB)	> 70		> 80	-	-	-	60
THD	1% ($5mV_{pp}$)		-	-	-74 dB	-76 dB	1% ($18mV_{pp}$)
Size (mm^2)	0.071		0.042	0.025	0.071	0.069	0.088[1]
Technology	0.18μm		65nm	65nm	40nm	65nm	0.18μm

[1] Estimated

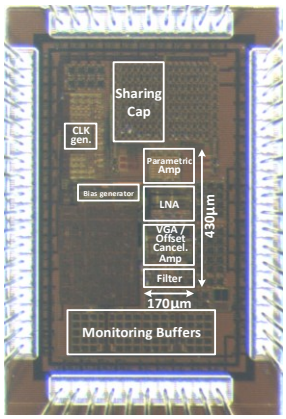


Fig. 10. Die photograph.