A 224 pW 260 ppm/°C Gate-Leakage-based Timer for Ultra-Low Power Sensor Nodes with Second-Order Temperature Dependency Cancellation

Jongyul Lim, Taekwang Jung, Mehdi Saliganeh, Makoto Yasuda¹, Satoru Miyoshi², Masanu Kawaminami¹², David Blaauw, Dennis Sylvester
University of Michigan, MI; ¹Mie Fujitsu Semiconductor Limited, Japan; ²Fujitsu Electronics America, CA

Abstract
A key challenge in the design of on-chip wake-up timers for compact wireless sensor nodes is to achieve high timing accuracy over temperature and supply voltage variation within an ultra-low power budget. We propose a gate-leakage-based frequency-locked timer with first- and second-order cancellation achieving 260 ppm/°C from −5 to 95°C. The timer consumes 224 pW at 90 Hz output frequency with 0.93%/V supply voltage dependence in the 1.1-3.3 V range.

Introduction
Wake-up timers are a critical component of wireless sensor nodes (WSNs) for the Internet of Things. Since they are on even when the sensor node is in sleep mode, they must consume extremely low power. In addition, they should ensure high timing accuracy for synchronization between devices and general timekeeping while remaining compact, leading to a highly constrained design space. An RC oscillator [1] or frequency-locked oscillator [2] based on temperature-compensated resistors achieves frequency stability across temperature of <50 ppm/°C. However, these approaches consume ~100 nW or more, which far exceeds the power budget of state-of-the-art ultra-low-power sensors. Extending these approaches to sub-nW requires extremely large resistors, unacceptably increasing the area and cost. Recently, a switch-resistor based timer achieved a high effective resistance without increasing resistor size and obtained a temperature coefficient (TC) of 13.8 ppm/°C [3]. However, the approach requires large capacitors, and power consumption remains relatively high at 4.7 nW. An alternative to resistor-based timers is gate-leakage-based timers; several such timers have been proposed [4-5], providing sub-nW power consumption in compact silicon area. However, gate leakage exhibits significant first- and second-order temperature dependence, complicating temperature compensation, and it is also sensitive to the gate voltage. As a result, previous gate leakage timers have TCs in excess of several hundred ppm/°C and line sensitivities (LS) >150%/V. The gate leakage timer in [5] achieves 31 ppm/°C but requires 10-point calibration, and its 660 pW power consumption does not include the power of a required auxiliary temperature sensor. Further, its LS is unacceptably high at 420%/V.

This paper proposes a 224-pW gate-leakage-based frequency locked timer with first- and second-order temperature dependency cancellation, yielding a TC of 260 ppm/°C across −5 to 95°C. Supply insensitive reference voltage generators and an on-chip low dropout (LDO) regulator decrease LS to 0.93%/V for 1.1–3.3 V, which marks a 150× improvement compared to previous gate-leakage-based timers.

Proposed Circuit
The proposed design uses a frequency locked oscillator scheme [2,3] in which current I₁, set by the gate leakage of a standard-Vth NMOS N₁, is matched with current I₂, using modulation of the frequency of a switched capacitor C₂ (Fig. 1). The measured temperature dependence of N₁ gate leakage shows both first- and second-order components (Fig. 2). It is essential to cancel both components to achieve a good TC. In the proposed design, we use two tuning mechanisms. We cancel the first-order dependence by varying V₁ in a proportional to temperature (PTAT) fashion using a voltage reference with tunable temperature dependence (Fig. 1, right). This PTAT reference consists of two PMOS diode stacks, each with different threshold voltages and sizes to create a first-order dependence on temperature (Fig. 3b). Switches control the high-Vt PMOS size, which tunes the slope of V̇PTAT from 0.5 to 0.68%/°C (simulation).

To cancel the second-order dependence, we use a 2T voltage reference, which has intrinsic convex temperature dependence [6] (Fig. 3a). However, the convexity of this reference is fixed and is not easily tuned to cancel the second-order dependence of gate leakage. Hence, we leverage the exponential dependence of gate leakage on voltage to provide this tuning mechanism, as follows: First, we remove first-order dependence by tuning the native NMOS and High-Vt PMOS sizes, resulting in V₂ₓ = Vₓ0(α(T−T₀)²). We then amplify V₂T, and a mux structure selects the output voltage V̇REF = V₁ = kmax(V₂T,αT−T₀²) where kmax varies with the mux selection. Note that this does not change the relative magnitude of the convexity of V₁. However, gate leakage I₁ is exponentially dependent on V₁, resulting in I₁ ≈ exp(kₐ₁V₂T₁α)exp(kₐ₁α(T−T₀)²). Hence, by changing kₐ₁ (i.e., the mux setting) we can modulate the relative magnitude of the convexity of I₁, which allows us to cancel the second-order temperature dependence of the gate leakage. Fig. 3c shows simulation results of this approach. After both first- and second-order temperature dependencies are canceled, only third- and higher-order terms remain. Finally, the center frequency (0th order) is adjusted by tuning C₂ in Fig. 1.

Two PMOS devices (P₁ and P₂, Fig. 1) implement the current mirror. The devices are high threshold thick-oxide PMOS transistors operating in subthreshold with V_DS > 5 kT/q, which significantly reduces mismatch between I₁ and I₂. The low power voltage controlled oscillator (VCO) in Fig. 1 provides the timer’s output frequency and is composed of stacked high threshold inverters to minimize short circuit current (Fig. 4). The voltage range of VCTRL across temperature, 0.67–0.9 V, is too narrow and situated at too high a voltage to compensate the VCO frequency across temperature. We double the voltage range and shift it lower using switch capacitor C₃, obtaining VCTRL with range 0.2–0.65 V. Capacitors C₃–C₅ also generate the dominant pole of the frequency lock scheme.

Gate leakage has high voltage sensitivity, leading to strong frequency dependence on supply voltage in previous gate-leakage-based timers. The proposed design addresses this by placing native NMOS transistors in the convex voltage generator and PTAT voltage generator, enabling low line sensitivity (1.3%/V and 2.2%/V, respectively, simulation). An on-chip LDO further reduces supply voltage dependence while consuming only 18 pW (simulation).

Measurements
The proposed gate-leakage-based timer was implemented in 55nm CMOS (MIFS C55DDC) in 0.057 mm². Fig. 5 shows the measured frequency variation from −5 to 95°C for five typical corner dies. Fig. 5a gives results with no tuning, while Fig. 5b has 2-pt calibration to cancel first-order dependence. Fig. 5c uses the proposed second-order cancelation with 3-pt calibration, yielding measured TCs of 175–343 ppm/°C, which is 5× better than first-order cancelation only. The timer consumes 224 pW at 25°C with 90 Hz output frequency; power increases to 1.2 nW at 95°C (Fig. 8). Line sensitivity is 0.33–1.29%/V across 1.1–3.3 V supply voltage for the five dies (Fig. 6). Fig. 11 compares TC, LS, and energy per cycle to those of previous sub-nW timers and resistor-based timers. The proposed timer is Pareto optimal in terms of TC and LS vs. power among the listed works, enabling a new ultra-low power timer design space. Energy per cycle of 2.49 pJ/cycle is comparable to the best reported among the listed works.

References
Fig. 1. Proposed gate leakage based frequency locked timer.

Fig. 2. Measured gate leakage current across temperature in 55nm CMOS.

Fig. 3. (a) Proposed convex voltage generator (b) PTAT voltage generator and (c) simulation result of first- and second-order cancellation.

Fig. 4. Diagram of stacked inverter VCO with switch capacitor voltage doubler.

Fig. 5. Measured frequency variation over temperature: (a) without calibration (b) with 2-pt and (c) with 3-pt calibration.

Fig. 6. Measured line sensitivity of output clock frequency.

Fig. 7. Simulated power breakdown of timer

Fig. 8. Measured power consumption

Fig. 9. Measured Allan deviation

Fig. 10. Die photo.

Fig. 11. Comparison scatter plots with previous work (best reported dies): (a) temperature coefficient (b) line sensitivity and (c) energy per cycle

Table 1. Comparison table

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage [V]</td>
<td>1.2</td>
<td>1.8/0.5</td>
<td>0.5</td>
<td>0.7/1.2</td>
<td>0.6</td>
<td>0.45</td>
</tr>
<tr>
<td>Power [mW]</td>
<td>38/42</td>
<td>50/42</td>
<td>66*</td>
<td>150</td>
<td>120</td>
<td></td>
</tr>
<tr>
<td>Frequency [GHz]</td>
<td>90</td>
<td>18</td>
<td>2.8</td>
<td>6</td>
<td>11</td>
<td>0.08</td>
</tr>
<tr>
<td>Temp. Coeff. (ppm/°C)</td>
<td>175-343</td>
<td>8500</td>
<td>2000</td>
<td>1500</td>
<td>375</td>
<td>31(1)</td>
</tr>
<tr>
<td>Temp. Range [°C]</td>
<td>-5 ~ 95</td>
<td>30 ~ 60</td>
<td>60 ~ 80</td>
<td>60 ~ 90</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>Line Sensitivity [%V/°C]</td>
<td>-1.15</td>
<td>0.62</td>
<td>0.05</td>
<td>0.10</td>
<td>0.20</td>
<td>0.30</td>
</tr>
<tr>
<td>Energy [pJ/cycle]</td>
<td>2.49</td>
<td>2.1</td>
<td>2.0/0.25</td>
<td>15.8</td>
<td>110</td>
<td>13.6</td>
</tr>
<tr>
<td>Area [mm²]</td>
<td>0.057</td>
<td>0.18</td>
<td>0.026</td>
<td>0.015</td>
<td>0.02</td>
<td>0.0005</td>
</tr>
</tbody>
</table>

a. Average over multiple samples
b. Calculated from Fig. 5
c. Power consumption without a temperature sensor
d. 10 point calibration with a temperature sensor