A Reference Oversampling Digital Phase-Locked Loop with −240 dB FOM and −80 dBc Reference Spur

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Abstract

This paper proposes a reference oversampling phase-locked loop that simultaneously suppresses in-band noise and oscillator noise while maintaining a low reference spur. The proposed phase locked loop achieves −240.3 dB Figure of Merit (FOM) and −80 dBc reference spur. The integrated jitter is 508 fs_{rms} and the power consumption is 3.6 mW at 2 GHz output clock frequency.

Introduction

Inductor-less phase locked loops (PLLs) offer many advantages over LC designs, such as smaller area, wider frequency range, and less frequency pulling [1]. However, designing a low-noise PLL using a ring oscillator is challenging due to the high oscillator noise and the stability requirement of a PLL, which limits the maximum loop bandwidth to 1/10 of the reference frequency, making it difficult to filter out oscillator noise effectively. Furthermore, simultaneous suppression of various noise sources, such as the reference, time-to-digital converter, charge-pump, loop filter and oscillator, introduces conflicting requirements. Consequently, the oscillator noise sometimes is not filtered at the maximum bandwidth.

Multiplying delay-locked loops (MDLL) and injection-locked clock multipliers (ILCM) have shown promising noise performance by increasing the loop bandwidth by up to half of the reference frequency [2, 3]. However, because they inject the reference directly into the oscillator, they inevitably produce large spurs at the output.

This paper introduces a reference oversampling PLL (OSPLL) that can fundamentally overcome the bandwidth constraint of a PLL. The loop bandwidth can be configured to be even higher than the reference frequency so that the ring oscillator noise is effectively suppressed without the penalty of a high reference spur. Furthermore, the in-band noise can also be reduced drastically as the effective input frequency is multiplied by a factor of N, where N is the PLL frequency multiplication ratio. The 28 nm prototype design consuming 3.6 mW achieved 508 fs_{rms} jitter, −80 dBc reference spur, and −240.3 dB jitter-power figure of merit (FOM) at 2 GHz output frequency.

Proposed PLL

Fig. 1 illustrates the operating principle of the proposed OSPLL. A 50 MHz sinusoidal reference CLKREF is directly connected to an array of reference sampling phase detectors (RSPDs) without a reference buffer. A multiphase generator drives the RSPDs using time-interleaved clocks, Φ1:N, generated by retiming a division of the digitally-controlled oscillator (DCO) output so that the frequency of Φi is 50MHz and each Φi is spaced by one DCO period from another. As the N time-interleaved RSPDs operate sequentially in time within a reference period, the effective sampling rate for the sinusoidal reference clock is the output frequency (CLKOUT). Therefore, the in-band noise of the PLL is greatly suppressed, and at the same time, the PLL loop bandwidth can be extended up to 1/10th of CLKOUT. Each RSPD generates a single-bit output, PDOUT, indicating the phase of CLKOUT is either leading or lagging the phase of the input. Then, each PDOUT<i> is multiplied by its proportional gain, P_{GAIN}<i>, and fed to a DCO, which forms a bang-bang phase-locked loop operating at every DCO cycle. The integral path of the PLL is designed by using one of the PDOUTs.

Fig. 2 explains the detailed operation of the RSPD. CLKREF is sampled onto C_S at the falling edge of Φi and transferred to a comparator input, V_{SMPL}, through an AC coupling capacitor, C_C, while its DC is defined at V_{CM} through a large resistor, R_B. A voltage difference between V_{SMPL} and V_{CM} indicates the output phase error while their DC value is equal to V_{CM}. The polarity of V_{SMPL}-V_{REF} is sensed by a comparator clocked by Φ_{COMPi} whose input offset is cancelled by a charge pump that asserts the voltage of V_{OC} such that PDOUT has equal probability of 1s and 0s. Note that RSPDs with an AC coupling capacitor only sense the AC fluctuation of the phase error. Therefore, one of the 40 RSPDs is designed without a C_C so it can provide the *pivot* position of the phase locking at the positive zero crossing point of CLKREF, while the sampling points of the other RSPDs are defined relative to the pivot position.

The intrinsic noise of an RSPD consists of sampling noise, kT/C_S, and comparator noise, and is the same for every RSPD. On the other hand, the signal of each RSPD, which is the phase error, is dependent on the slope of CLKREF at the point that it samples. For instance, RSPD<3> in Fig. 2 samples CLKREF close to its peak point so its output is mostly driven by RSPD noise rather than the phase error. Therefore, the RSPD outputs that sample at steeper points of CLKREF must be emphasized compared to RSPD outputs that sample CLKREF near its peak points. Also, the RSPD outputs that sample CLKREF during its negative slope need to be multiplied by −1. The proportional gain, P_{GAIN}<1:40>, is set to be quadrature to the input phase to meet the aforementioned two criteria, as shown in Fig. 2.

Fig. 3 provides a detailed block diagram of the proposed architecture. In the startup phase, a conventional bang-bang PLL is enabled to lock the output to the target frequency. Then, the startup PLL is disabled, and the outputs of the proposed RSPD, PDOUT<1:40>, are converted to UP or DN pulses. Each pulse drives DCO for 1 DCO cycle through a PDAC, suppressing the oscillator noise at every DCO cycle. This oscillator noise suppression is done without directly injecting the reference to the oscillator as with MDLLs or ILCMs, minimizing the reference spur. Only PDOUT<1> is connected to the integral path to lower the complexity. The multiphase generator produces 40 time-interleaved clocks using CLKOUT, as shown in the bottom of Fig. 3. It forms a closed chain of 40 unit cells, each of which is composed of a flip-flop (FF) and clock-gating logic. A bypass mux is also included in each unit cell to provide programmability of the frequency division ratio. Initially one half of the units, U<1:20>, are set to 1 while the other half, U<21:40>, are set to 0. Then, the pre-assigned signals propagate in one direction of the chain at every rising edge of CLKOUT. The FF clock is gated when the input and output of the FF are both 0 to save 30% of the multiphase generator power.

Fig. 4 illustrates the structure of the DCO, which is composed of pseudo-differential delay cells and current DACs including a 3-bit current steering DAC for each RSPD to program a proper P_{GAIN}. UP and DN connections are swapped for the negative P_{GAIN}'s. Note that a dummy current path with a unity gain amplifier is used to ensure accurate current steering while UP and DN pulses are toggling.

Measurements

The proposed PLL was fabricated in a 28 nm CMOS process and occupies 0.07 mm^2. The design consumes 3.6 mW and achieves 508 fs_{rms} integrated jitter at 2 GHz, as shown in Fig. 5. Compared to the conventional bang-bang mode, the in-band noise is reduced by oversampling the reference, and the DCO noise is minimized by extending the loop bandwidth. The reference spur is measured at −80 dBc (Fig. 6). Fig. 7 compares the measurement results of the proposed PLL with recently published inductor-less integer-N frequency synthesizers. With the reference oversampling technique, the proposed PLL achieves appealing jitter performance, FOM, and a low reference spur while eliminating the need for a power hungry reference buffer by directly using the sinusoidal input [4]. Table I summarizes the performance of the proposed OSPLL relative to state-of-the-art designs, and Fig. 8 shows the die photo.

References

[1] L. Kong *et al.*, ISSCC, 2015. [2] H. Kim *et al.*, ISSCC, 2016.
[3] D. Coombs *et al.*, ISSCC, 2017. [4] J. Sharma *et al.*, ISSCC, 2018.

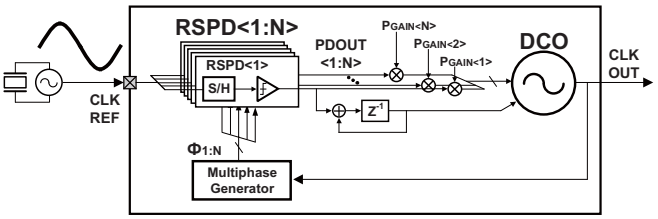

Fig. 1. Conceptual diagram of the proposed OSPLL.

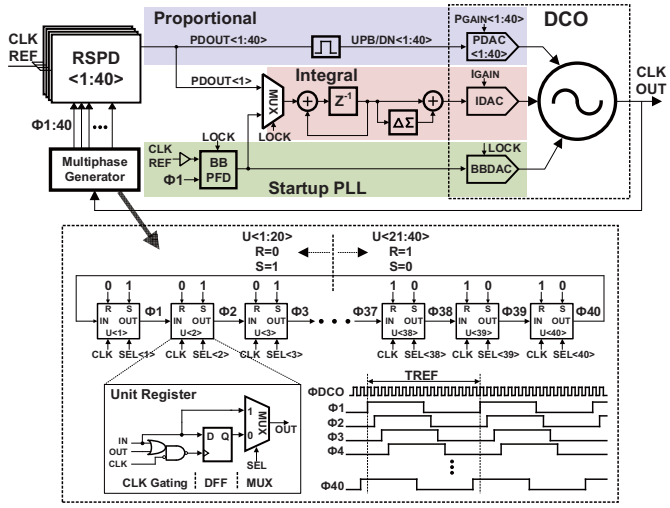

Fig. 3. Detailed schematic of the proposed OSPLL and the multiphase generator

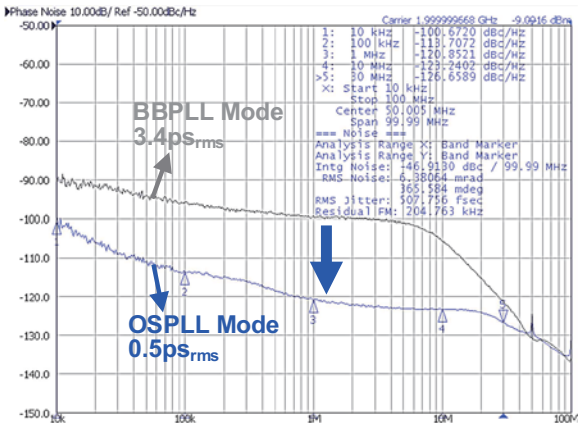

Fig. 5. Measured phase noise.

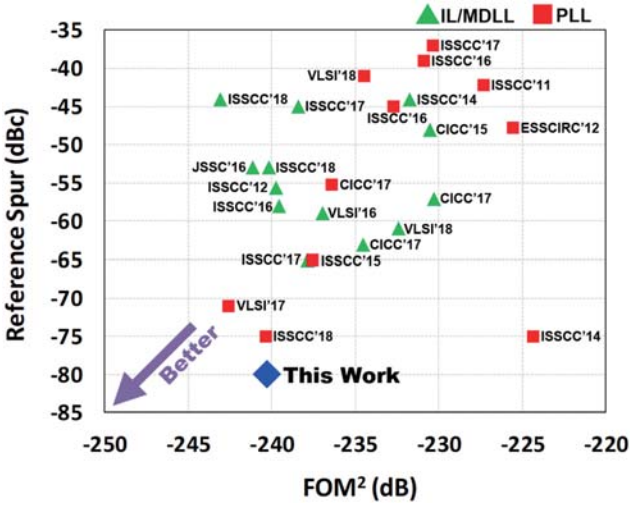

Fig. 7. Spur vs. FOM² of ring oscillator based integer-N synthesizers

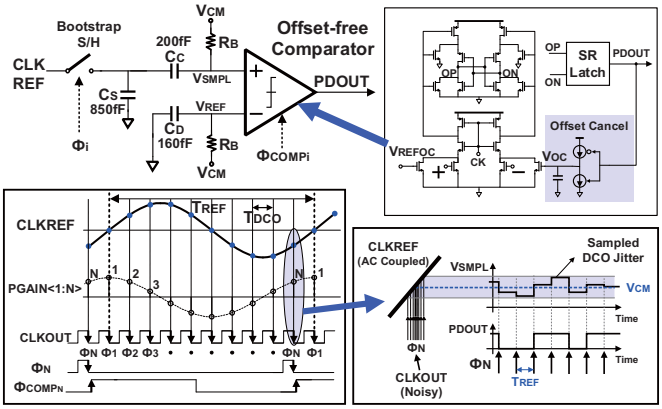

Fig. 2. Schematic and operation principle of the reference sampling phase detector (RSPD).

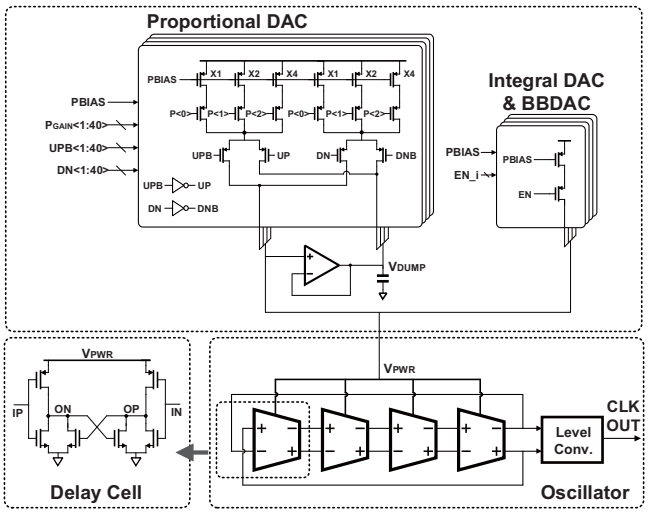

Fig. 4. Schematic of DCO of the proposed OSPLL.

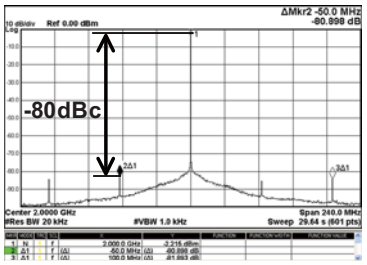

Fig. 6. Measured spectrum and the reference spur.

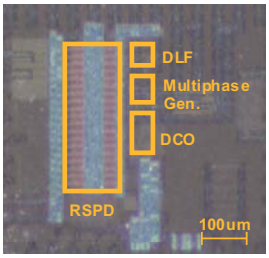

Fig. 8. Die photograph.

Table I. Comparison with recent ring oscillator based integer-N synthesizers

	This Work	Tsai, VLSI18	Seong, ISSCC18	Kuan, VLSI18	Megawer, ISSCC18	Yang, ISSCC18
Type	OSPLL	PLL	PLL	ILPLL	ILCM	MDLL
Output Frequency (GHz)	2.0	3.0	2.4	4.0	4.752	3.0
Reference Frequency (MHz)	50	200	75	250	54	200
Phase Noise @1MHz (dBc/Hz)	-120.8	-119.0	-119.8	-119.0	-113.71	-118.0
Integrated RMS Jitter (ps)	0.508 (10K-100M)	0.619 (100K-1G)	0.32 (1K-100M)	0.427 (100K-1G)	0.366 (10K-30M)	0.292 (10K-40M)
Power (mW)	3.6	2.3	6.0	6.3	6.5	1.45
*FOM[1] (dB)	-240.3	-240.5	-242.1	-239.4	-240.5	-249.1
**FOM[2] (dB)	-240.3	-234.5	-240.3	-232.4	-240.2	-243.1
Reference Spur (dBc)	-80	-52 ~ -41	-75	-61	-53	-44
Area (mm²)	0.07	0.012	0.055	0.018	0.16	0.0056
Technology	28nm	7nm	65nm	7nm	65nm	28nm

$*FOM^1 = 10log\left[\left(\frac{\sigma_{rms}}{1sec}\right)^2 \cdot \left(\frac{Power}{1mW}\right)\right]$ $**FOM^2 = 10log\left[\left(\frac{\sigma_{rms}}{1sec}\right)^2 \cdot \left(\frac{Power}{1mW}\right) \cdot \left(\frac{F_{REF}}{50MHz}\right)\right]$