Xiao Wu

1301 Beal Ave., Ann Arbor, MI, USA 48105 (734)-604-7560 lydiaxia@umich.edu

AEAS OF INTEREST

Hardware accelerator Energy harvester Power management circuits IoT system integration

EDUCATION

University of Michigan Ann Arbor, USA

- Ph.D. Student in Electrical Engineering with Prof. David Blaauw Sep. 2016 -May 2019
- M.S. in Electrical Engineering, major G.P.A. 3.89/4.0 May 2016
- B.S.E. Electrical and Computer Engineering, major G.P.A. 4.0/4.0 May. 2014

Shanghai Jiaotong University Shanghai, China

- B.S.E., Electrical and Computer Engineering Aug. 2014

RESEARCH PROJECTS

A 0.04mm^3 (500x smaller than rice) wireless sensor system for inter-cellular temperature measurement

- Designed and integrated in the system: Cortex-M0+ processor, a sub-threshold oscillation-based temperature sensor, optical tranceiver including LED driver and modulation/demodulation circuits, and custom SRAM.
- Taped out in 55nm and integrated the complete 2-layer sensor system, preparing for implantation.
- Measured system operation shows successful wireless programming, accurate temperature measurement with 0.034°C RMS noise resolution, transmission of temperature code and demodulation of correct packet at base station from 15.6cm away.

A fully integrated counter flow energy reservoir for small form-factor sensor systems

- Designed a fully integrated energy reservoir unit that dynamically reconfigures a storage capacitor array using a so-called "countercurrent flow" approach, achieving 11.5× increase in energy delivery to high power loads (e.g. radio) in small battery-powered systems, compared to conventional method.
- Taped out in 180nm CMOS. The energy reservoir achieves efficient (65%) of the stored energy to the load and supplies up to 13.6mW output power.

A 66pW discontinuous switch-capacitor energy harvester for sensor applications

- Designed a discontinuous harvester with moving-sum charge pump for low startup energy, an automatic conversion ratio modulator and a 15pW asynchronous mode controller.
- Taped out in 180nm. The harvester achieves >40% end-to-end efficiency from 113pW to 1.5µW with 66pW minimum input power, marking a >10x improvement over prior ultra-low power harvesters.

A hardware accelerator for PairHMM calculation in DNA sequencing

- Designed pruning-based PairHMM algorithm with a data magnitude estimator, a pruner to reduce required floating point calculation and therefore increase throughput by 10×, and a monitor to guarantee result accuracy.
- Taping out in 40nm CMOS the corresponding hardware accelerator with fixed and floating point PairHMM PE arrays, and an on-demand memory scheduler for workload balancing.

COURSE PROJECTS

AES engine: an energy efficient AES accelerator using charge sharing dynamic logic gates (UM, 14)

Amplifier: a low power multi-stage amplifier with local-feedback enhancement compensation (UM, 14)

Processor: a 2-way superscalar out-of-order processor with early branch resolution and load-store queue (UM, 13)

SRAM: custom SRAM with dynamic voltage scaling using canary circuit, and error correction code. (UM, 13)

PUBLICATIONS

X. Wu, et.al, "A 66pW Discontinuous Switch-Capacitor Energy Harvester for Self-Sustaining Sensor Application," *IEEE Symposium on VLSI Circuits (VLSI-Circuits)*, June 2016

X. Wu, et.al, "A 20pW Discontinuous Switched-Capacitor Energy Harvester for Smart Sensor Applications," *IEEE Journal of Solid State Circuits (JSSC), Invited Paper to the Special Issue on VLSI 2016*

X. Wu, et.al, "A Fully Integrated Counter Flow Energy Reservoir for 70% Efficient Peak-Power Delivery in Ultra-Low-Power Systems," *IEEE International Solid-State Circuits Conference (ISSCC),2017*

X. Wu, et.al, "A Fully Integrated Counter Flow Energy Reservoir for Peak Power Delivery in Small Form-Factor Sensor Systems," *IEEE Journal of Solid State Circuits (JSSC), Invited paper to the Special issue on ISSCC 2017*

X. Wu, et.al, "A 0.04mm^3 16nW Wireless and Batteryless Sensor System with Integrated Cortex-M0+ Processor and Optical Communication for Cellular Temperature Measurement," *IEEE Symposium on VLSI Circuits (VLSI-Circuits)*, *June 2018*

EXPERIENCE

Apple Inc. Cupertino, USA

Intern, SEG-Power Circuit & Tech July – Sep.,2018

- Proposed and evaluated low power architectures for on-chip power management units to reduce leakage power of deep submicron SoC.
- Co-designed power regulation unit with low power amplifier, comparator, charge pump and voltage detector, and verified its robustness across required process, voltage and temperature range.
- Automated circuit sizing and design verification with Python.

University of Michigan Ann Arbor, USA

Graduate Student Instructor, VLSI Design II Jan.-May,2018

- Taught weekly discussion sessions, evaluated group projects and helped prepare exam.

AWARDS

1st prize, AMD Design contest – EECS427 VLSI Design (UM, 13). James B. Angell Scholar (UM, 14)

SKILLS

Cadence Virtuoso, Innovus/Encounter, Design compiler, Verilog HDL, Liberate, HSPICE, CustomSim, LabVIEW, Altium Designer, C/C++, Matlab, Perl, Python.