Jihwan Seol

Windwood Dr., Ann Arbor, MI, 48105
Phone: 734-882-9117 E-mail: jhseol@umich.edu

Education

- **University of Michigan, Ann Arbor** USA

  Ph.D. in Electrical Engineering and Computer Science *Sep. 2017 - Present*

  - Advisor: Prof. David Blaauw & Dennis Sylvester

- **KAIST (Korea Advanced Institute of Science and Technology)** South Korea

  M.S. in Electrical Engineering *Feb. 2010 - Feb.2012*

  - Advisor: Prof. Lee-Sup Kim
  - GPA: 3.51/4.0 Overall
  - Thesis: A Low Power Injection Locked Oscillator for a Forwarded Clock Receiver

- **Yonsei University** South Korea

  B.S. in Electrical and Electronic Engineering *Mar. 2003 - Aug.2009*

  - GPA: 3.81/4.0 Overall, 3.91/4.0 Upper
  - Thesis: A Low Power Area Efficient 90 Degree Shift Delay Locked Loop for DDR Interface, under the supervision of Prof. Seong-Ook Jung

Work Experience

- **DRAM Design Team, Memory Business, Samsung Electronics** South Korea

  Senior Engineer *Mar. 2016 - Present*

  - LPDDR3, LPDDR5
    - Core/Peripheral Circuits for Active-Precharge Path
      - Command Decoder, Row Address Path, Row Decoder, Row Repair Circuits
      - Bit-line Sense Amplifiers, Sensing Control Circuits
    - High Speed IO Circuits for LPDDR5

  Engineer *Mar. 2014 - Feb. 2016*

  - LPDDR2, LPDDR4
    - Novel Bit-line Sense Amplifiers
      - Offset Cancellation Type Bit-line Sense Amplifiers for Mass Production
    - Core/Peripheral Circuits for Active-Precharge Functions
      - Command Decoder, Row Address Path, Bit-line Sense Amplifiers
      - Voltage Regulators for Bit-line Sensing Operation
    - On-chip Temperature Sensors
    - Temperature Compensated Self Refresh and Auto Refresh Control Circuits/Functions
    - Voltage Generators (Reference Generators, LDOs, Charge Pumps for High Voltage)

Assistant Engineer *Mar. 2012 - Feb. 2014*

- LPDDR2, LPDDR3
  - On-chip Temperature Sensors
  - Temperature Compensated Self Refresh and Auto Refresh Control Circuits/Functions

Research Experience

- **Michigan Integrated Circuit Laboratory, University of Michigan** *Sep. 2017 – Present*
  - Ultra wide bandwidth and low spur ring oscillator based phase-locked loop
    - Accepted/Presented in VLSI 2019 as a 1st author
  - Ultra low jitter and low spur LC oscillator based phase-locked loop
- **MVLSI Laboratory, KAIST** *Feb. 2010 - Feb.2012*
  - Researched High-speed Low-power Forwarded Clock Transceivers
  - Researched Injection Locked Oscillators for Jitter filtering and de-skew
  - Designed and Tape-out a forwarded clock receiver using an Injection Locked Oscillator
    - Accepted/Presented in ISSCC 2013 as a 1st author
- **VLSI System Laboratory, Yonsei University** *Feb. 2009 - Jun. 2009*
  - Researched Delay locked loops for DRAM interface
  - Designed a 90 degree shift delay locked loop for DDR DRAM interface
    - Issued a patent in South Korea

Publications

- **Ji-Hwan Seol** ; Dennis Sylvester ; David Blaauw ; Taekwang Jang "A Reference Oversampling Digital Phase-Locked Loop with -240 dB FOM and -80 dBc Reference Spur" 2019 Symposium on VLSI Circuits (VLSI)
- Kyojin David Choo ; Li Xu ; Yejoong Kim ; **Ji-Hwan Seol** ; Xiao Wu ; Dennis Sylvester ; David Blaauw "Energy-Efficient Motion-Triggered IoT CMOS Image Sensor With Capacitor Array-Assisted Charge-Injection SAR ADC", 2019 IEEE Journal of Solid-State Circuits (JSSC)
- Kyojin D. Choo ; Li Xu ; Yejoong Kim ; **Ji-Hwan Seol** ; Xiao Wu ; Dennis Sylvester ; David Blaauw "Energy-Efficient Low-Noise CMOS Image Sensor with Capacitor Array-Assisted Charge-Injection SAR ADC for Motion-Triggered Low-Power IoT Applications", 2019 IEEE International Solid-State Circuits Conference (ISSCC)
- **Ji-Hwan Seol** ; Young-Ju Kim ; Sang-Hye Chung ; Kyoung-Soo Ha ; Seung-Jun Bae ; Jung-Bae Lee ; Joo Sun Choi ; Lee-Sup Kim "An 8Gb/s 0.65mW/Gb/s forwarded-clock receiver using an ILO with dual feedback loop and quadrature injection scheme", 2013 IEEE International Solid-State Circuits Conference (ISSCC)

Patents

- Seong-Ook Jung; Kyung-Ho Ryu; Dong-Hun Jung; **Ji-Hwan Seol**
  "Delay Locked Loop and Duty Cycle Correction Circuit Thereof", issued in South Korea
  (Patent number: 101027759)

Military Service

- **KATUSA (Korean Augmentation to the United States Army)** South Korea

Sergeant, Battery Head Quarter, 6-37 FA, 8th U.S. Army *Oct. 2005 - Oct. 2007*

- Section chief of the battery head quarter
  - In charge of 3 U.S. soldiers and 2 Korean Soldiers
- Designed a database system for human resource management

Honors and Awards

- Full Financial Sponsorship for Ph.D. Program *Aug. 2016,* Samsung Electronics
- 2 Years Early Promotion to Senior Engineer *Mar. 2016,* Samsung Electronics
- Highest Honors Feb. *2009, Yonsei University*
- Honors Aug. *2008, Yonsei University*
- U.S. Army Commendation Medal (ARCOM) Oct. 2007, U.S. Army
- U.S. Army Achievement Medal (AAM) Mar. 2007, U.S. Army
- U.S. Army Achievement Medal (AAM) Dec. 2006, U.S. Army
- Honors Aug. *2005, Yonsei University*
- High Honors Aug. *2004, Yonsei University*