Millimeter-Scale Node-to-Node Radio Using a Carrier Frequency-Interlocking IF Receiver for a Fully Integrated $4 \times 4 \times 4$ mm^3 Wireless Sensor Node

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***Abstract*— Ultralow-power (ULP) mm-scale Internet-of-Things (IoT) platforms enable newly emerging applications such as pervasive agricultural monitoring and biosensing. Although there is an increasing interest in node-to-node communication as defined in Bluetooth v5.0, prior research in mm-scale wireless systems is mostly limited to asymmetric node-to-gateway communications. We present a 2.4-GHz node-to-node communication system for an ultra-small wireless sensor node fully integrated within a $4 \times 4 \times 4$ mm^3 form factor. The system integrates multiple stacked layers including an RF transceiver, a ULP processor, a photovoltaic (PV) cell, a 32-kHz crystal, and a 3-D magnetic dipole antenna. The transceiver front-end circuit is co-designed with a printed 3-D magnetic dipole antenna to form a power oscillator for the transmitter (TX) as well as a Q-enhanced amplifier (QEA) for the receiver (RX). A new carrier frequency-interlocking IF architecture successfully mitigates the TX–RX carrier frequency synchronization challenge that is critical to the mm-scale radio systems. The complete system achieves −94-dBm sensitivity with 97-μW power consumption and −12.6-dBm equivalent isotropically radiated power (EIRP). Standalone operation of a sensor node is demonstrated through bi-directional wireless communication to another sensor node over 1-m distance in real, uncontrolled wireless channels.**

***Index Terms*— Internet-of-Things (IoT), mesh wireless sensor networks, millimeter-scale sensor node, printed loop antenna, Q-enhanced amplifier (QEA), ultra-low power (ULP) RF transceiver.**

I. Introduction

THE number of connected smart devices is growing fast toward the highly anticipated vision of ubiquitous Internet-of-Things (IoT) devices. Along this trend of growth of connected IoT devices shown in Fig. 1, the sensor node's form factor has been consistently scaled down to centimeter and, more recently, to millimeter scales [1]–[3]. Making the wireless sensing system smaller, lower power, and more affordable has become an important problem for both industry and academic research. A mm-scale distributed sensor node enables novel applications such as industrial ubiquitous sensing, smart cities [4], agricultural monitoring, implantable biomedical devices, and unobtrusive surveillance systems. For these applications, the communication solution needs to cover at least a few meter distance while maintaining the ultra-small (mm-scale) form factor including the antenna.

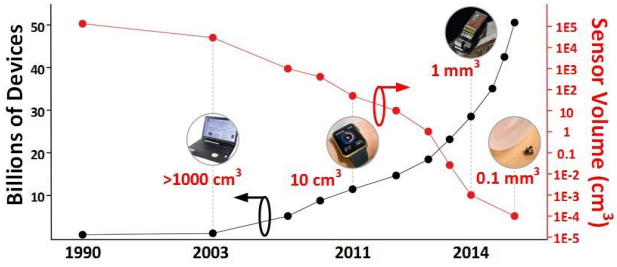

Fig. 1. IoT trends on the number of devices and the size of miniature nodes.

There are numerous challenges for radio systems when fully integrated within a mm-scale form factor. The first one is its limited form-factor dimension. Because of this constraint, the antenna becomes electrically small and its radiation efficiency suffers as governed by fundamental physics. In addition, an RF antenna often requires a relatively large keep out area as in Fig. 2(a), which makes it harder to integrate in a small system. From an antenna design perspective, millimeter-wave (>10 GHz) is a good candidate for the small form-factor design due to its compact antenna dimension. However, the excessive path-loss of millimeter-wave signal and the power consumption of the transceiver make it less practical for small and low-cost IoT sensors.

Another major challenge for mm-scale node wireless communication is the limited energy source of the system. The battery capacity does not scale linearly with its dimension. Existing mm-scale batteries, as shown in Fig. 2(b),

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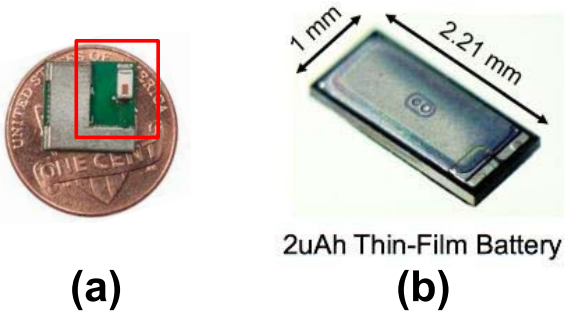


Fig. 2. Challenges for the mm-scale sensor. (a) Small RF antenna. (b) mm-scale battery.

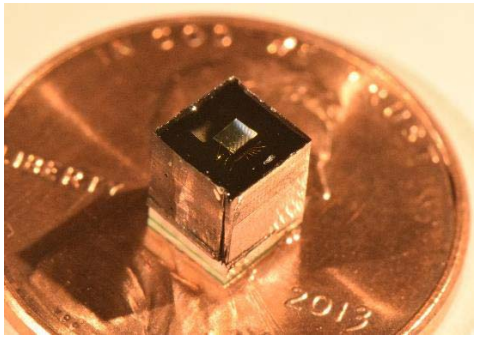


Fig. 3. Proposed fully integrated system with the processor, radio, PV cell, and printed antenna. Stacked chips are encapsulated with black epoxy with an opening exposed to PV cells for light-energy harvesting.

have extremely small capacity ($<10\ \mu$Ah) and very high internal resistance (10–30 kΩ). They can only source tens of μA, which is not sufficient to operate a conventional (standardized) low-power radio such as Bluetooth [5] and ZigBee [6].

Prior solutions to those challenges typically employ an asymmetric solution where the sensor node only communicates with a high-performance gateway, which is plugged into a power outlet and has powerful digital signal processing (DSP) capability [2], [3]. The asymmetric communication topology and powerful gateway hardware allow the sensor node to reduce significantly its complexity and power consumption [3]. However, this approach is only feasible in a centralized star network topology. The main drawback of a gateway-based star network is that its coverage area is limited by the gateway deployment. As the number of sensor nodes increases covering a larger area, the number of gateway devices also needs to increase proportionally. This will not only increase the cost of sensor network deployment but also impose additional constraints on applications when a strategic gateway placement is not feasible (e.g., due to the lack of power source). On the other hand, in a mesh network where nodes communicate with each other without involving a gateway, the signal can hop from one node to another for increased network coverage. The capability of supporting a mesh network is an increasing trend in the recent IoT standard such as Bluetooth 5 and ZigBee [5], [6].

While there are some existing standards that define IoT mesh connectivity, their complexity, power consumption, and stringent standard-compliance specification limit their applicability to mm-scale sensor nodes. The issue of poor gain of an electrically small RF antenna on a mm-scale platform becomes more critical in the mesh network, because the signal is attenuated twice at both the TX and the RX. Moreover, since the communication link is symmetric without a powerful gateway, each sensor node needs to support sufficient TX power as well as good RX sensitivity. The carrier frequency synchronization between the TX and the RX becomes critical, as each ultralow power (ULP) node lacks computational power and resources to mitigate synchronization errors via complicated DSP adopted in other solutions [3], [7].

In this article, we propose a mm-scale node-to-node radio system, as shown in Fig. 3, fully integrated within a $4\times4\times4$ mm^3 form factor operating in the 2.4-GHz industrial, scientific, medical (ISM) band. The system is constructed by stacking integrated circuits (ICs) that are connected through wire bonding [8] and placed on one side of a miniaturized printed antenna. We have employed the following major techniques in the proposed radio system:

1) High-Q Miniaturized 3-D Antenna and Circuit Co-Design: We investigate and quantify the performance of electrically small dipole antennas, co-designed with the transceiver front-end circuitry. We tightly integrate a highly custom-designed $4\times4\times3$ mm^3 3-D magnetic dipole antenna into the system to resonate with the off-chip lumped components without conventional antenna impedance matching.

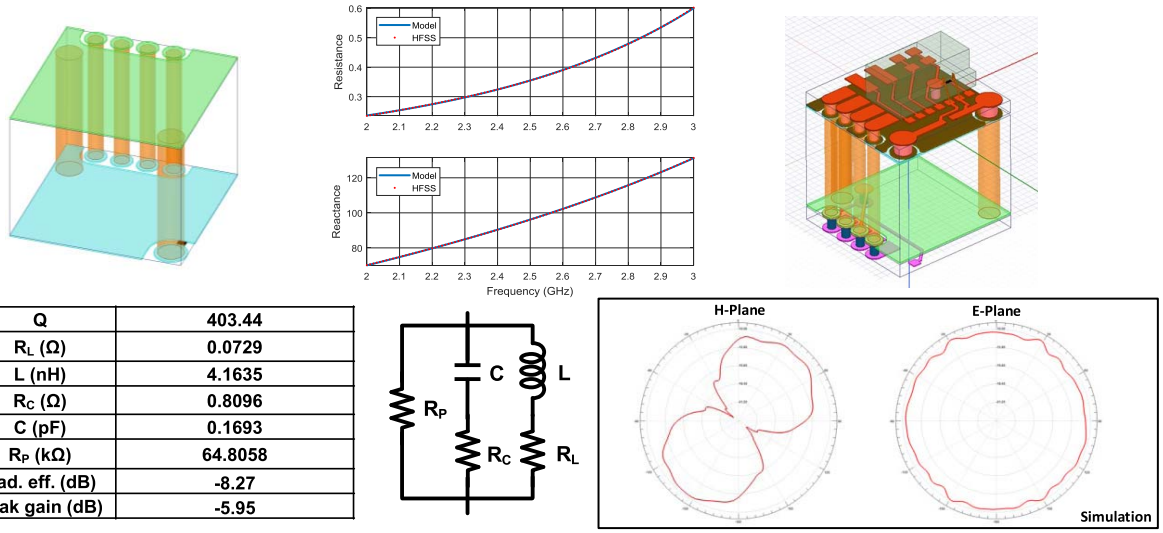
2) 2.4-GHz RF Front-End Sharing for TX and RX Using a Low-Power 32-kHz Real-Time Clock Reference: For node-to-node synchronization, we use a low-power 32-kHz crystal oscillator, as the frequency reference for both baseband sampling and 2.4-GHz RF carrier frequency. Moreover, we take advantage of a front-end circuit sharing scheme to ensure the frequency alignment between the TX and the RX.

3) Carrier Frequency-Interlocking IF Receiver: A new carrier frequency-interlocking IF receiver is proposed to tighten the passband of the RX chain for improving the sensitivity without explicitly estimating the RX local-oscillator (LO) frequency or unnecessarily widening the IF stage bandwidth. The proposed architecture reuses most of the receiver chains for both data communication and auto-tuning of the RX passband by locking the RX LO frequency at the maximum energy reception when stimulated with the TX frequency generated with the same front end.

This article is organized as follows. Section II provides the system overview including the design of an electrically small antenna, link-budget analysis, and the time-division multiple access (TDMA) scheme. Section III describes the design tradeoffs between the prior low-power receivers and the proposed architecture. Section IV describes the circuit implementation details. Section V presents the measurement results, and Section VI concludes this article.

II. System Overview

The proposed system integrates an off-chip 32-kHz crystal, three off-chip capacitors (two 4.7-μF decaps and one antenna-tuning cap), and a magnetic dipole printed circuit board (PCB) antenna on which the RF transceiver, ULP Cortex M0 processor, and other chips are stacked. We employ an always-on 32-kHz ULP crystal oscillator as the carrier



Q	403.44
R_L (Ω)	0.0729
L (nH)	4.1635
R_C (Ω)	0.8096
C (pF)	0.1693
R_P (kΩ)	64.8058
Rad. eff. (dB)	-8.27
Peak gain (dB)	-5.95

Fig. 4. Proposed electrically small magnetic dipole antenna, its circuit model, and the radiation pattern.

frequency reference, baseband frequency reference, and sleep timer to enable TDMA-based node-to-node communication. A ULP Cortext M0 processor integrated in the system tracks the received symbol time-stamps and adjusts the wake-up/transmit/receive/sleep timing for the synchronized TDMA communication among the nodes. Long-term clock drift is governed by the 32-kHz crystal oscillator (Seiko SC12S) in our system, which has ±20 ppm frequency tolerance and is relatively stable. For example, with 1-s packet interval, the sampling time mismatch is limited to ±0.02 ms (much shorter than one pulsewidth in our system). Long-term time drift can be compensated by performing periodic timing adjustment based on the time offset between the expected packet detection time and the actual detection time obtained by the software running on the Cortex M0. We can adjust the sensor duty-cycle interval to reduce the timing drift at the cost of increased overall system power.

A. Electrically Small Antenna

Fig. 4 shows the magnetic dipole antenna used in this radio system. The antenna is fabricated with a two-layer Rogers RO4003C material with a dimension of $4 \times 4 \times 3.118$ mm^3. The proposed antenna forms a 3-D loop with two diagonal vias connecting the upper and lower layers, as shown in Fig. 4 (top left). There are four additional side vias serving as the routing connection for electronics [chips, battery, and photovoltaic (PV) cell] in the upper and lower layers. The antenna can be modeled as a parallel resistor (R), inductor (L), capacitor (C) circuits with parameters shown in Fig. 4 (bottom).

Operating such an antenna at a radio frequency makes it electrically small. Thus, it has the minimum quality factor (Q) bounded by Chu limit [9] or 1 for the lossy antenna [10], where r is the radius of the magnetic dipole and R_L is the loss resistance

$$Q \geq \frac{20\pi^2 kr}{R_L}, \quad k = \frac{2\pi}{\lambda}. \tag{1}$$

The Q-factor at 2.45 GHz is 403 according to our simulation, which is significantly higher than that of a conventional antenna designed for relatively wide bandwidth and 50-Ω matching. The simulated radiation pattern including the impact of electronics around the proposed antenna shows that this type of antenna does not require a keep-out area, which is very beneficial to mm-scale system integration. Moreover, when sensor nodes are placed on a horizontal ground plane, the far-field performance of the 3-D structure improves because of the image current generated by the current in the vertical loop [11]. An electrically small antenna has difficulties in impedance matching, and a low-Q antenna with a wide bandwidth is usually preferred for traditional (without a stringent size constraint) antenna design. However, we take advantage of the proposed electrically high-Q antenna as: 1) a front-end RF bandpass filter for out-of-band interference suppression and 2) a part of the passive voltage-boosting circuit, which will be discussed further in Section IV.

B. Incident Field of Electrically Small Antenna

Since the antenna is electrically small and not matched to 50 Ω, the Friis equation is not directly applicable to calculate the received signal power available at the antenna output. We analyze the voltage developed at the receiver's antenna by (2), where E is the incident electric field at the specific distance [12] and r is the radius of the antenna

$$V = 4Ekr^2, \quad k = \frac{2\pi}{\lambda}. \tag{2}$$

Fig. 5 shows the calculated voltage developed at the receiver antenna when 100-μW power is incident into the transmitter antenna and the expected equivalent isotropically radiated power (EIRP) is −17.8 dBm. At ≥ 5-m distance, ≤ 5-μV swing is developed at the received antenna, which is equivalent to ≤ −96-dBm received power at the input of the antenna. Note that the available equivalent power at the output of the antenna is significantly lower because of the poor gain (−7.8 dBi, simulated) of the electrically small antenna.

C. TDMA-Based Node-to-Node Communication

Fig. 6 shows the TDMA scheme used in the proposed radio system, a simplified version of [13]. Each time slot shown

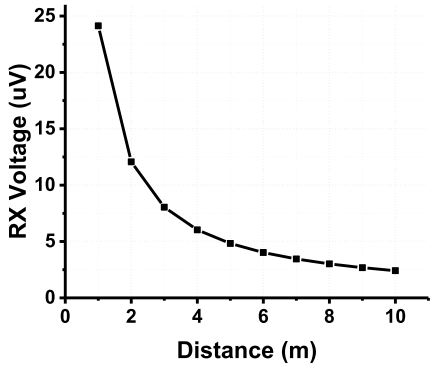


Fig. 5. Voltage developed at the receiving node antenna assuming 100-μW power goes into the transmitting node.

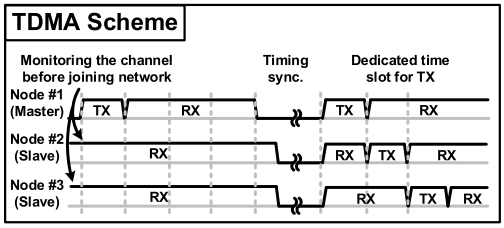


Fig. 6. Multiple access scheme used in the proposed radio system. All nodes will need to monitor the channel before starting transmission except the master node.

in Fig. 6 can be programed within a range from 0.25 ms (1 bit) to 24 ms (96 bits). All sensor nodes are pre-programed with a unique node identification (ID) and a master node is pre-determined. Except for the master node, all other nodes who want to join the network need to first monitor the channel until it receives a valid message to extract the correct timing information from a node participating in the network. Upon extracting the timing information from a received packet, the processor calculates the dedicated transmission time slot based on its node ID to join the TDMA network. All nodes transmit at the designated time slot, which is uniquely determined based on their node ID while they are in the receive mode for the time slots that belong to other nodes. This scheme requires the sensor node to be mostly in the receive mode especially when the number of nodes in the network is large. Hence, more attention needs to be paid to optimize the receiver power rather than the transmitter power to minimize the overall energy for the bidirectional node-to-node communication.

III. Carrier Frequency-Interlocking IF Receiver

A. Low-Power Receiver Design Tradeoffs

A low-power high-sensitivity receiver is a key to enable node-to-node mesh network communication among the mm-scale sensor nodes. The low-IF/sliding-IF receiver [14], [15] commonly used in the low-power Bluetooth or Zigbee receivers demonstrates good sensitivity, but the stringent specification of a high-quality local oscillator (LO) makes its power consumption unsustainable by a mm-scale battery. As many wireless network applications using mm-scale sensor nodes do not require a high data rate, we make a tradeoff in our transceiver design to lower the power consumption for a lower data rate (4 kb/s) and narrower bandwidth, which consequently allows longer data communication links due to

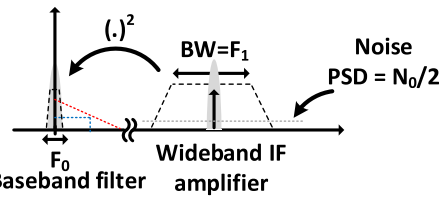


Fig. 7. Frequency-domain spectrum of the IF signal being converted into baseband and the noise redistribution (in red and blue curves).

less noise power integrated over a narrower bandwidth. Most of recent low-power (<100 μW) receiver designs [16]–[19] employ a non-coherent demodulation scheme, which has the benefit of reducing the power consumption of LO generation [without a phase-locked loop (PLL)] and simplifying the demodulation circuit. Prior designs such as those in [16] adopt an uncertain-IF approach that uses a free-running LO and widens the intermediate frequency (IF) stage bandwidth (e.g., 100 MHz in [16]) to accommodate the uncertainty of LO. This approach significantly lowers the receiver power consumption but has signal-to-noise (SNR) reduction due to its wideband IF stage that invites more noise.

A representative frequency-domain spectrum for non-coherent energy detection low/uncertain IF receiver SNR analysis is shown in Fig. 7. The noise power spectral density (PSD) is $\frac{N_0}{2}$, the passband bandwidth at the energy detector input (determined by the IF stage) is assumed to be F_1, and the baseband signal (or its matched filter) bandwidth is F_0, where $F_0 \ll F_1$ holds for many ULP RF receiver designs.

We derive (3) for the SNR analysis of the IF energy detector receiver, where V_{sig} represents the signal voltage

$$(V_{sig} + \sqrt{\frac{N_0}{2}F_1})^2 = (V_{sig})^2 + 2V_{sig}\sqrt{\frac{N_0}{2}F_1} + \frac{N_0}{2}F_1. \quad (3)$$

Equation (3) shows the noise power that consists of two contributors [20]: one is the noise self-mixing (the last term in 3), resulting in a triangular PSD at the baseband with the bandwith of F_1 as shown in the red line in Fig. 7 and the other contributor is the noise mixed with the signal uniformly distributed at the baseband (the second last term in 3) with the bandwidth of $\frac{F_1}{2}$ indicated by the blue line in Fig. 7. The power of the uniformly distributed noise is obtained by (4), which indicates that this noise power only depends on the input SNR (i.e., V_{sig} and N_0) and the signal (or baseband matched filter) bandwidth

$$\sigma^2_{uniform} = \int_0^{F_0} \frac{(2V_{sig}\sqrt{\frac{N_0}{2}F_1})^2/2}{F_1/2} df = 2(V_{sig})^2 N_0 F_0. \quad (4)$$

On the other hand, calculation of the noise power from the triangular PSD in (5) reveals that the noise power also depends on the IF stage bandwidth F_1. The total noise of a low/uncertain IF energy detector receiver is the summation of these two noise sources as in (6). When the input SNR is small at the maximum link distance, the $\sigma^2_{triangular}$ dominates, and thus, it is desired to make $F_1 = F_0$ for an ideal receiver. However, the low-power uncertain-IF scheme such

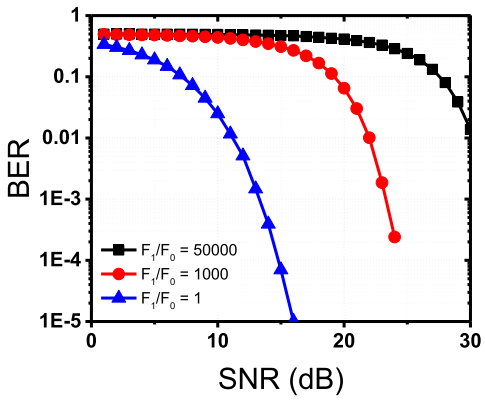


Fig. 8. Simulated BER degradation due to F_1/F_0 ratio.

as [16] requires a wide IF stage bandwidth $F_1 \gg F_0$ to capture the full signal power in the presence of LO frequency uncertainty. Fig. 8 shows the simulated bit-error-rate (BER) degradation due to the wider F_1 in the uncertain IF architecture

$$\begin{aligned}\sigma^2_{triangular} &= \int_0^{F_0} \left(\frac{N_0}{2}\right)^2 (F_1 - f)df \\ &= \left(\frac{N_0}{2}\right)^2 \left(F_1 F_0 - \frac{1}{2}F_0^2\right) \\ &\simeq \left(\frac{N_0}{2}\right)^2 F_1 F_0, \quad when \quad F_0 \ll F_1 \end{aligned} \tag{5}$$

$$\sigma^2_{noise} = \sigma^2_{uniform} + \sigma^2_{triangular}. \tag{6}$$

B. Carrier Frequency-Interlocking IF Receiver

The proposed carrier frequency-interlocking IF receiver architecture addresses the wideband IF stage issue by implicitly locking the receiver LO (a ring oscillator in this work) frequency to a referenced RF transmit signal. Conventional approaches explicitly lock both the TX and RX frequencies separately using a PLL, which often demands high power consumption and a relatively high-frequency (tens of mehahertz) crystal reference, which further increases the power consumption and the system integration cost. Instead, the proposed ULP radio locks the TX frequency using a 32-kHz crystal [21] and runs it in open loop per packet. Thanks to the circuit-antenna co-design and TX/RX front-end sharing, the locked TX signal can be used as a RF reference tone to lock the RX LO and IF stage after searching for the maximum received IF energy point, as shown in Fig. 9, and the interlocking timing is shown in Fig. 10.

The one-time exhaustive search can take a worst case duration up to 72 ms (TX frequency-locked loop (FLL) and the RX IF locking). Once the TX and RX frequencies are matched, the processor starts from the previous locked code to perform a minor adjustment for each time the sensor node transmit a packet. This adjustment completes during the ordinary transmission packet length. This topology reuses most of the receive data demodulation chain to perform the energy detection in the searching and locking phases. As the receiver LO and the IF passband are locked to the TX signal, the IF stage bandwidth can be reduced to improve the SNR (Fig. 8) without a well-controlled IF passband circuit or accurate LO frequency generation. Unlike the wide-IF uncertain LO topology, the relation of $F_{LO} = F_{RF} - F_{IF}$ can be guaranteed once the maximum IF energy is detected. This topology allows the exploration of the tradeoff space between the tuning range of the LO and the IF stage bandwidth.

Fig. 11 shows the circuit implementation of the proposed transceiver architecture. The TX and the RX share the same front-end power oscillator [3], [22] that uses the high-Q PCB antenna as an inductor for the LC oscillation circuit. The transmitter has a FLL using the 32-kHz real-time clock (RTC). The receiver uses a low-power ring oscillator (RO) to downconvert the RF signal to the IF stage that amplifies the signal, and it performs the energy detection to further convert the IF signal into baseband. The signal uses ON–OFF keying (OOK) modulation with Manchester coding. After the TX FLL, the receiver's RO is tuned for frequency interlocking by reusing most of the received data demodulation path and searching for the maximum energy point. The TX FLL and the RX frequency interlocking are performed every time when the sensor node wakes up.

IV. Circuit Implementation

A. Transmitter Design

Fig. 12 shows the TX front end and the FLL circuits. In the transmit mode, the baseband controller directly modulates the tail current to transmit the modulated RF pulses. The transmitter has a power oscillator structure that uses the antenna as the resonant inductive component with 4-V supply to maximize the output power. It delivers the signal directly onto the antenna coil without a matching network. This structure does not require an additional carrier frequency-generation (local oscillator) circuitry, which typically consumes a significant portion of the transmitter power. The intrinsically high-Q antenna lowers the power consumption of oscillation and provides phase-noise filtering. The transmitter exhibits a measured efficiency of 25.7% (excluding the antenna gain and at the condition of 3.6-V supply with −13.9-dBm EIRP). In order to maximize the Q of the oscillation tank, we use a high-Q off-chip surface-mount device (SMD) capacitor as the coarse-frequency-tuning component in addition to a 6-bit on-chip capacitor bank for finer tuning. One major challenge of this free-running oscillator approach is to align the carrier frequency between different sensor nodes and within the RF front-end TX and RX paths. The FLL is composed of a 32× divider, an asynchronous counter, and a frequency tuning logic (Fig. 12). The counter is clocked by a divided RTC (32.768/4 = 8.192 kHz) supplied by the processor layer in the system. It counts the number of divided RF signal transitions (75 MHz) and locks the frequency accordingly. The target frequency accuracy is within 0.1% (to match to the RX front-end passband, as explained in Section IV-B). Thanks to the high-Q antenna, we can free-run the transmitter during the actual data transmission after the frequency is set. Since the carrier frequency is mostly determined by the 3-D loop antenna and the OFF-chip capacitor, it does not have significant supply voltage dependence. Thus, the FLL is mainly for compensating the antenna and OFF-chip capacitor variations.

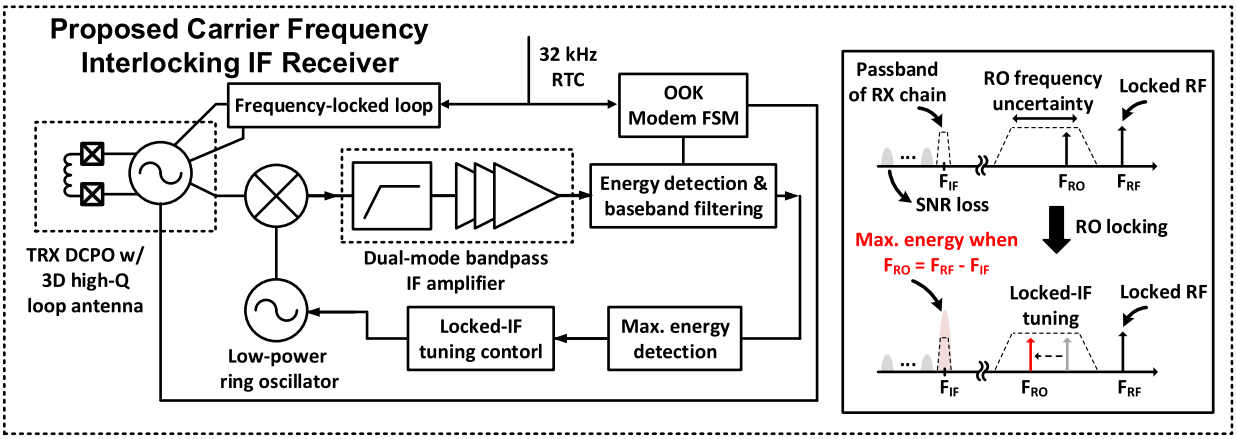


Fig. 9. Proposed-interlocking timing scheme.

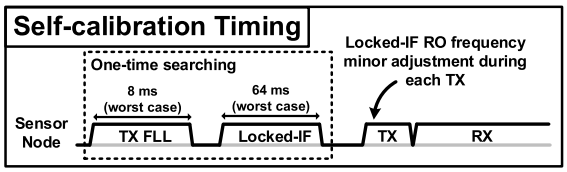


Fig. 10. Proposed carrier frequency-interlocking IF radio architecture and the frequency-domain explanation.

B. Receiver Design

In the receive mode, we employ a Q-enhanced amplifier (QEA) with the reuse of the TX power oscillator in the front end [3] followed by a mixing stage to downconvert the signal to IF, as shown in Fig. 13. The IF stage has a bandpass response with a 3-dB bandwidth of ≈4 MHz, which is matched to the bandwidth of the Q-enhanced amplifier front end. The IF stage is followed by a common-source (CS)-amplifier that serves as an energy detector (ED). The LO is a five-stage ring oscillator with 10-bit control. As shown in Fig. 13, the carrier frequency-interlocking IF loop reuses most of the normal receive chain. The attenuator is used for preventing saturation during the tuning loop that searches for the maximum ED output energy point when the transmitter is turned on. In the normal RX mode (without TX), the cross-coupled transistors are biased for the Q-enhanced mode operation [3] to obtain a high passive voltage gain (but without oscillation as in the TX mode or interlocking mode). Since this topology uses a relatively high phase-noise local oscillator in the receive mode, it can potentially cause reciprocal mixing when there is a strong blocker. However, the LC tank with the high-Q antenna serves as a band-selective front-end filter, which increases the receiver blocker tolerance and eliminates the need for a separate off-chip channel selection filter. For demodulation of the binary Manchester-coded OOK, the receiver compares the energy at two consecutive pulse positions. This scheme eliminates the need for a carefully tuned threshold voltage for the comparator in conventional OOK receivers.

Since the TX and RX share the same LC tank, its frequency will be naturally close. However, there are still some non-linear loading capacitors that can slightly shift the frequency between the TX and RX modes. Fig. 14 shows that there is a slight mismatch between the TX signal output spectrum and the Q-enhanced RX bandwidth due to the non-linear effect, but they are still close enough for the TX signal to fall into the RX passive voltage-boosting bandwidth.

V. Measurement Results

A. System Integration

Fig. 15 shows the proposed integrated radio system before black epoxy encapsulation. The system has a $4 \times 4 \times 4$ mm^3 form factor, which integrates the antenna, an OFF-chip 32-kHz crystal, and the stack of chips including the RF transceiver, power management unit (PMU), energy harvester, PV cells, and ULP processor. The four-side vias are used to connect the rechargeable battery on the other side of the antenna. The system has a total of three OFF-chip capacitors: two 4.7 μF decaps and one antenna-tuning cap. As shown in Fig. 15, electronic components are directly stacked on the top of the 3-D magnetic dipole antenna, as it does not require a keep-out area to maintain the radiation performance. We apply black epoxy (Fig. 3) to cover the chip stack, because ULP chips are highly sensitive to light. We use a mm-scale lithium battery in our system. The harvested energy from the PV cell has an efficiency >70% with different light conditions and it can provide 10 nA to 8 μA current to (re)charge the battery [23]. Fig. 16 is the die photograph of the radio chip taped out in the 55-nm deeply depleted channel (DDC) CMOS technology.

B. Sensor Node Transmitter Performance

Fig. 17(a) shows the carrier frequency-tuning range of the transmitter. The x-axis is the tuning thermometer code and the y-axis is the carrier frequency. We use the ON-chip capacitor banks for tuning. It has six tuning bits to cover a 20-MHz tuning range at 2.4 GHz. During the receive mode, the antenna (LC tank) Q value is boosted to about 1000 (0.1%), which sets the TX FLL accuracy requirement for frequency matching. As shown in Fig. 17(b), the five tested chips are measured to be frequency-aligned within the target range of 0.1% (≈ ±2.4 MHz for a 2.4-GHz carrier) with the FLL. The overall Q-factor is determined by the ratio of fine-tune and coarse capacitor. We intentionally make the ratio small to have the highest combined Q.

Fig. 18(a) shows the setup for wireless system performance testing. Fig. 18(b) shows the measured EIRP as a function of

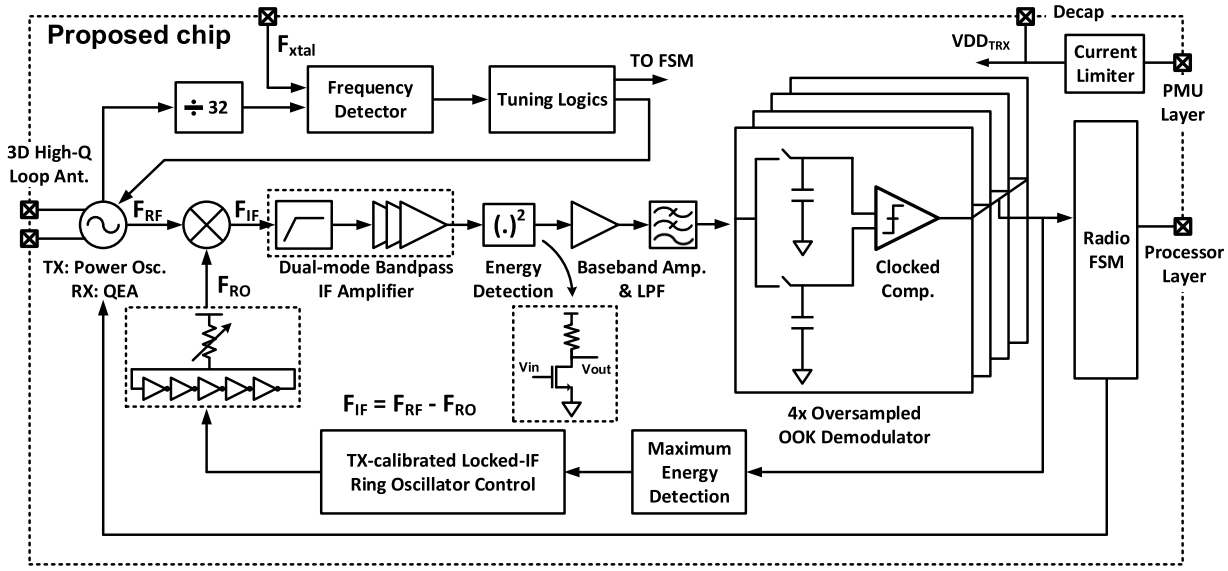


Fig. 11. Proposed radio system implementation.

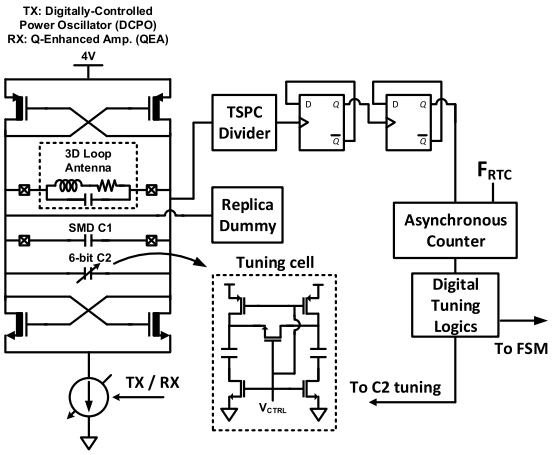


Fig. 12. Transmitter digitally controlled power oscillator FLL using system RTC.

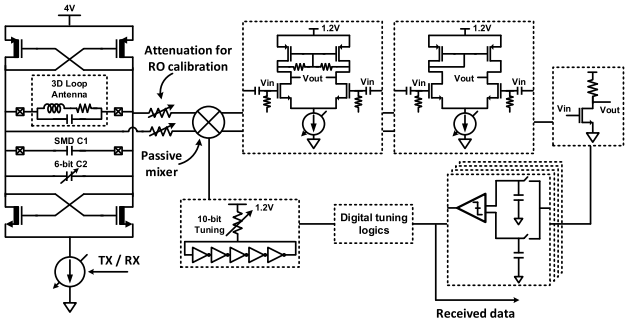


Fig. 13. Receiver circuit implementation with the proposed carrier frequency-interlocking loop.

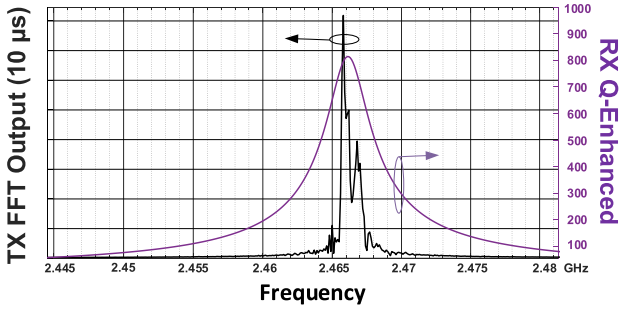


Fig. 14. Carrier frequency difference between the TX and the RX mode switching.

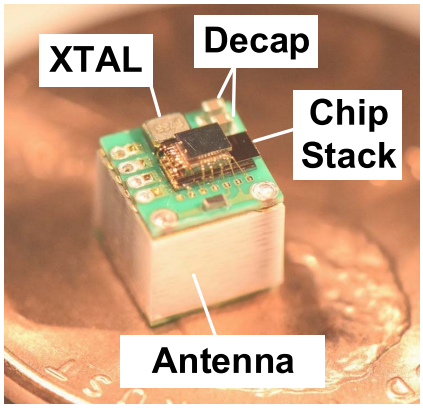


Fig. 15. Integrated wireless sensor node with 32-kHz crystal, three off-chip capacitors, antenna, radio, processor, solar cell, and PMU.

the transmitter bias current. The maximum EIRP *including* the mm-scale antenna's negative gain of −7.8 dBi (simulated) was measured at −12.6 dBm with an 880-μA bias current at 4 V.

C. Sensor Node Receiver Performance

Fig. 19(a) shows the measurement results of the proposed carrier frequency-interlocking IF loop to calibrate the RO frequency. Since the supply voltage in the mm-scale sensor node can significantly fluctuate (±150 mV) due to the weak battery and small decap, the interlocking loop was tested with different supply voltage levels. It is observed that it can lock the RO across a wide supply voltage range from 1.1 to 1.4 V. The worst case locking time is 64 ms when it searches through the entire tuning code (10 bits) with a 16-kHz clock. After one-time exhaustive search, the TRX frequency inter-locking is adjusted during each regular packet

TABLE I
SUMMARY AND COMPARISON WITH RECENT WORKS

		This work	ISSCC 2017 [3]	JSSC 2016 [17]	ISSCC 2015 [19]
Technology		55 nm	180 nm	65 nm	65nm
System Form Factor		4x4x4 mm^3	3x3x3 mm^3	4.6x4.6 mm^2 Receiver chip only	1.3x0.9 mm^2 Receiver chip only
# of off-chip components		5 (Antenna, xtal, decaps)	4 (Antenna, decaps)	11 (Inductors, decaps)	3 (Inductors)
Frequency		2.4 GHz	900 MHz	2.4 GHz	2.4 GHz
Sensor-to-Sensor Communication?		Yes	No	No	No
RX	Technique	Carrier Frequency Interlocking IF	Tuned-RF	Dual Uncertain-IF	RX-based FLL
	Modulation	Binary PPM	Binary PPM	OOK	OOK
	Power Consumption	97 µW (16 µW QEA)	1850 µW	99 µW	227 µW
	Data Rate	4 kbps	7.8 kbps – 62.5 kbps	10 kbps	1 Mbps
	Sensitivity*	-94 dBm (@ input of -7.8 dBi antenna)	-93 dBm (@ input of -23.4 dBi antenna)	-97 dBm (@ input of AFE)	-83 dBm (@ input of AFE)
TX	Technique	RTC-FLL	Free-running	N/A (RX only)	N/A (RX only)
	Max. EIRP	-12.6 dBm	-26.9 dBm		
	Power Consumption	3.5 mW @ 4V	2 mW @ 4V		
	Data Rate	4 kbps	30 bps – 30.3 kbps		

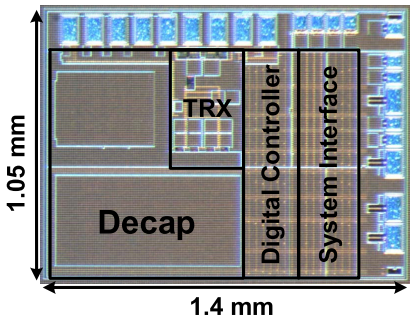


Fig. 16. Radio die photograph in 55-nm DDC CMOS.

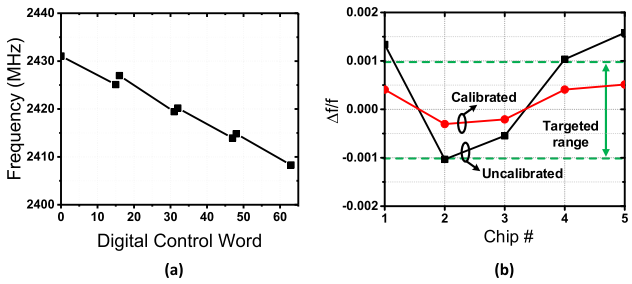


Fig. 17. Transmitter performance. (a) Tuning range. (b) FLL for frequency alignment over five different chips.

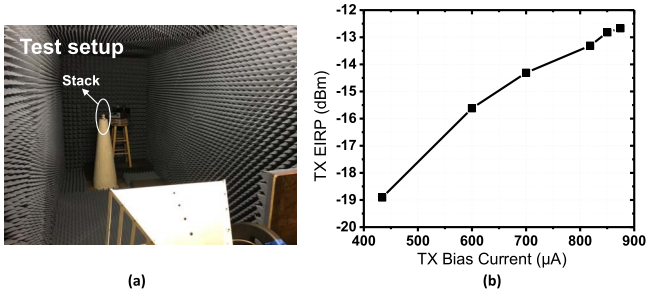


Fig. 18. (a) Test setup for wireless system measurement. (b) TX EIRP.

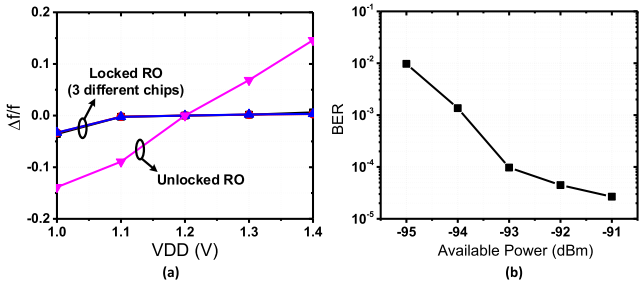


Fig. 19. Receiver performance. (a) Proposed carrier frequency-interlocking IF for RO calibration. (b) Sensitivity of the receiver including the antenna and available power defined as the received power at the antenna.

transmission without lengthening the packet. Note that the sensitivity of the receiver cannot be directly measured via a wired test, because the front end is co-designed with the antenna and not impedance-matched to 50 Ω. Therefore, we measure the sensitivity wirelessly by measuring the RX signal power level at a reference antenna next to the sensor node and sharing the baseband clock between the TX and the RX to synchronize the baseband timing. Fig. 19(b) shows the measured sensitivity of the proposed receiver. It achieves −94-dBm sensitivity with 10^{-3} BER. This sensitivity is the power level available at the input of the mm-scale antenna, and the power available for demodulation is significantly lower due to the negative antenna gain (simulated antenna gain of −7.8 dBi). The receiver power consumption is 97 μW at the data rate of 4 kb/s.

D. System Measurement

Fig. 20 shows the captured waveforms, showing two sensor nodes communicating with each other in a TDMA scheme. An internal TX control signal from one node and the ED out-

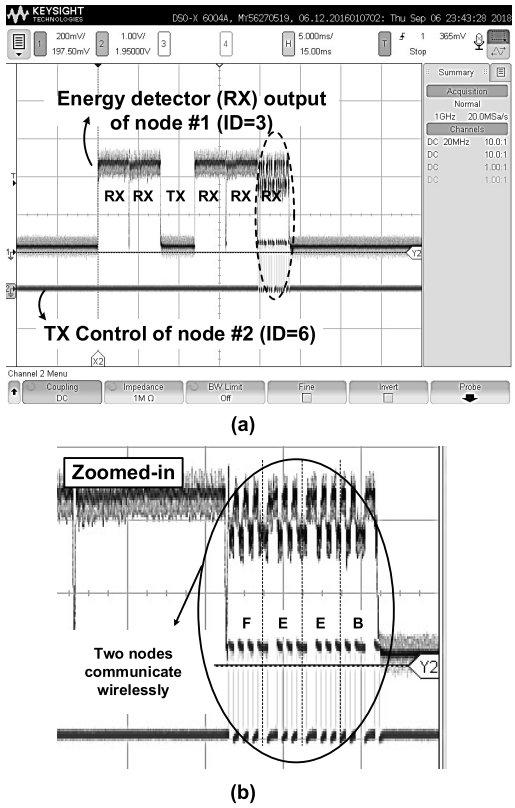


Fig. 20. (a) Wireless measurement of two nodes communicate with each other in the TDMA scheme. (b) Zoomed-in view to one TX-RX event. TX node transmits data "0xBEEF" in hexadecimal.

put signal from another node are captured on an oscilloscope. From Fig. 20, sensor node #1 has a node ID of 3 (thus it transmits at the third slot) and node #2 has a node ID of 6 (transmission using the sixth slot). The zoomed-in plot for the sixth slot clearly shows that two nodes are time-synchronized (node 2 TX and node 1 RX), and the Manchester-coded message is correctly demodulated. Table I summarizes the performance of the transceiver and provides a comparison with the related work.

VI. Conclusion

This article presented a fully integrated IoT sensor node communication system, addressing unique challenges in mm-scale node-to-node communication such as the electrically small antenna design, frequency synchronization, and stringent energy budget. In this article, we studied and analyzed the design tradeoffs of the ULP radio system and proposed a new transceiver architecture by co-designing the TRX front end with the antenna. We prototyped the system in a $4 \times 4 \times 4$ mm^3 form factor that integrates a transceiver chip, an antenna, a crystal, a PMU, a solar cell, and a baseband processor with a new carrier frequency-interlocking IF receiver architecture for low-power and high sensitivity communication. The proposed mm-scale radio system demonstrated a sensor-to-sensor communication with -12.6-dBm EIRP for TX and -94-dBm sensitivity with 97-μW power consumption for RX. This system enables wireless mesh networks for ultra-small sensing devices increasing their potential for unobtrusive IoT sensing applications.

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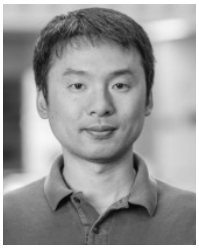

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