CURRICULUM VITAE

Andrea M. Bejarano
bejarano@umich.edu
734-780-0981

EDUCATION

University of Michigan (2019-Expected 2024)

PhD Electrical and Computer Engineering

- Advisors: Prof. David Blaauw and Prof. Hun Seok Kim
- Track: VLSI/Embedded Systems

University of Bristol (2015-2019)

MEng Electrical and Electronic Engineering: First Class Honors

HONORS AND AWARDS

- EE Departmental Prize for the best Master's Individual Research Project, University of Bristol *(July 2019)*
  "4G LTE and 5G Direct-Air-to-Ground Communications for Airplanes: Capacity and Coverage Enhancement through Cellular Planning and Interference Mitigation Techniques"
- SCEEM Community Award for outstanding contribution to School Outreach and Societies, University of Bristol *(July 2019)*
- United Kingdom Electronic Skills Foundation Scholarship *(2017-2019)*
- University of Bristol PLUS Award (*June 2017)*

CURRENT RESEARCH

Low-power Imaging System – University of Michigan

September 2019 – Ongoing

- Working on a millimeter-scale, low-power imaging system, which includes integrating several system components, and developing and testing system behaviors according to a user-defined scenario
- Creating a data collection platform which integrates with this system in order to train and evaluate the algorithms used in the system

PROFESSIONAL EXPERIENCE

VLSI Design Teaching Assistant – University of Bristol, United Kingdom

January 2019 – April 2019

- Worked alongside the unit director and other teaching assistants to provide relevant teaching and laboratory support, and guidance for students

Digital Design Intern, Dialog Semiconductor – Swindon, United Kingdom

June 2018 – August 2018

- Developed a PMIC FPGA emulation improvement project alongside the Digital Design Team by using software, such as Cadence SimVision and Xilinx Vivado, to implement chip-level modifications

- Enhanced my presentation skills by showcasing the procedure and usage of the new FPGA extended emulation environment to Senior Engineers and Application Engineers

PMIC Layout Intern, Dialog Semiconductor – Swindon, United Kingdom

June 2017 – August 2017

- Optimized existing IP by 40% for an upcoming product by working collaboratively alongside the PMIC (power management integrated circuit) Layout Team
- Demonstrated strong self-management by learning how to use Cadence software for cell floor-planning, routing, layout vs. schematics and design rule checks in a short period of time
- Developed critical thinking and communication skills by justifying layout decisions and presenting work to the Senior Design and Layout Engineers leading the project

PREVIOUS RESEARCH

Electrical and Electronic Engineering Master's Thesis, University of Bristol

September 2018 – May 2019

- Evaluated how 4G LTE is currently being used and redesigned to provide broadband mobile services to aircraft passengers, and explored how new characteristics of 5G can be considered in the DA2GC (Direct Air to Ground Communications) scenario
- Creation of a software simulation platform to provide data on the networks' performance metrics and individual users' data and to evaluate whether 5G techniques, including MIMO, beamforming and beamsteering, can be used to improve DA2GC networks

LEADERSHIP AND OUTREACH

- Electrical and Electronic Engineering Course Representative, University of Bristol *(2016-2019)*
- Secretary of the Bristol Electrical and Electronic Engineering Society *(2017-2019)*
- "Studying EEE at University" and "Women in Electrical Engineering" Outreach Talks, Madrid *(2017-2019)*
- DigiMakers Engineering Outreach Volunteer, Bristol *(2015-2018)*
- IntoUniversity Engineering Outreach, Bristol *(2017)*
- UK Teenage Cancer Trust Volunteer, Bristol *(2017)*

RELEVANT SKILLS

Programming/Hardware Languages and Software

- Experienced in using Python, Java, C, SystemVerilog and VHDL
- Proficient using MATLAB, Altium, Cadence, ModelSim and Xilinx ISE

Languages

English (native), Spanish (native), French (Advanced B2 Level)