Chien-Wei Tseng

1301 Beal Ave. – Ann Arbor, MI 48105, USA

(734)-881-5727 • cwtseng@umich.edu

INTERESTS

Wireless transceiver and DSP system.

WORKING AND RESEARCH EXPERIENCE

Michigan Integrated Circuits Lab(MICL), Ann Arbor, MI, USA
Graduate Student Research Assistant, Advisor: Prof. David Blaauw *Sep.2019 - Present*

- Research on wireless long-range narrow band localization system.
  - Fast-lock ADPLL design and analysis.
  - Low power narrow band Rx design and analysis.

MediaTek Inc., Hsinchu, Taiwan
Senior Engineer *Aug.2014 - Jul.2019*

- Developed a sub-6GHz transmitter for celluar 5G communication system.
  - Designed a wideband 2 to 5 GHz front-end transmitter, including PGA, MOD, and LO circuits.
  - Proposed a harmonic rejection transmitter architecture to suppress TX spurious emissions.
  - Proposed a divider synchronization algorithm for MIMO scenario.
- Developed a multi-mode multi-band TX front-end module for GSM/EDGE/TD-SCDMA/TD-LTE systems.
  - Designed a multi-mode class-F CMOS power amplifier with maximum 33 dBm output power.
  - Proposed a wide bandwidth adaptive bias circuit to improve AM-AM$<$ 0.5 dB and AM-PM$<$ 1 deg.
- Developed a harmonic-rejection filter in TSMC IPD process.
  - Designed a 2nd to 4th $>$ 50 dB harmonic rejection passive filter in hybrid package/IPD process.

NCTU Radio Frequency Very Large Scale Integration Lab, Hsinchu, Taiwan
Research Assistant *Mar.2014 - Jun.2014*

- Developed a 35 GHz 4x4 phase array transceiver in 65 nm CMOS process.
  - Designed 35 GHz LNA, MOD, TIA, and LO circuits in receiver path.
  - Developed a network synthesis tool to generate narrow/wide band matching network with matlab.

NCTU Radio Frequency Very Large Scale Integration Lab, Hsinchu, Taiwan
Master, Advisor: Prof. Yu-Jiu Wang *Sep.2011 - Feb.2014*

- Developed a 60 GHz power amplifier in 40 nm CMOS process.
  - Designed a class-AB PA with 2-path current-mode combine, achieved 19.6 dBm Pout and 18.3 % PAE.
  - Developed a model fitting optimizer tool for inductor/transformer with matlab.

EDUCATION

University of Michigan, Ann Arbor, MI, USA
PhD in Electrical and Computer Engineering *Sep.2019 - Present*

- GPA: 3.89/4.0.
- Selected courses: VLSI for Wireless Communication & Machine Learning(EECS 598), Matrix Method for Signal Processing, Data Analysis and Machine Learning(EECS 551), Integrated Analog/Digital Interface Circuits(EECS 511), Analog Integrated Circuits(EECS 522)

National Chiao Tung University (NCTU), Hsinchu, Taiwan
M.S in Electronics Engineering and Electronics, Advisor: Prof. Yu-Jiu Wang *Sep.2011 - Feb.2014*

- GPA: 4.14/4.3.

National Chiao Tung University (NCTU), Hsinchu, Taiwan
B.S in Electronics Engineering *Sep.2007 - Jun.2011*

- GPA: 3.96/4.3, Major GPA: 4.12/4.3.

PUBLICATIONS AND PATENTS

[1] M. Tsai, C. Tseng, K. Tsai, S. Andrabi, P. Huang, F. Beffa, Y. Chen, and B. Tenbroek. 10.6 A 4G/5G Cellular Transmitter in 12nm FinFET with Harmonic Rejection. In *2020 IEEE International Solid-State Circuits Conference - (ISSCC)*, pages 182–184, 2020.

[2] M. Tsai, C. Lin, P. Chen, T. Chang, C. Tseng, L. Lin, C. Beale, B. Tseng, B. Tenbroek, C. Chiu, G. Dehng, and G. Chien. 13.1 A fully integrated multimode front-end module for GSM/EDGE/TD-SCDMA/TD-LTE applications using a Class-F CMOS power amplifier. In *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, pages 216–217, Feb 2017.

[3] C. Chu, S. Tseng, J. Gao, Y. Chen, Y. Chang, C. Tseng, T. Huang, B. Hu, B. Su, T. Chu, and Y. Wang. A fully-integrated Ka-band 4TX/4RX phased-array transceiver IC in 65nm CMOS. In *2016 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, pages 1–3, Aug 2016.

[4] C. Tseng and Y. Wang. A 60 GHz 19.6 dBm Power Amplifier With 18.3% PAE in 40 nm CMOS. *IEEE Microwave and Wireless Components Letters*, 25(2):121–123, Feb 2015.

[5] C. Tseng and Y. Tseng and M. Tsai and Y. Chen and B. Lin. "PHASE-ROTATED HARMONIC-REJECTION MIXER APPARATUS" US Patent No.10,171,034, Jan 2019.

[6] C. Tseng and M. Tsai. "POWER AMPLIFIER SYSTEM AND ASSOCIATED BIAS CIRCUIT" US Patent No.10,103,691, Oct 2018.

[7] C. Tseng and M. Tsai. "POWER AMPLIFIER SYSTEM AND ASSOCIATED CONTROL CIRCUIT AND CONTROL METHOD" US Patent No.10,056,869, Aug 2018.

[8] Y. Chen and B. Tenbroek and C. Tseng and Y. Tseng and M. Tsai and B. Lin. "QUADRATURE TRANSMITTER, WIRELESS COMMUNICATION UNIT, AND METHOD FOR SPUR SUPPRESSION" US Patent No.10,009,050, June 2018.

TECHNIQUE SKILLS

- **Circuit simulation tools:** Cadence Virtuoso/Allegro, GoldenGate, Agilent ADS, Synopsys Custom Compiler.
- **EM simulation tools:** EMX, HFSS, Sonnet, Agilent Momentum.
- **Programming skills:** C/C++, Matlab, Python, Cadence SKILL, Verilog-AMS.

HONORS AND AWARDS

- **MediaTek Inc.VAwards**, eight times, 2014-2019.
- **National Chip Implementation Center (CIC) Outstanding Chip Design Award**, 2014.