Gordy Carichner

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SUMMARY Broad electronics design background including: digital/analog circuit design at PCB, IC and system levels, EMC design/test, and lab characterization of circuit performance.

EMPLOYMENT

7/19-present **Senior Research Engineer, University of Michigan, Ann Arbor, Michigan**

- System integration of millimeter scale ultra-low power systems with focus on collaborative research projects.
- System design, PCB layout, code development, test and characterization of multi-chip systems.

3/16-7/19 **Hardware Engineering Manager, Applied Dynamics International, Ann Arbor, Michigan**

- Managing team of seven engineers and CAD designers in hardware design of PC-based real-time simulation and data acquisition systems for aerospace applications.
- Hardware system design and system integration lead for new Rolls-Royce Deutschland test facility.
- Led efforts in EMC test, CE certification for European market and development of design guides.

6/13-3/16 **Senior Electrical Engineer, Applied Dynamics International, Ann Arbor, Michigan**

- Design aspects include: custom cabling, interface PCBs, system BOM, component selection and manufacturing documentation.
- Updated ECR process; standardized cable and PCB manufacturing checks; ISO 9001 documentation.

10/04-2/13 **Staff Electronic Design Engineer, Silicon Frequency Control, Integrated Device Technology/Mobius Microsystems, Ann Arbor, Michigan**

- 3rd engineer hired at Mobius (acquired by IDT in 2010). Contributed in both digital and analog design, characterization and CAD integration in the development of all-silicon CMOS frequency references.
- Responsible for design, layout and characterization of all I/O circuits including a universal I/O supporting programmable-drive CMOS, LVPECL, LVDS and HCSL up to 650MHz and a 1.6GHz CML output driver. Developed ESD protection, characterization boards and characterized jitter performance.
- Led two successful IP design efforts including: a hybrid oscillator for the UM WIMS processor and a low-power ring oscillator for a commercial customer.
- Gained extensive lab characterization and debug experience. Utilized in-house Python-based lab test automation environment to measure device performance. Very familiar with sampling and real-time scopes, spectrum analyzers, DMMs, SMUs, supplies, thermal chambers and solder rework.
- Debugged difficult silicon issues including: frequency drift on startup, intermittent NVM corruption, latch-up, I/O/core noise sensitivities and loops reducing inductor Q. Developed platform to test effects of stress on frequency, including board and fixture design.
- Responsible for all early digital design. Implemented control, serial port, NVM interface and automatic frequency trim in Verilog. Brought in ARM-Artisan standard cell libraries for digital designs. Added BIST and other testability features to design. Experience in full-custom divider design and architecture.
- Integrated Mentor Graphics Calibre for physical verification. Provided support for Cadence and PDK issues. Performed all early spiral inductor modeling using ASITIC and eventually purchased HFSS.
- Implemented first demo boards for Mobius, including board design, layout and CPLD programming.

11/98-10/04 **Adjunct Lecturer, University of Michigan, Ann Arbor, Michigan**

- Instructor, EECS 427, VLSI Design I, key senior/graduate-level design course in VLSI curriculum.
- 20-60 students/term with designs regularly placing high in national VLSI design contests.
- Modified design flow to use industry standard Cadence and Synopsys design tools.

11/98-10/04 **CAD Applications Engineer, University of Michigan, Ann Arbor, Michigan**

- Responsible for installation, end-user support, tutorial development and integration of over 80 commercial electronic CAD applications used in research and coursework in EECS.
- Brought Cadence tools into mainstream use in EECS department. Developed CAD applications support website. Technical liaison for MOSIS microelectronic fabrication service.

- Presented CAD infrastructure for Intel's model VLSI curriculum in Hangzhou, China

3/01-6/07 **Layout Design Consultant, Sensicore, Ann Arbor, Michigan**

- Responsible for all mask layout of Sensicore's chemical sensor devices.

7/91-11/98 **Technical Staff Engineer, Motorola Inc., Semiconductor Products Sector, Austin, Texas**

- CMOS digital/analog design including: specification, Verilog modeling, SPICE simulation, timing/physical verification, synthesis, schematic entry, layout and debug of low power DSPs.
- Responsible for on-chip emulation, multiply/accumulate, ROM, address generation and JTAG designs. Methodology improvements including: detailed capacitance extraction, dynamic timing verification and ROM via programming.
- Managed design efforts of up to six engineers. Responsible for project/resource planning, specification and overall success of the silicon design.
- Performed chip-level integration duties including top-level place and route, physical verification, parasitic extraction and timing verification.

PATENTS AND PUBLICATIONS

- Seven patents issued in the areas of all-silicon frequency references and on-chip emulation.
- Co-authored nine journal and conference publications in the areas of all-silicon frequency references and VLSI education.

SKILLS

- OS/tools: Linux, Windows, Office suite
- CAD: Cadence, Mentor Graphics, Synopsys, Altium
- Programming: Python and shell scripting
- Lab HW: scopes, spectrum analyzers, DMMs, frequency counters, environmental chambers

EDUCATION

The University of Michigan, Ann Arbor, Michigan

- MSEE, BSEE, magna cum laude, Outstanding Teaching Assistant Award